

## MM74HCT74 Dual D-Type Flip-Flop with Preset and Clear

### General Description

The MM74HCT74 utilizes advanced silicon-gate CMOS technology to achieve operation speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and  $\bar{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HCT logic family is functionally and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

### Features

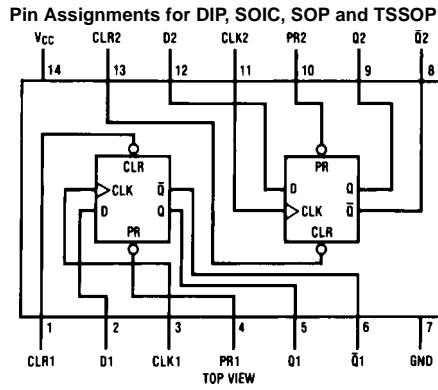
- Typical propagation delay: 20 ns
- Low quiescent current: 40  $\mu$ A maximum (74HCT Series)
- Low input current: 1  $\mu$ A maximum
- Fanout of 10 LS-TTL loads
- Meta-stable hardened

### Ordering Code:

Order Number	Package Number	Package Description
MM74HCT74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
M74HCT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HCT74N_NL	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

### Connection Diagram



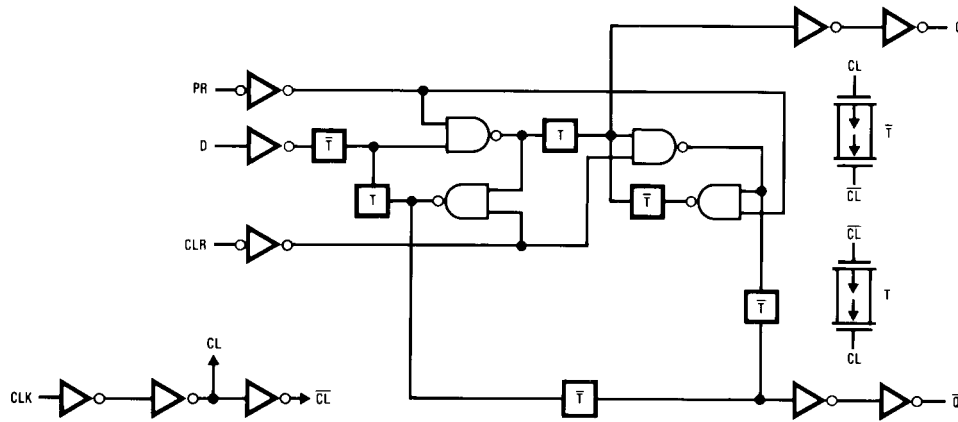
### Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}0$

Q0 = the level of Q before the indicated input conditions were established.

**Note 1:** This configuration is nonstable; that is, it will not persist when pre-set and clear inputs return to their inactive (HIGH) level.

### Logic Diagram



**Absolute Maximum Ratings**(Note 2)

(Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}+1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}+0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.5	5.5	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ )		500	ns

**Note 2:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.**Note 3:** Unless otherwise specified all voltages are referenced to ground.**Note 4:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.**DC Electrical Characteristics** $V_{CC} = 5V \pm 10\%$  (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{ to }85^\circ\text{C}$	$T_A = -55\text{ to }125^\circ\text{C}$	Units
			Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
$V_{IL}$	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu\text{A}$	$V_{CC}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
		$ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5\text{V}$	4.2	3.98	3.84	3.7	V
		$ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5\text{V}$	5.2	4.98	4.84	4.7	V
$V_{OL}$	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu\text{A}$	0	0.1	0.1	0.1	V
		$ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5\text{V}$	0.2	0.26	0.33	0.4	V
		$ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5\text{V}$	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$		$\pm 0.0.5$	$\pm 0.5$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$		2.0	20	80	$\mu\text{A}$
		$V_{IN} = 2.4\text{V}$ or $0.5\text{V}$ (Note 5)		0.3	0.4	0.5	mA

**Note 5:** This is measured per pin. All other inputs are held at  $V_{CC}$  Ground.

**AC Electrical Characteristics** $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$ 

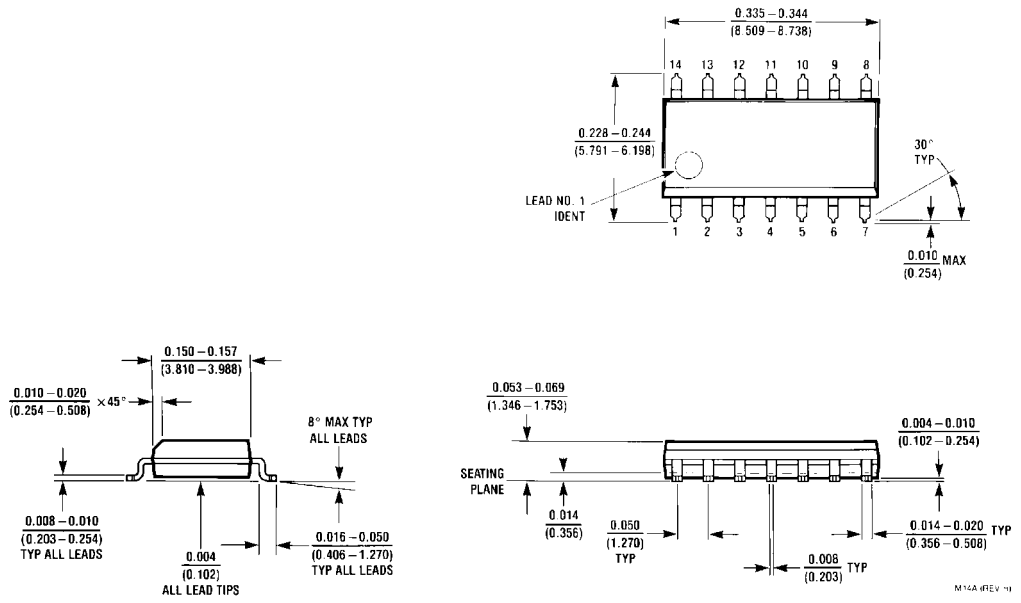
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency from Clock to Q or $\bar{Q}$		50	30	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Clock to Q or $\bar{Q}$		18	30	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		18	30	ns
$t_{REM}$	Minimum Removal Time, Preset or Clear to Clock			20	ns
$t_S$	Minimum Setup Time Data to Clock			20	ns
$t_H$	Minimum Hold Time Clock to Data		-3	0	ns
$t_W$	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

**AC Electrical Characteristics** $V_{CC} = 5.0V \pm 10\%$ ,  $C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$  unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		$T_A = -40^\circ \text{ to } +85^\circ C$	Units
			Typ	Guaranteed Limits		
$f_{MAX}$	Maximum Operating Frequency			27	21	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from Clock to Q or $\bar{Q}$		21	35	44	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		21	35	44	ns
$t_{REM}$	Minimum Removal Time Preset or Clear to Clock			20	25	ns
$t_S$	Minimum Setup Time Data to Clock			20	25	ns
$t_H$	Minimum Hold Time Clock to Data		-3	0	0	ns
$t_W$	Minimum Pulse Width Clock, Preset or Clear		9	16	20	ns
$t_r$ , $t_f$	Maximum Clock Input Rise and Fall Time			500	500	ns
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time			15	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 6)	(per flip-flop)	10			pF
$C_{IN}$	Maximum Input Capacitance		5	10	10	pF

**Note 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

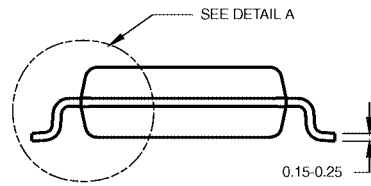
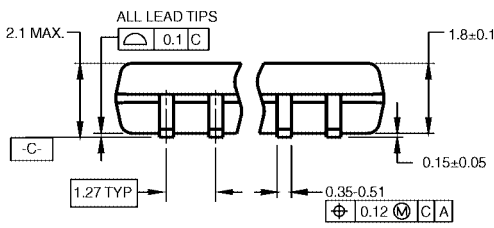
**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

M14A (REV. 11)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

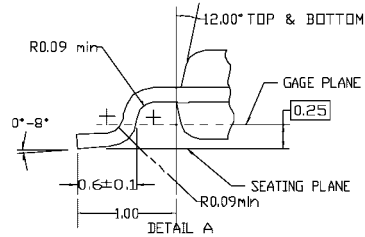
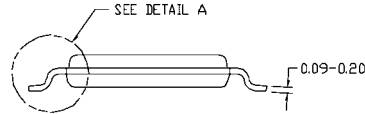
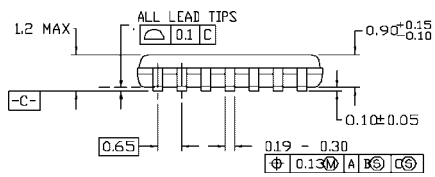
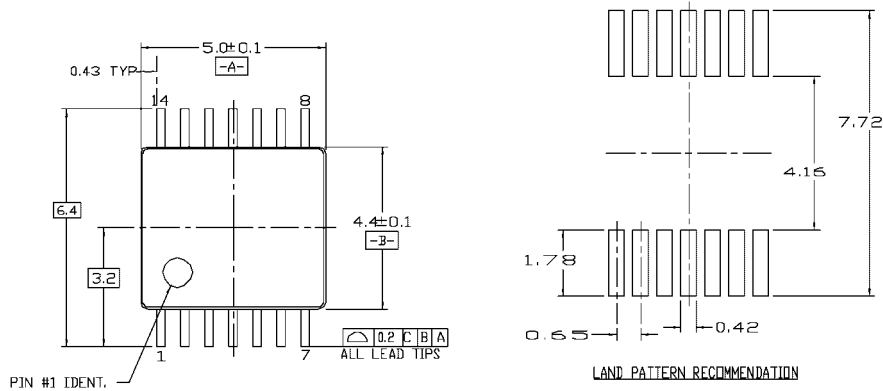
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



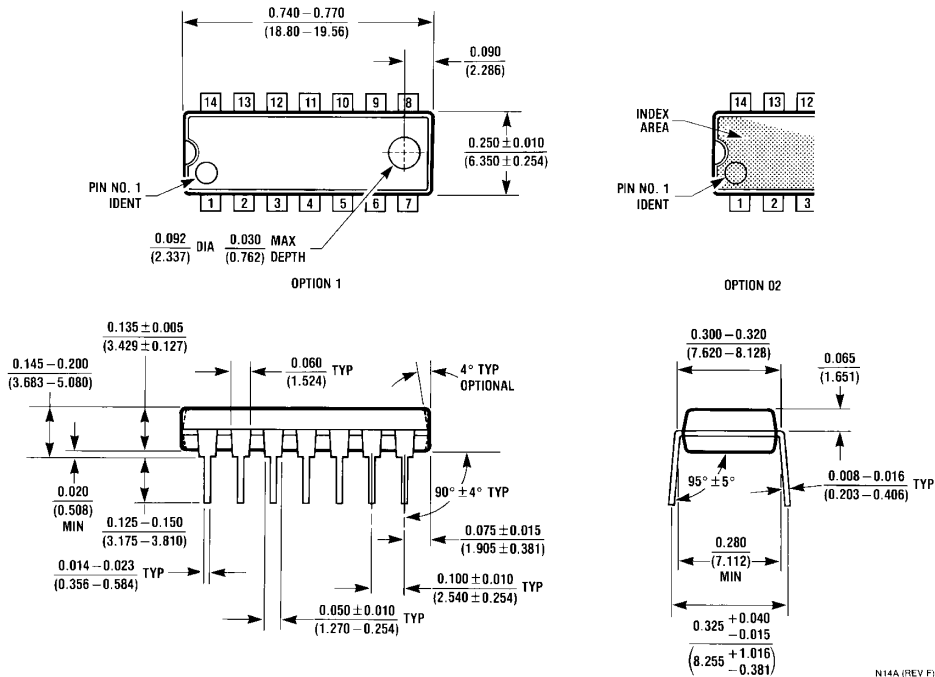
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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