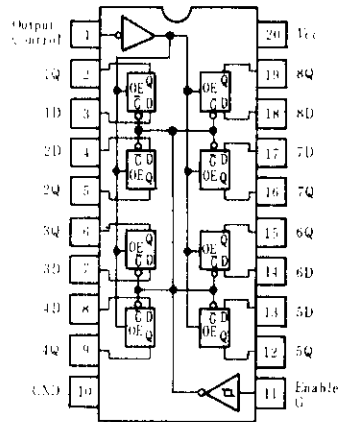


# HD74LS373 Octal D-type Transparent Latches (with three-state outputs)

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

## PIN ARRANGEMENT



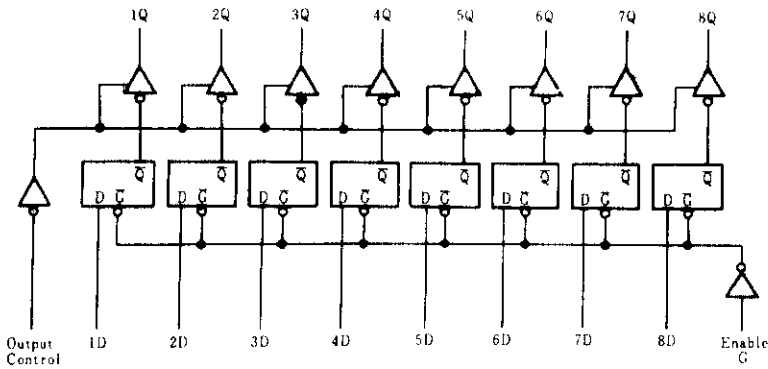
(Top View)

## FUNCTION TABLE

Inputs			Output
Output control	Enable G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

Notes: H = high level, L = low level,  
X = irrelevant  
Q<sub>0</sub> = level of Q before the indicated steady-state input conditions were established.  
Z = off (high-impedance) state of a three-state output

## BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage	V <sub>OH</sub>	—	—	5.5	V
Output current	I <sub>OH</sub>	—	—	-2.6	mA
	I <sub>OL</sub>	—	—	24	mA
Enable pulse width	t <sub>w</sub>	"H" level	15	—	ns
		"L" level	15	—	ns
Data setup time	t <sub>su</sub>	5 ↓	—	—	ns
Data hold time	t <sub>h</sub>	25 ↓	—	—	ns

Note) ↓ : The arrow indicates the falling edge of clock pulse.

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$	Data inputs	—	—	0.7	V	
G, Output control inputs		—	—	0.8	V		
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = V_{IL\text{max}}$ , $I_{OH} = -2.6\text{mA}$	2.4	—	—	V	
	$V_{OL}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = V_{IL\text{max}}$	$I_{OL} = 12\text{mA}$	—	—	0.4	V
$I_{OL} = 24\text{mA}$			—	—	0.5	V	
Off-state output current	$I_{OZH}$	$V_{CC} = 5.25\text{V}$ , $V_{IH} = 2\text{V}$	$V_O = 2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{OZL}$		$V_O = 0.4\text{V}$	—	—	-20	$\mu\text{A}$
Input current	$I_{IH}$	$V_{CC} = 5.25\text{V}$ , $V_I = 2.7\text{V}$	—	—	20	$\mu\text{A}$	
	$I_{IL}$	$V_{CC} = 5.25\text{V}$ , $V_I = 0.4\text{V}$	—	—	-0.4	mA	
	$I_I$	$V_{CC} = 5.25\text{V}$ , $V_I = 7\text{V}$	—	—	0.1	mA	
Short-circuit output current	$I_{OS}$	$V_{CC} = 5.25\text{V}$	-30	—	-130	mA	
Supply current	$I_{CC}$	$V_{CC} = 5.25\text{V}$ , $V_I = 4.5\text{V}$ (Output control)	—	24	40	mA	
Input clamp voltage	$V_{IK}$	$V_{CC} = 4.75\text{V}$ , $I_{IN} = -18\text{mA}$	—	—	-1.5	V	

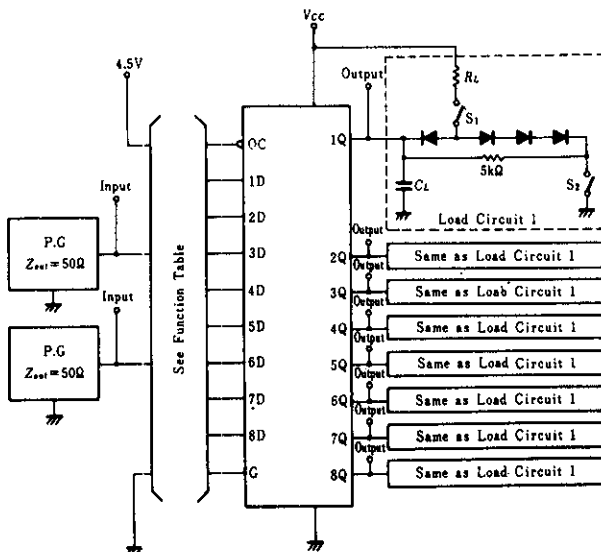
\*  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

## ■ SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{V}$ , $T_a = 25^\circ\text{C}$ )

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	$t_{PLH}$	D	Q	$C_L = 45\text{pF}$ $R_L = 667\Omega$	—	12	18	ns
	$t_{PHL}$				—	12	18	
	$t_{PLH}$	G	Q		—	20	30	
	$t_{PHL}$				—	18	30	
Output enable time	$t_{ZH}$	OC	Q		—	15	28	
	$t_{ZL}$				—	25	36	
Output disable time	$t_{HZ}$	OC	Q	$C_L = 5\text{pF}$ $R_L = 667\Omega$	—	12	20	
	$t_{LZ}$				—	15	25	

## ■ TESTING METHOD

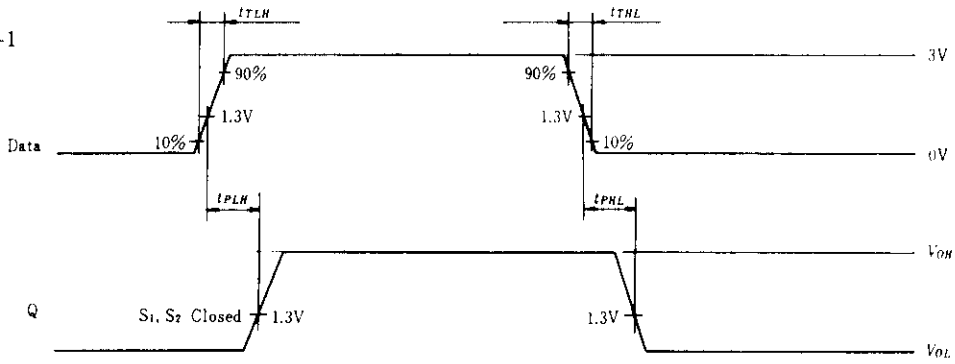
Test Circuit



- Notes:
1.  $C_L$  includes probe jig capacitance.
  2. All diodes are 1S2074 (H).

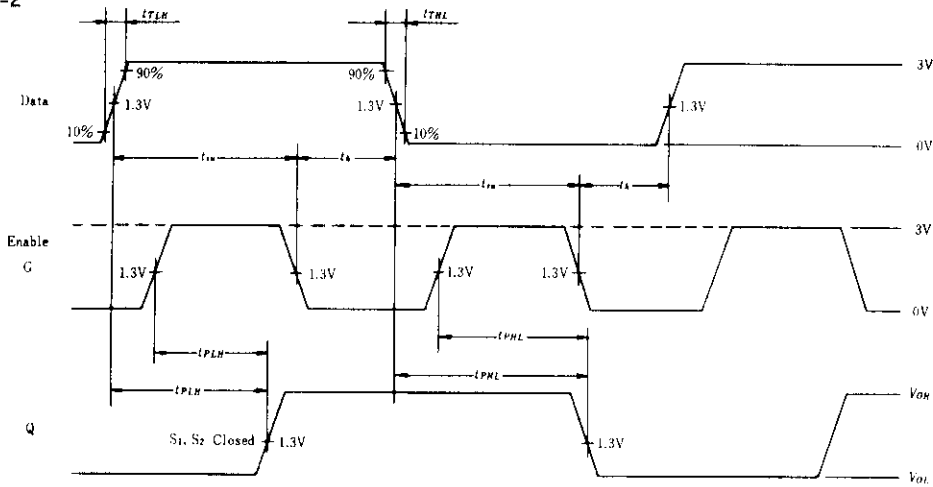
# HD74LS373

Waveform-1



Notes: Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%

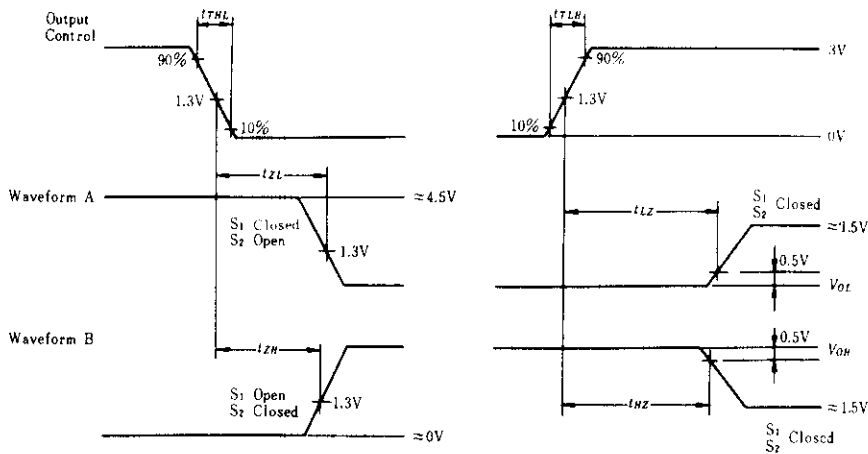
Waveform-2



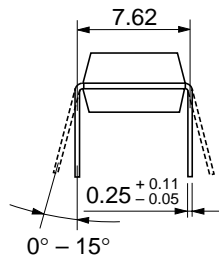
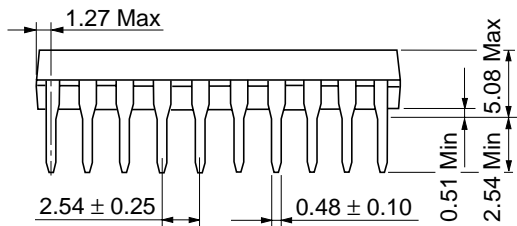
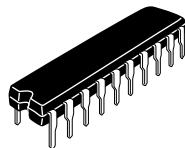
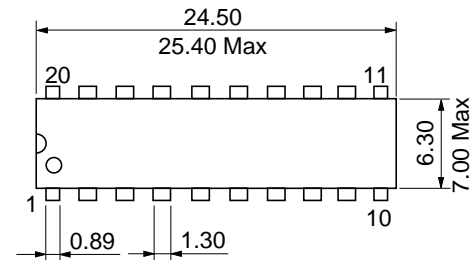
Note: Enable input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$

Data input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , G input is high.

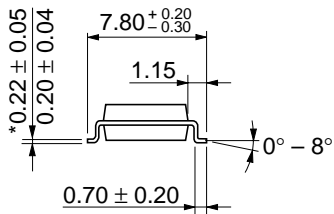
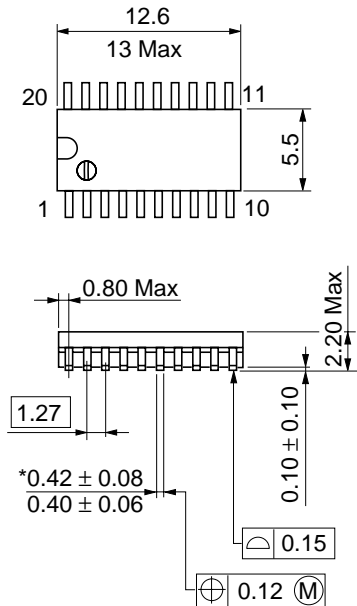
Waveform-3



Notes: 1. Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%  
2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

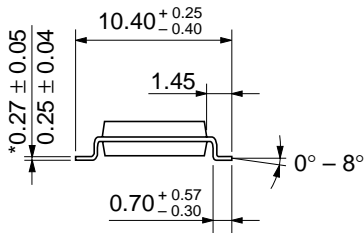
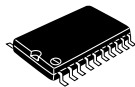
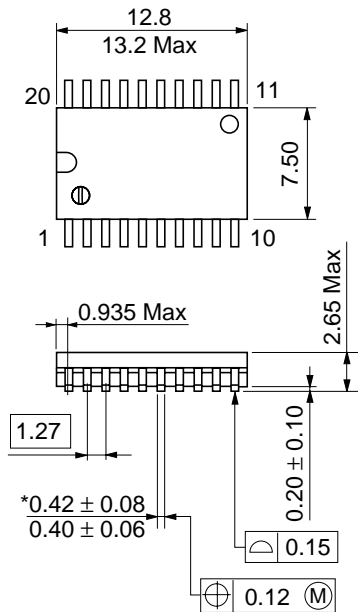


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

\*Dimension including the plating thickness  
Base material dimension



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

\*Dimension including the plating thickness  
 Base material dimension

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