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Jameco Part Number 1061340

WIDEBAND, LOW NOISE, LOW DISTORTION FULLY DIFFERENTIAL AMPLIFIER

FEATURES

- **Fully Differential Architecture**
- **Centered Input Common-mode Range**
- **Output Common-Mode Control**
- **Minimum Gain of 2V/V (6 dB)**
- **Bandwidth: 1900 MHz**
- **Slew Rate: 6600 V/µs**
- **1% Settling Time: 2 ns**
- **HD_2: –75 dBc at 100 MHz**
- **HD_3: –80 dBc at 100 MHz**
- **OIP_3: 37 dBm at 70 MHz**
- **Input Voltage Noise: 1.9 nV/$\sqrt{Hz}$ (f >10 MHz)**
- **Power Supply Voltage: 3 V to 5 V**
- **Power Supply Current: 37.7 mA**
- **Power-Down Current: 0.65 mA**

APPLICATIONS

- **5 V Data Acquisition Systems High Linearity ADC Amplifier**
- **Wireless Communication**
- **Medical Imaging**
- **Test and Measurement**

RELATED PRODUCTS

Device	Min. Gain	Common Mode Range of Input*
THS4508	6 dB	–0.3V to 2.3V
THS4509	6 dB	0.75V to 4.25V
THS4511	0 dB	–0.3V to 2.3V
THS4513	0 dB	0.75V to 4.25V
*Note: Assumes a 5V single-ended power supply		

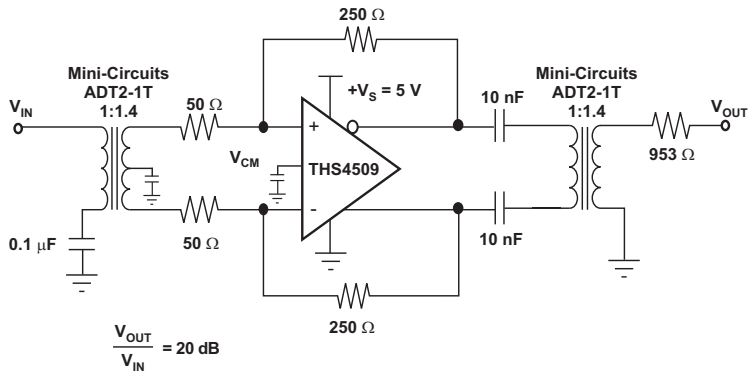
DESCRIPTION

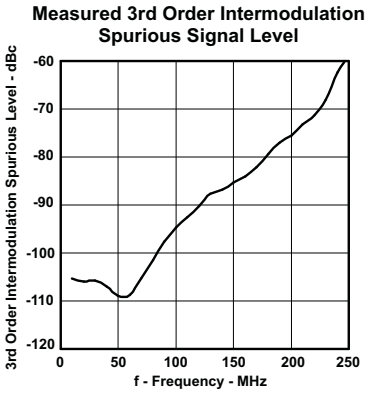
The THS4509 is a wideband, fully differential op amp designed for 5-V data acquisition systems. It has a low noise at 1.9 nV/$\sqrt{Hz}$, and low harmonic distortion of –75 dBc HD_2 and –80 dBc HD_3 at 100 MHz with 2 Vpp, G = 10 dB, and 1 kΩ load. Slew rate is high at 6600 Vµs, and with settling time of 2 ns to 1% (2 V step), it is ideal for pulsed applications. It is designed for minimum gain of 6 dB, but is optimized for gain of 10 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 3 mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4 mV differential offset voltage. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The input and output are optimized for best performance with their common-mode voltages set to mid-supply. Along with high performance at low power supply voltage, this makes for high performance single supply 5-V data acquisition systems. The combined performance of the THS4509 in a gain of 10 dB driving the ADS5500 ADC, sampling at 125 MSPS, is 81 dBc SFDR and 69.1 dBc SNR with a –1 dBFS signal at 70 MHz.

The THS4509 is offered in a Quad 16-pin leadless QFN package (RGT), and is characterized for operation over the full industrial temperature range from –40°C to 85°C.





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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION

TEMPERATURE	PACKAGED DEVICES	
	QUAD QFN(1) (2) (RGT-16)	SYMBOL
–40°C to 85°C	THS4509RGTT	–
	THS4509RGTR	

(1) This package is available taped and reeled. The R suffix standard quantity is 3000. The T suffix standard quantity is 250.
(2) The exposed thermal pad is electrically isolated from all other pins. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_{S-} to V_{S+}	Supply voltage		6 V
V_I	Input voltage		$\pm V_S$
V_{ID}	Differential input voltage		4 V
I_O	Output current(1)		200 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature		150°C
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	ESD ratings	HBM	2000
		CDM	1500
		MM	100

(1) The THS4509 incorporates a (QFN) exposed thermal pad on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the QFN thermally enhanced package.

DISSIPATION RATINGS TABLE PER PACKAGE

PACKAGE	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \le 25°C$	$T_A = 85°C$
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

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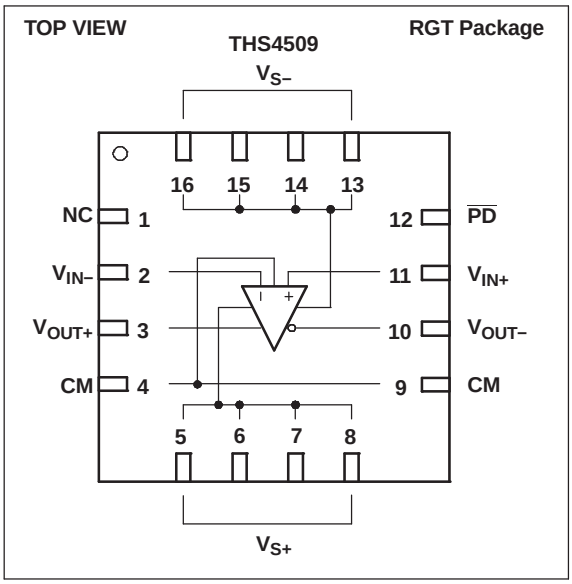
DEVICE INFORMATION



TERMINAL FUNCTIONS

TERMINAL (RGT PACKAGE)		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	V_{IN-}	Inverting amplifier input
3	V_{OUT+}	Non-inverted amplifier output
4,9	CM	Common-mode voltage input
5,6,7,8	V_{S+}	Positive amplifier power supply input
10	V_{OUT-}	Inverted amplifier output
11	V_{IN+}	Non-inverting amplifier input
12	$\overline{PD}$	Powerdown, $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation
13,14,15,16	V_{S-}	Negative amplifier power supply input

SPECIFICATIONS; $V_{S+} - V_{S-} = 5$ V:

Test conditions unless otherwise noted: V_{S+} = +2.5 V, V_{S-} = –2.5 V, G = 10 dB, CM = open, V_O = 2 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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SPECIFICATIONS; $V_{S+} - V_{S-}$ = 5 V: (continued)

Test conditions unless otherwise noted: V_{S+} = +2.5 V, V_{S-} = –2.5 V, G = 10 dB, CM = open, V_O = 2 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Small-Signal Bandwidth	G = 6 dB, V_O = 100 mVpp			2.0		GHz	
	G = 10 dB, V_O = 100 mVpp			1.9		GHz	
	G = 14 dB, V_O = 100 mVpp			600		MHz	
	G = 20 dB, V_O = 100 mVpp			275		MHz	
Gain-Bandwidth Product	G = 20 dB			3		GHz	
Bandwidth for 0.1dB flatness	G = 10 dB, V_O = 2 Vpp			300		MHz	
Large-Signal Bandwidth	G = 10 dB, V_O = 2 Vpp			1.5		GHz	
Slew Rate (Differential)	2V Step			6600		V/µs	
Rise Time				0.5		ns	
Fall Time				0.5			
Settling Time to 1%				2			
Settling Time to 0.1%				10			
2nd Order Harmonic Distortion	f = 10 MHz			–104		dBc	
	f = 50 MHz			–80			
	f = 100 MHz			–68			
3rd Order Harmonic Distortion	f = 10 MHz			–108		dBc	C
	f = 50 MHz			–92			
	f = 100 MHz			–81			
2nd Order Intermodulation Distortion	200 kHz Tone Spacing, R_L = 499 Ω	f_C = 70 MHz		–78		dBc	
		f_C = 140 MHz		–64			
3rd Order Intermodulation Distortion		f_C = 70 MHz		–95			
		f_C = 140 MHz		–78			
2nd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω, referenced to 50 Ω output	f_C = 70 MHz		78		dBm	
		f_C = 140 MHz		58			
3rd Order Output Intercept Point		f_C = 70 MHz		43			
		f_C = 140 MHz		38			
1-dB Compression Point	f_C = 70 MHz			12.2		dBm	
	f_C = 140 MHz			10.8			
Noise Figure	50 Ω System, 10 MHz			17.1		dB	
Input Voltage Noise	f > 10 MHz			1.9		nV/√Hz	
Input Current Noise	f > 10 MHz			2.2		pA/√Hz	
DC PERFORMANCE							
Open-Loop Voltage Gain (A_{OL})				68		dB	C
Input Offset Voltage	T_A = 25°C			1	4	mV	A
	T_A = –40°C to 85°C			1	5	mV	
Average Offset Voltage Drift	T_A = –40°C to 85°C			2.6		µV/°C	B
Input Bias Current	T_A = 25°C			8	15.5	µA	A
	T_A = –40°C to 85°C			8	18.5		
Average Bias Current Drift	T_A = –40°C to 85°C			20		nA/°C	B
Input Offset Current	T_A = 25°C			1.6	3.6	µA	A
	T_A = –40°C to 85°C			1.6	7		
Average Offset Current Drift	T_A = –40°C to 85°C			4		nA/°C	B
INPUT							
Common-Mode Input Range High				1.75		V	B
Common-Mode Input Range Low				–1.75			
Common-Mode Rejection Ratio				90		dB	
Differential Input Impedance				1.35 || 1.77		MΩ || pF	C

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SPECIFICATIONS; $V_{S+} - V_{S-}$ = 5 V: (continued)

Test conditions unless otherwise noted: V_{S+} = +2.5 V, V_{S-} = –2.5 V, G = 10 dB, CM = open, V_O = 2 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Common-Mode Input Impedance				1.02 || 2.26		MΩ || pF	C
OUTPUT							
Maximum Output Voltage High	Each output with 100 Ω to mid-supply	T_A = 25°C	1.2	1.4		V	A
		T_A = –40°C to 85°C	1.1	1.4			
Minimum Output Voltage Low		T_A = 25°C		–1.4	–1.2	V	
		T_A = –40°C to 85°C		–1.4	–1.1		
Differential Output Voltage Swing			4.8	5.6		V	
	T_A = –40°C to 85°C		4.4				
Differential Output Current Drive	R_L = 10 Ω			96		mA	C
Output Balance Error	V_O = 100 mV, f = 1 MHz			–49		dB	
Closed-Loop Output Impedance	f = 1 MHz			0.3		Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-Signal Bandwidth				700		MHz	C
Slew Rate				110		V/µs	
Gain				1		V/V	
Output Common-Mode Offset from CM input	1.25 V < CM < 3.5 V			5		mV	
CM Input Bias Current	1.25 V < CM < 3.5 V			±40		µA	
CM Input Voltage Range				–1.5 to 1.5		V	
CM Input Impedance				23 || 1		kΩ || pF	
CM Default Voltage				0		V	
POWER SUPPLY							
Specified Operating Voltage			3	5	5.25	V	C
Maximum Quiescent Current	T_A = 25°C			37.7	40.9	mA	A
	T_A = –40°C to 85°C			37.7	41.9		
Minimum Quiescent Current	T_A = 25°C		34.5	37.7		mA	
	T_A = –40°C to 85°C		33.5	37.7			
Power Supply Rejection (PSRR)				90		dB	C
POWERDOWN	Referenced to V_{S-}						
Enable Voltage Threshold	Assured *on* above 2.1 V + V_{S-}			>2.1 + V_{S-}		V	C
Disable Voltage Threshold	Assured *off* below 0.7 V + V_{S-}			<0.7 + V_{S-}		V	
Powerdown Quiescent Current	T_A = 25°C			0.65	0.9	mA	A
	T_A = –40°C to 85°C			0.65	1		
Input Bias Current	$\overline{PD}$ = V_{S-}			100		µA	C
Input Impedance				50 || 2		kΩ || pF	
Turn-on Time Delay	Measured to output on			55		ns	
Turn-off Time Delay	Measured to output off			10		µs	

SPECIFICATIONS; $V_{S+} - V_{S-}$ = 3 V:

Test conditions unless otherwise noted: V_{S+} = +1.5 V, V_{S-} = –1.5 V, G = 10 dB, CM = open, V_O = 1 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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SPECIFICATIONS; $V_{S+} - V_{S-}$ = 3 V: (continued)

Test conditions unless otherwise noted: V_{S+} = +1.5 V, V_{S-} = –1.5 V, G = 10 dB, CM = open, V_O = 1 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Small-Signal Bandwidth	G = 6 dB, V_O = 100 mVpp			1.9		GHz	
	G = 10 dB, V_O = 100 mVpp			1.6		GHz	
	G = 14 dB, V_O = 100 mVpp			625		MHz	
	G = 20 dB, V_O = 100 mVpp			260		MHz	
Gain-Bandwidth Product	G = 20 dB			3		GHz	
Bandwidth for 0.1dB flatness	G = 10 dB, V_O = 1 Vpp			400		MHz	
Large-Signal Bandwidth	G = 10 dB, V_O = 1 Vpp			1.5		GHz	
Slew Rate (Differential)	2V Step			3500		V/µs	
Rise Time				0.25		ns	
Fall Time				0.25			
Settling Time to 1%				1			
Settling Time to 0.1%				10			
2nd Order Harmonic Distortion	f = 10 MHz			–107		dBc	
	f = 50 MHz			–83			
	f = 100 MHz			–60			
3rd Order Harmonic Distortion	f = 10 MHz			–87		dBc	C
	f = 50 MHz			–65			
	f = 100 MHz			–54			
2nd Order Intermodulation Distortion	200 kHz Tone Spacing, R_L = 499 Ω	f_C = 70 MHz		–77		dBc	
		f_C = 140 MHz		–54			
3rd Order Intermodulation Distortion		f_C = 70 MHz		–77			
		f_C = 140 MHz		–62			
2nd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω	f_C = 70 MHz		72		dBm	
		f_C = 140 MHz		52			
3rd Order Output Intercept Point		f_C = 70 MHz		38.5			
		f_C = 140 MHz		30			
1-dB Compression Point	f_C = 70 MHz			2.2		dBm	
	f_C = 140 MHz			0.25			
Noise Figure	50 Ω System, 10 MHz			17.1		dB	
Input Voltage Noise	f > 10 MHz			1.9		nV/√Hz	
Input Current Noise	f > 10 MHz			2.2		pA/√Hz	
DC PERFORMANCE							
Open-Loop Voltage Gain (A_{OL})				68		dB	
Input Offset Voltage	T_A = 25°C			1		mV	
Average Offset Voltage Drift	T_A = –40°C to 85°C			2.6		µV/°C	
Input Bias Current	T_A = 25°C			6		µA	C
Average Bias Current Drift	T_A = –40°C to 85°C			20		nA/°C	
Input Offset Current	T_A = 25°C			1.6		µA	
Average Offset Current Drift	T_A = –40°C to 85°C			4		nA/°C	

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SPECIFICATIONS; $V_{S+} - V_{S-} = 3$ V: (continued)

Test conditions unless otherwise noted: V_{S+} = +1.5 V, V_{S-} = –1.5 V, G = 10 dB, CM = open, V_O = 1 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
INPUT							
Common-Mode Input Range High				0.75		V	B
Common-Mode Input Range Low				–0.75			
Common-Mode Rejection Ratio				80		dB	
Differential Input Impedance				1.35 || 1.77		MΩ || pF	C
Common-Mode Input Impedance				1.02 || 2.26		MΩ || pF	C
OUTPUT							
Maximum Output Voltage High	Each output with 100 Ω to mid-supply	T_A = 25°C		0.45		V	C
Minimum Output Voltage Low		T_A = 25°C		–0.45		V	
Differential Output Voltage Swing				1.8		V	
Differential Output Current Drive	R_L = 10 Ω			50		mA	
Output Balance Error	V_O = 100 mV, f = 1 MHz			–49		dB	
Closed-Loop Output Impedance	f = 1 MHz			0.3		Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-Signal Bandwidth				570		MHz	C
Slew Rate				60		V/µs	
Gain				1		V/V	
Output Common-Mode Offset from CM input	1.25 V < CM < 3.5 V			4		mV	
CM Input Bias Current	1.25 V < CM < 3.5 V			±40		µA	
CM Input Voltage Range				–1.5 to 1.5		V	
CM Input Impedance				20 || 1		kΩ || pF	
CM Default Voltage				0		V	
POWER SUPPLY							
Specified Operating Voltage				3		V	C
Quiescent Current	T_A = 25°C			34.8		mA	A
Power Supply Rejection (PSRR)				70		dB	C
POWERDOWN	Referenced to V_{S-}						
Enable Voltage Threshold	Assured *on* above 2.1 V + V_{S-}			>2.1 + V_{S-}		V	C
Disable Voltage Threshold	Assured *off* below 0.7 V + V_{S-}			<0.7 + V_{S-}		V	
Powerdown Quiescent Current				0.46		mA	
Input Bias Current	$\overline{PD}$ = V_{S-}			65		µA	
Input Impedance				50 || 2		kΩ || pF	
Turn-on Time Delay	Measured to output on			100		ns	
Turn-off Time Delay	Measured to output off			10		µs	

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TYPICAL CHARACTERISTICS

TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 5$ V

Test conditions unless otherwise noted: V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, G = 10 dB, Single-Ended Input, Input and Output Referenced to Midrail

Small-Signal Frequency Response			Figure 1
Large Signal Frequency Response			Figure 2
Harmonic Distortion	HD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 3
	HD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 4
	HD_2, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 5
	HD_3, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 6
	HD_2, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 7
	HD_3, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 8
	HD_2, G = 10 dB	vs Output voltage	Figure 9
	HD_3, G = 10 dB	vs Output voltage	Figure 10
	HD_2, G = 10 dB	vs Common-mode input voltage	Figure 11
	HD_3, G = 10 dB	vs Common-mode input voltage	Figure 12
Intermodulation Distortion	IMD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 13
	IMD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 14
	IMD_2, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 15
	IMD_3, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 16
	IMD_2, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 17
	IMD_3, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 18
Output Intercept Point	OIP_2	vs Frequency	Figure 19
	OIP_3	vs Frequency	Figure 20
0.1 dB Flatness			Figure 21
S-Parameters		vs Frequency	Figure 22
Transition Rate		vs Output Voltage	Figure 23
Transient Response			Figure 24
Settling Time			Figure 25
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Output Impedance		vs Frequency	Figure 27
Overdrive Recovery			Figure 28
Output Voltage Swing		vs Load Resistance	Figure 29
Turn-Off Time			Figure 30
Turn-On Time			Figure 31
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Open Loop Gain		vs Frequency	Figure 33
Input Referred Noise		vs Frequency	Figure 34
Noise Figure		vs Frequency	Figure 35
Quiescent Current		vs Supply Voltage	Figure 36
Power Supply Current		vs Supply Voltage in Powerdown Mode	Figure 37
Output Balance Error		vs Frequency	Figure 38
CM Input Impedence		vs Frequency	Figure 39
CM Small-Signal Frequency Response			Figure 40
CM Input Bias Current		vs CM Input Voltage	Figure 41
Differential Output Offset Voltage		vs CM Input Voltage	Figure 42
Output Common-Mode Offset		vs CM Input Voltage	Figure 43

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SMALL-SIGNAL FREQUNECY RESPONSE

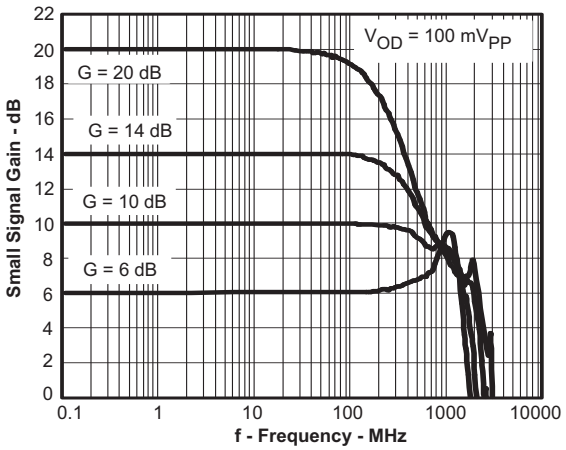

Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

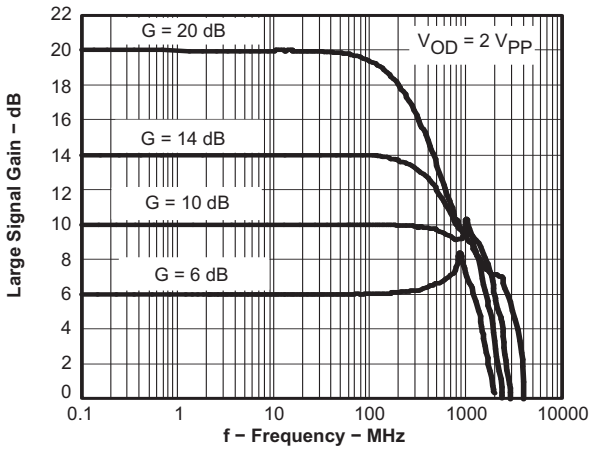

Figure 2.

HD_2 vs FREQUENCY

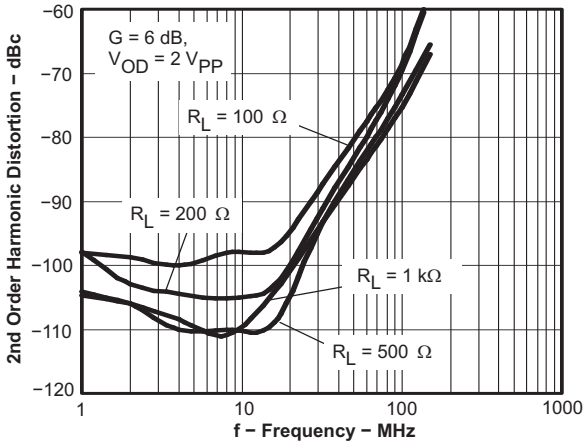

Figure 3.

HD_3 vs FREQUENCY

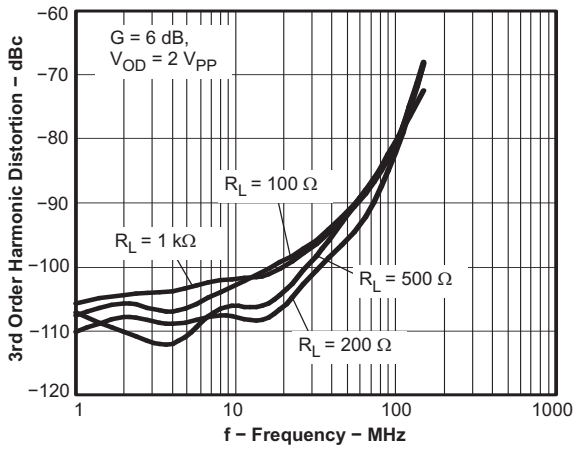

Figure 4.

HD_2 vs FREQUENCY

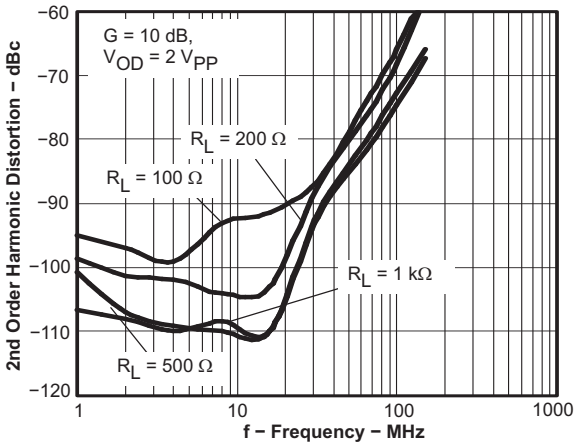

Figure 5.

HD_3 vs FREQUENCY

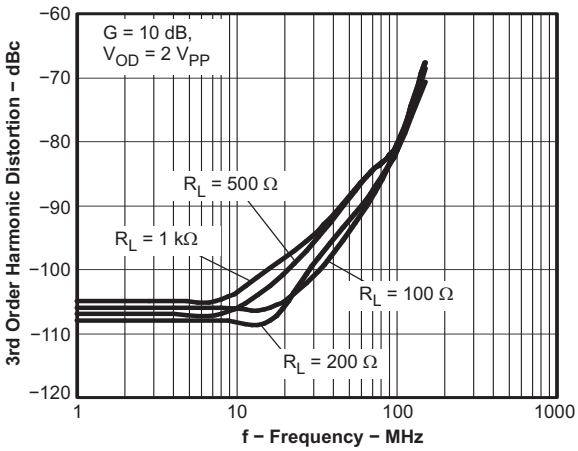

Figure 6.

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HD_2 vs FREQUENCY

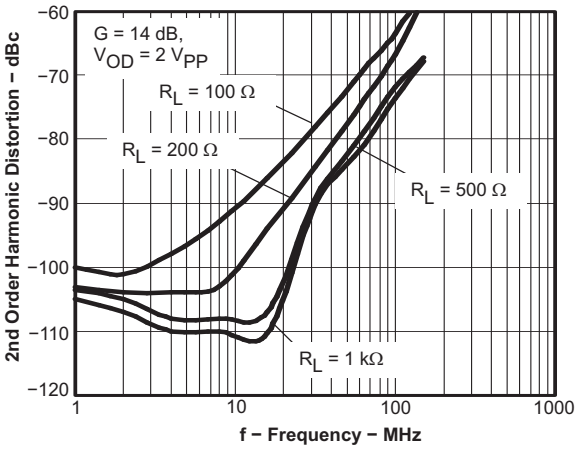

Figure 7.

HD_3 vs FREQUENCY

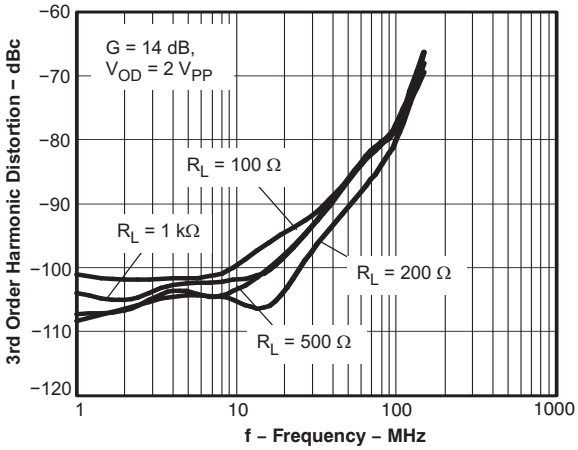

Figure 8.

HD_2 vs OUTPUT VOLTAGE

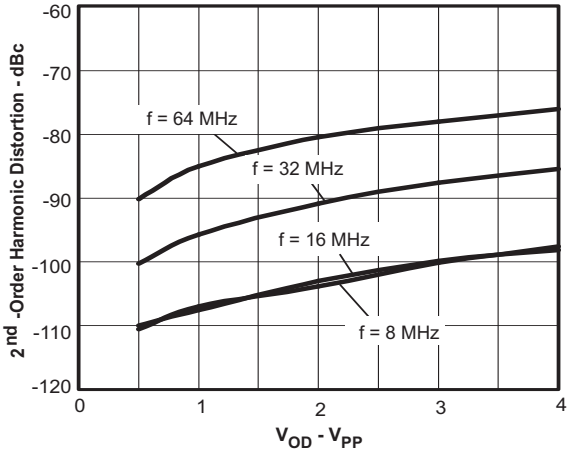

Figure 9.

HD_3 vs OUTPUT VOLTAGE

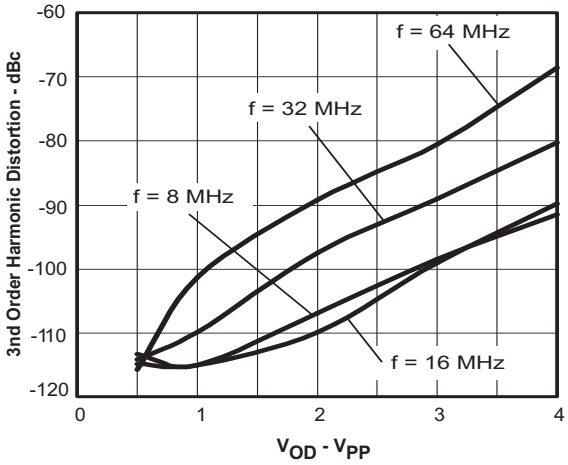

Figure 10.

HD_2 vs COMMON-MODE OUTPUT VOLTAGE

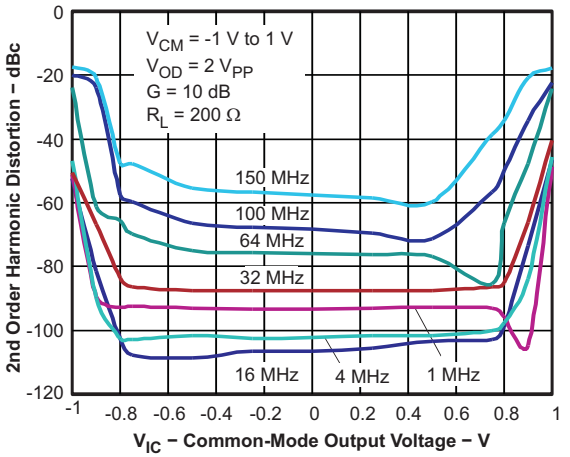

Figure 11.

HD_3 vs COMMON-MODE OUTPUT VOLTAGE

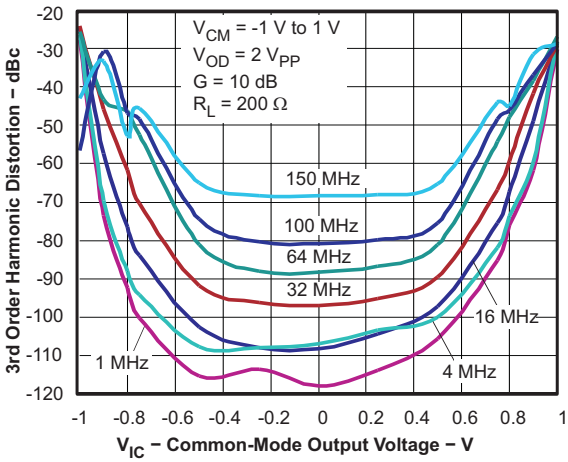

Figure 12.

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IMD$_2$ vs FREQUENCY

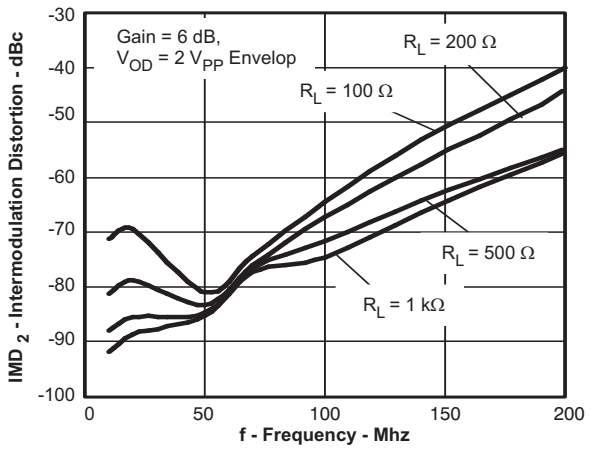

Figure 13.

IMD$_3$ vs FREQUENCY

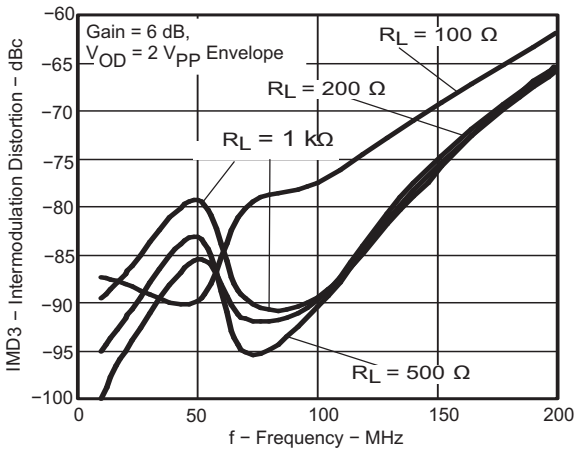

Figure 14.

IMD$_2$ vs FREQUENCY

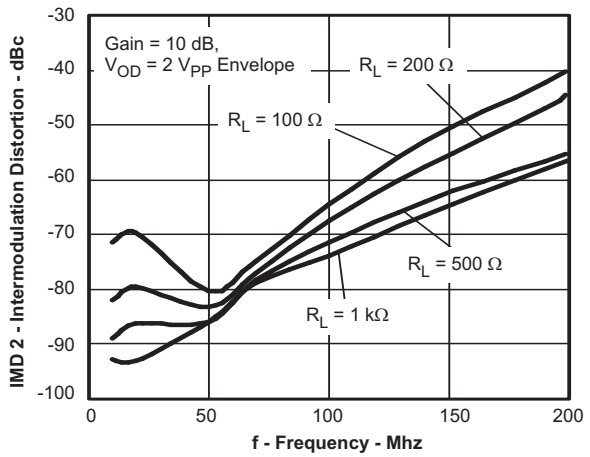

Figure 15.

IMD$_3$ vs FREQUENCY

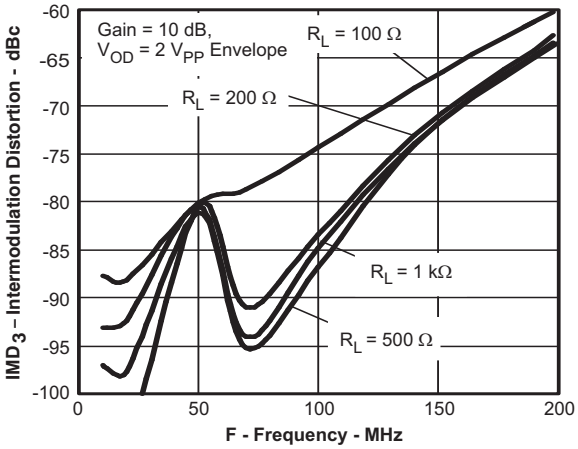

Figure 16.

IMD$_2$ vs FREQUENCY

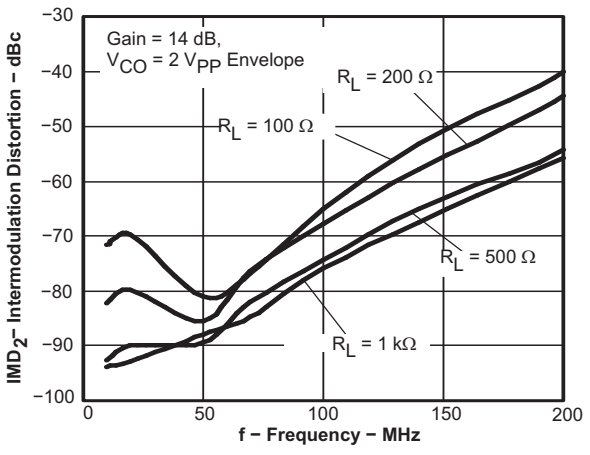

Figure 17.

IMD$_3$ vs FREQUENCY

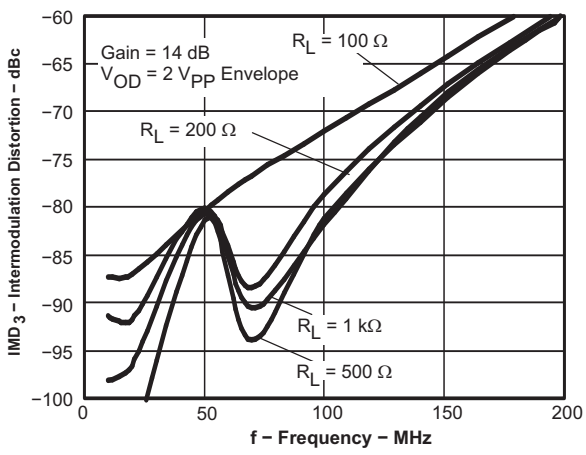

Figure 18.

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OIP_2 vs FREQUENCY

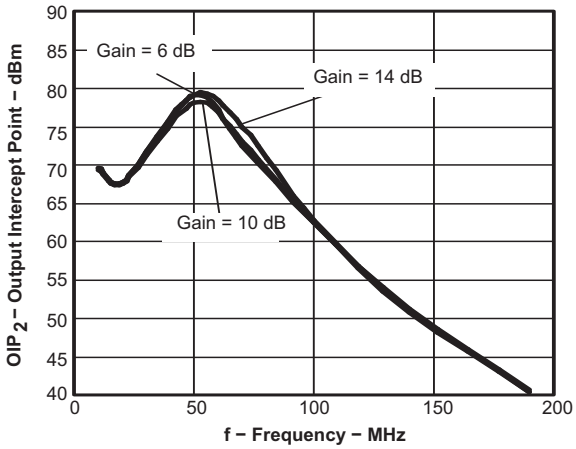

Figure 19.

OIP_3 vs FREQUENCY

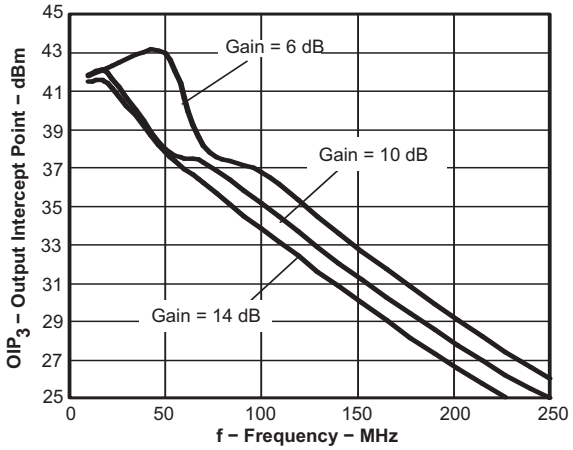

Figure 20.

0.1-dB FLATNESS

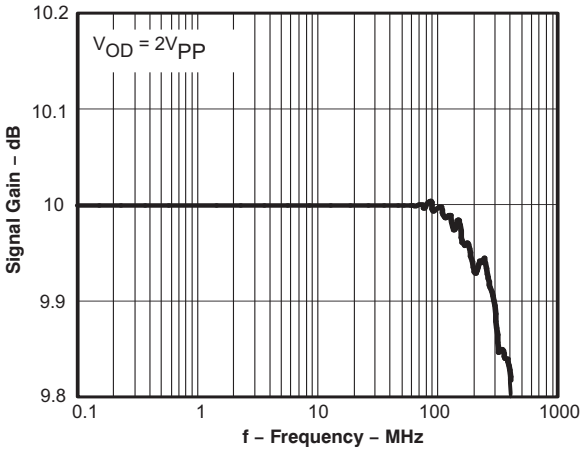

Figure 21.

S-PARAMETERS vs FREQUENCY

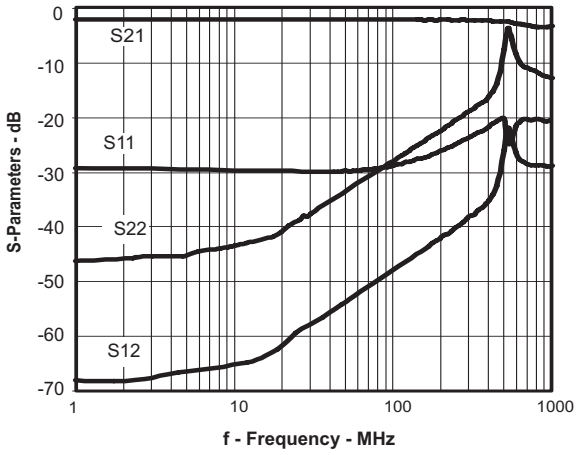

Figure 22.

TRANSISTION RATE vs OUTPUT VOLTAGE

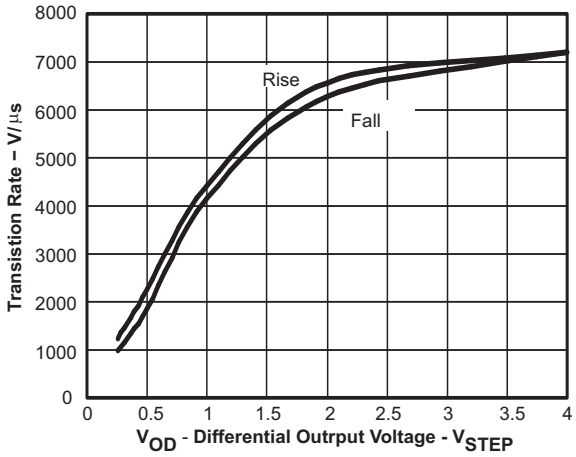

Figure 23.

TRANSIENT RESPONSE

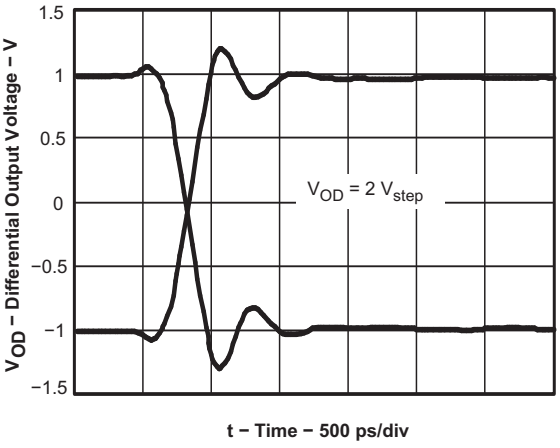

Figure 24.

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SETTLING TIME

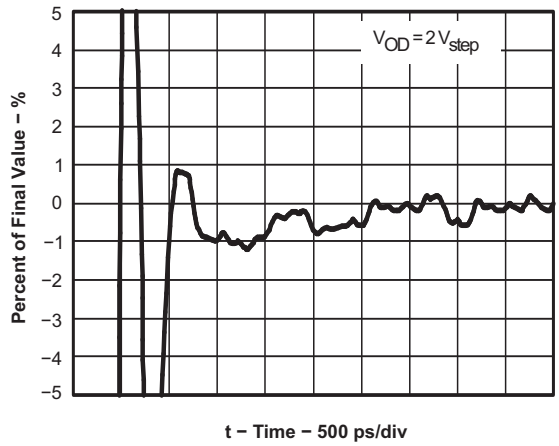

Figure 25.

REJECTION RATIO vs FREQUENCY

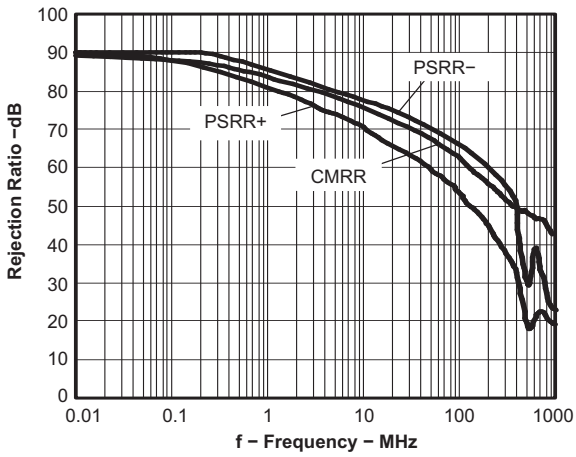

Figure 26.

OUTPUT IMPEDANCE vs FREQUENCY

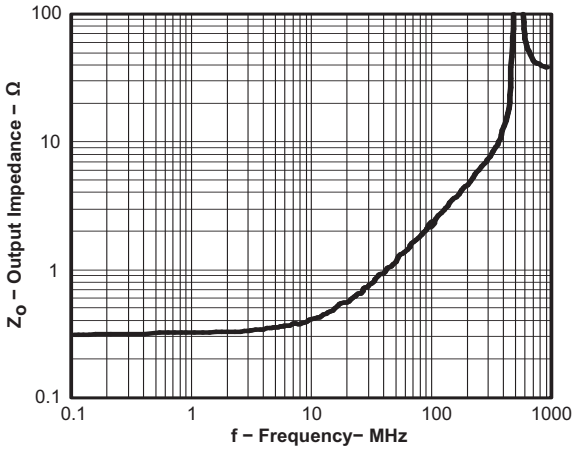

Figure 27.

OVERDRIVE RECOVERY

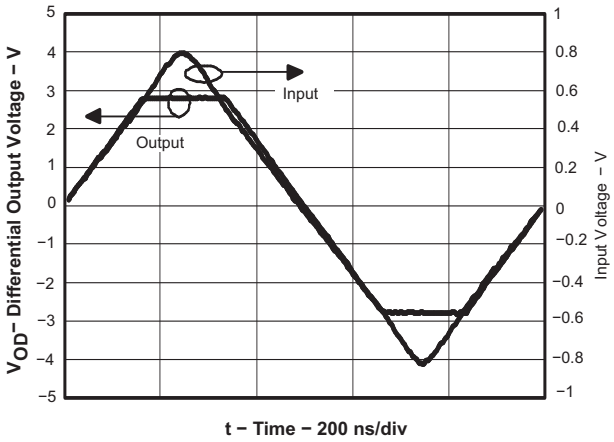

Figure 28.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

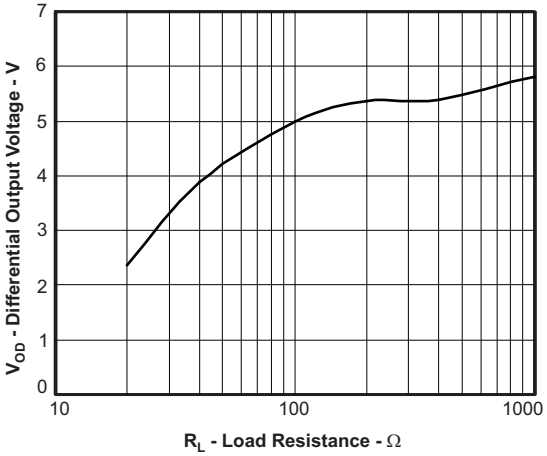

Figure 29.

TURN-OFF TIME

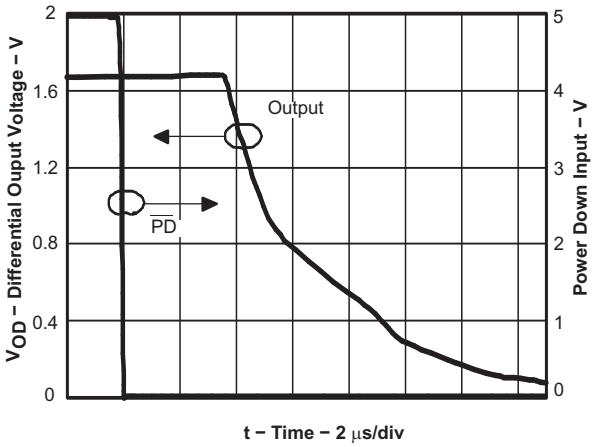

Figure 30.

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TURN-ON TIME

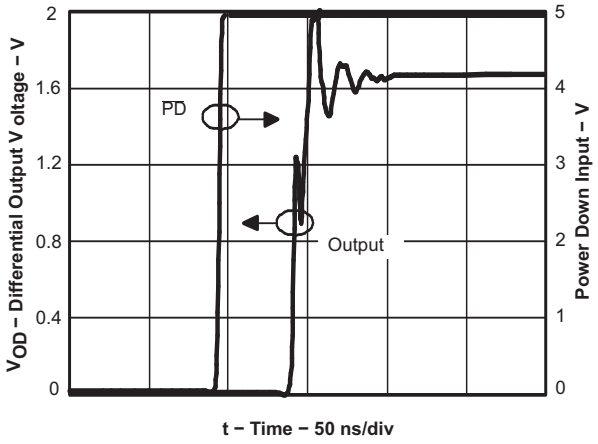

Figure 31.

INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

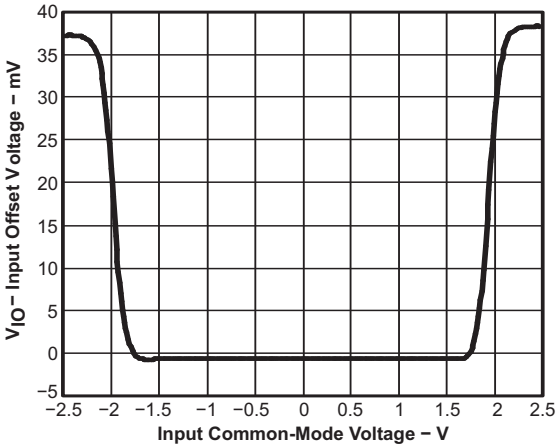

Figure 32.

OPEN LOOP GAIN AND PHASE vs FREQUENCY

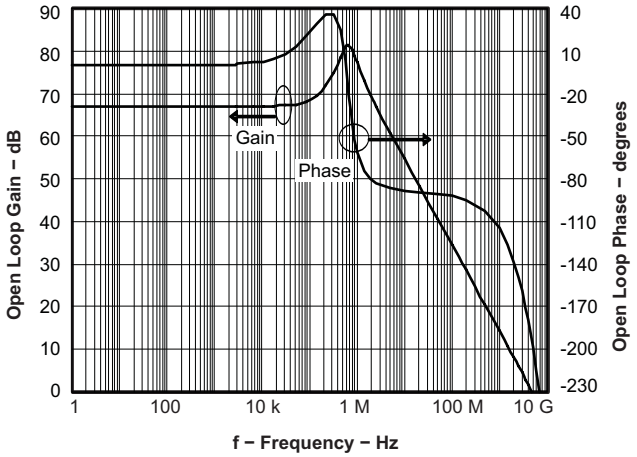

Figure 33.

INPUT REFERRED NOISE vs FREQUENCY

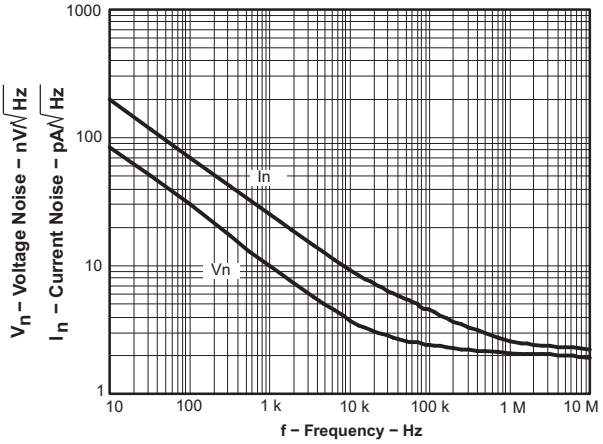

Figure 34.

NOISE FIGURE vs FREQUENCY

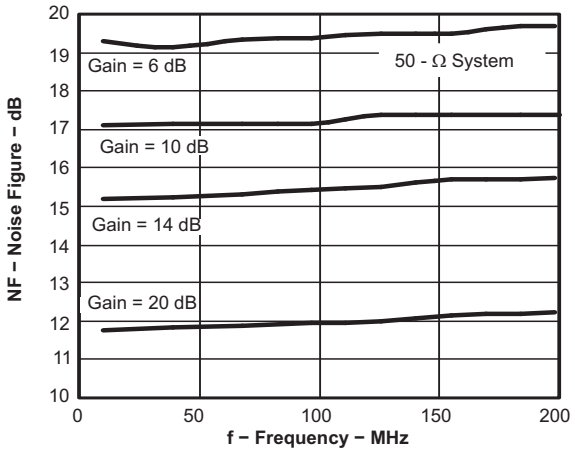

Figure 35.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

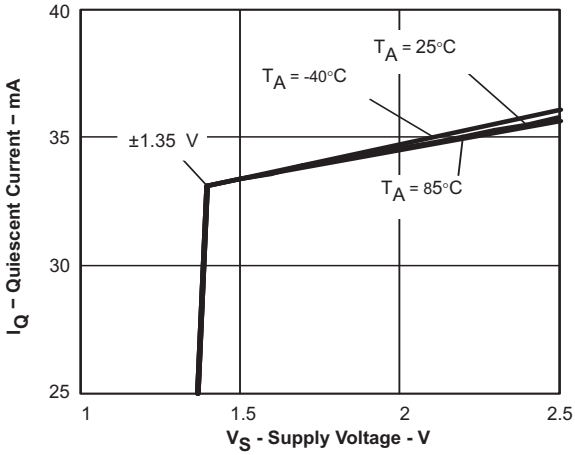

Figure 36.

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POWER SUPPLY CURRENT vs SUPPLY VOLTAGE IN POWER-DOWN MODE

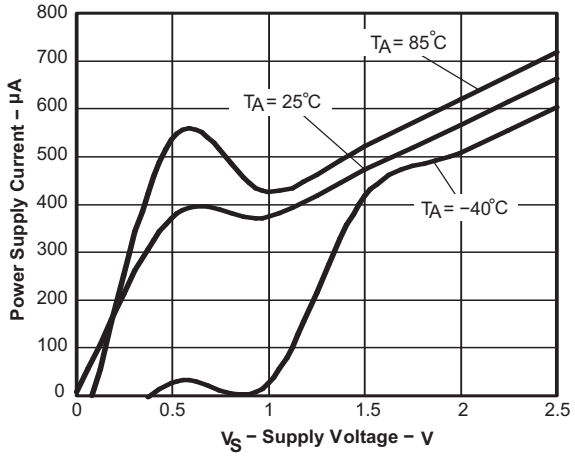

Figure 37.

OUTPUT BALANCE ERROR vs FREQUENCY

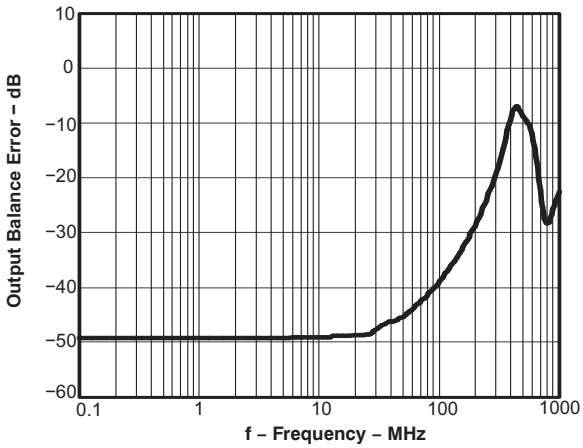

Figure 38.

CM INPUT IMPEDANCE vs FREQUENCY

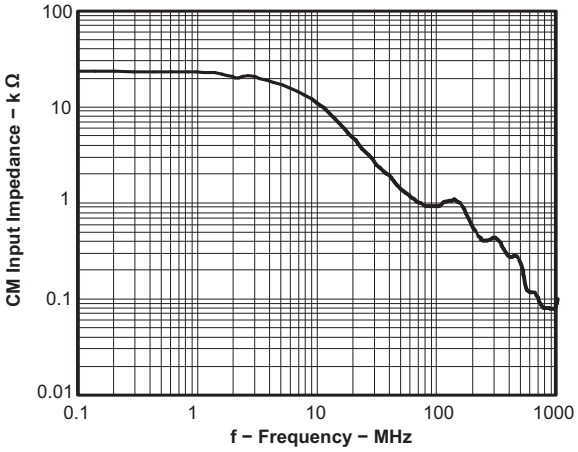

Figure 39.

CM SMALL SIGNAL FREQUENCY RESPONSE

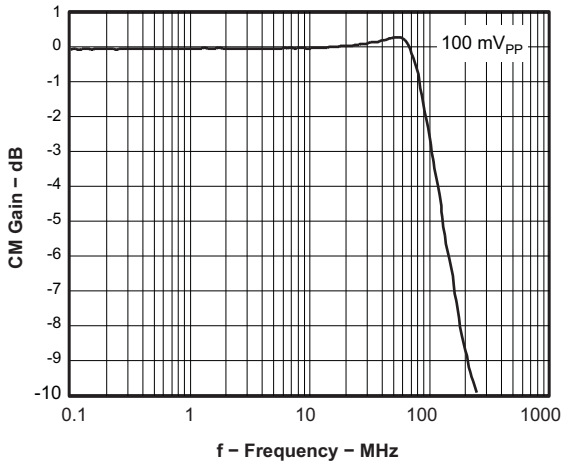

Figure 40.

CM INPUT BIAS CURRENT vs CM INPUT VOLTAGE

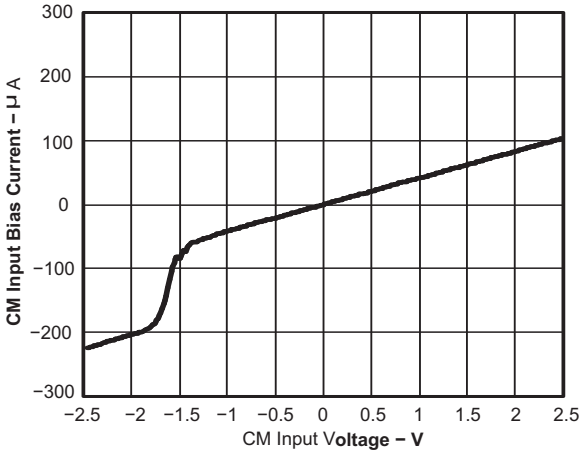

Figure 41.

DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs CM INPUT VOLTAGE

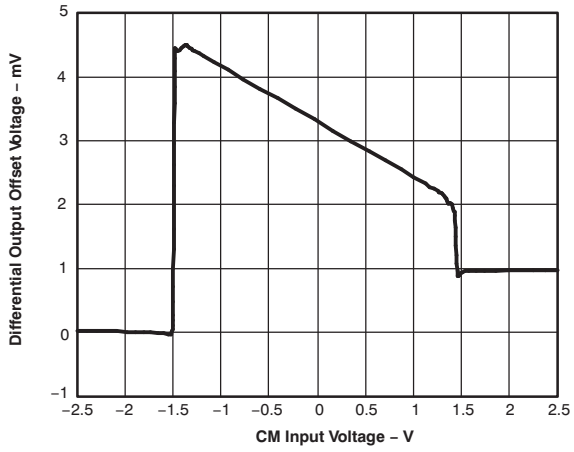

Figure 42.

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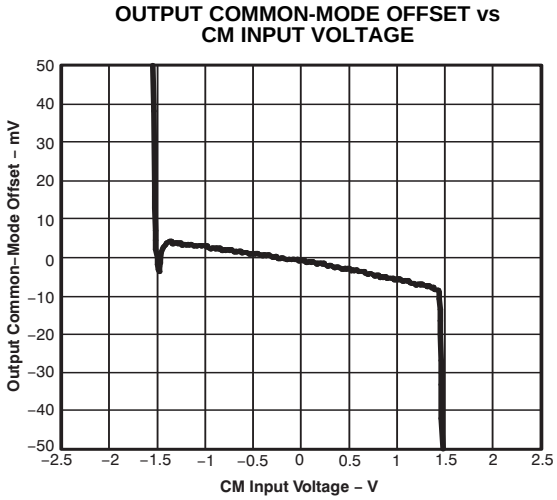

Figure 43.

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TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 3$ V

Test conditions unless otherwise noted: V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 Vpp, R_F = 349 Ω, R_L = 200 Ω Differential, G = 10 dB, Single-Ended Input, Input and Output Referenced to Midrail

Small-Signal Frequency Response			Figure 44
Large Signal Frequency Response			Figure 45
Harmonic Distortion	HD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 46
	HD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 47
	HD_2, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 48
	HD_3, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 49
	HD_2, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 50
	HD_3, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 51
Intermodulation Distortion	IMD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 52
	IMD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 53
	IMD_2, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 54
	IMD_3, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 55
	IMD_2, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 56
	IMD_3, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 57
Ouput Intercept Point	OIP_2	vs Frequency	Figure 58
	OIP_3	vs Frequency	Figure 59
0.1 dB Flatness			Figure 60
S-Parameters		vs Frequency	Figure 61
Transition Rate		vs Output Voltage	Figure 62
Transient Response			Figure 63
Settling Time			Figure 64
Output Voltage Swing		vs Load Resistance	Figure 65
Rejection Ratio		vs Frequency	Figure 66
Overdrive Recovery			Figure 67
Output Impedance		vs Frequency	Figure 68
Turn-Off Time			Figure 69
Turn-On Time			Figure 70
Ouput Balance Error		vs Frequency	Figure 71
Noise Figure		vs Frequency	Figure 72
CM Input Impedance		vs Frequency	Figure 73
Differential Output Offset Voltage		vs CM Input Voltage	Figure 74
Output Common-Mode Offset		vs CM Input Voltage	Figure 75

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SMALL-SIGNAL FREQUENCY RESPONSE

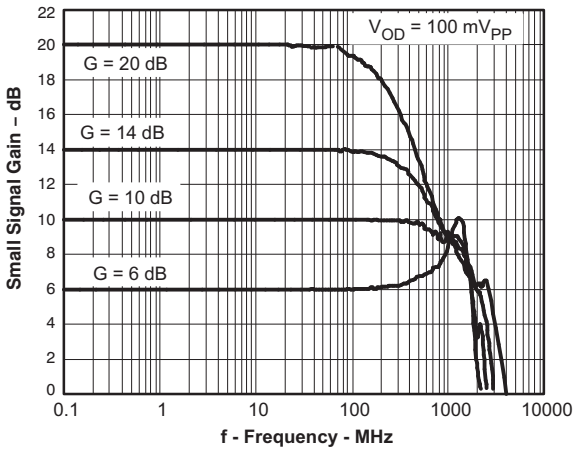

Figure 44.

LARGE-SIGNAL FREQUENCY RESPONSE

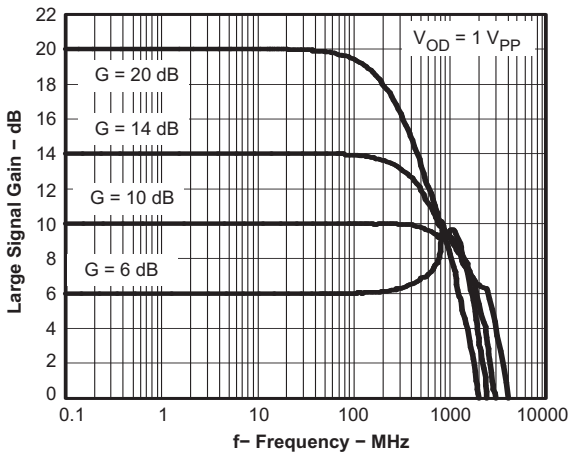

Figure 45.

HD2 vs FREQUENCY

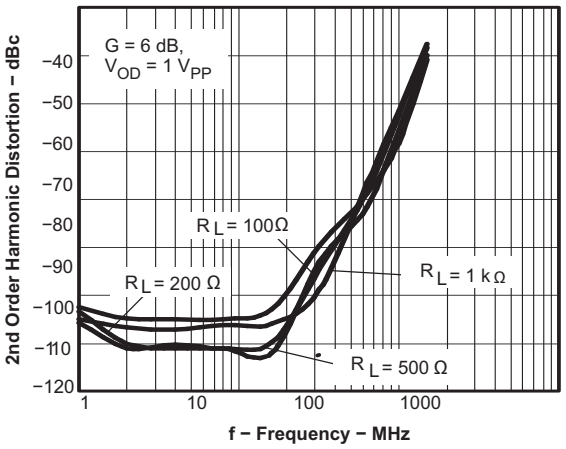

Figure 46.

HD3 vs FREQUENCY

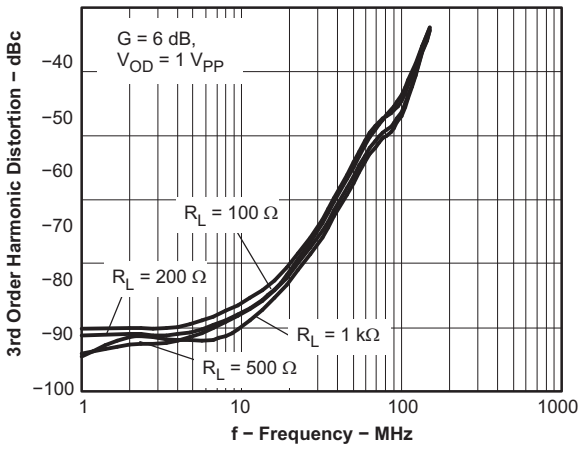

Figure 47.

HD2 vs FREQUENCY

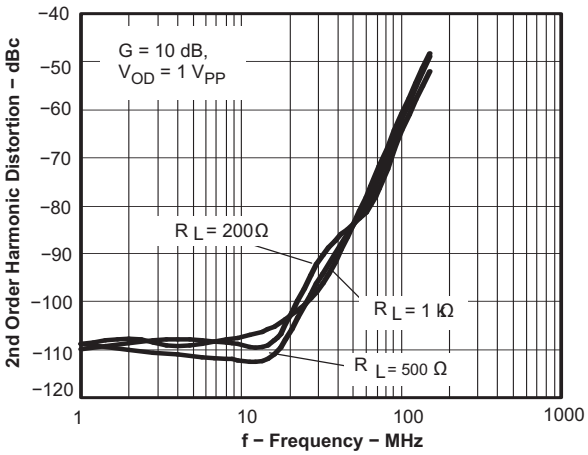

Figure 48.

HD3 vs FREQUENCY

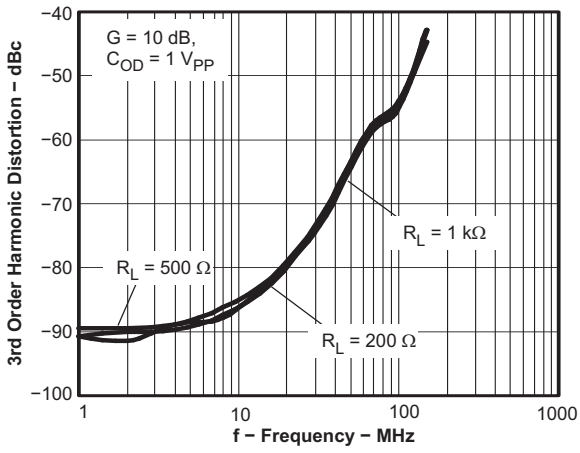

Figure 49.

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HD_2 vs FREQUENCY

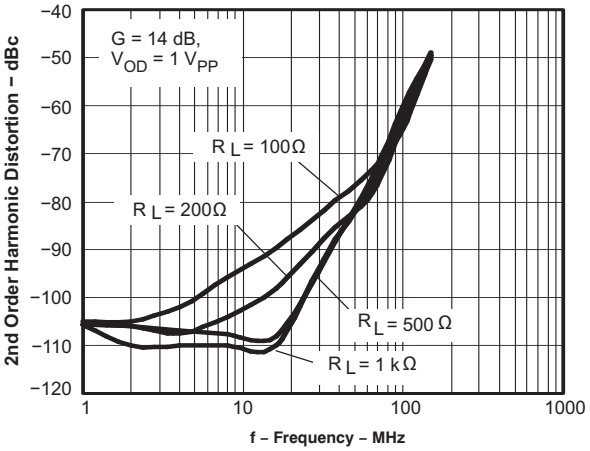

Figure 50.

HD_3 vs FREQUENCY

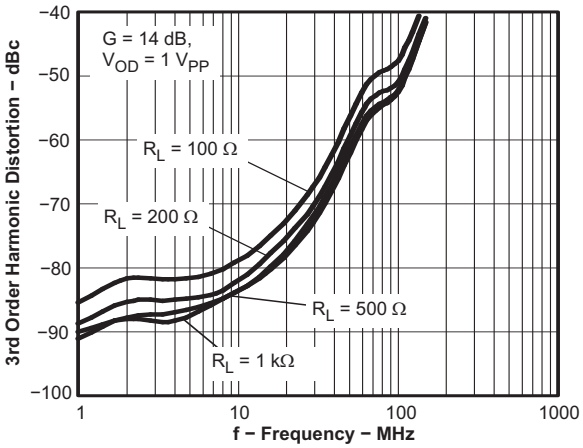

Figure 51.

IMD_2 vs FREQUENCY

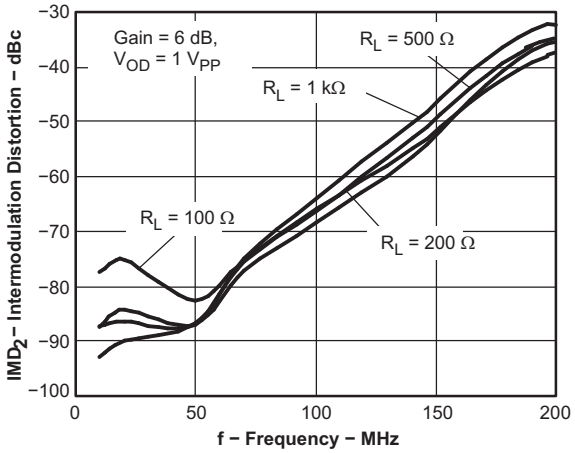

Figure 52.

IMD_3 vs FREQUENCY

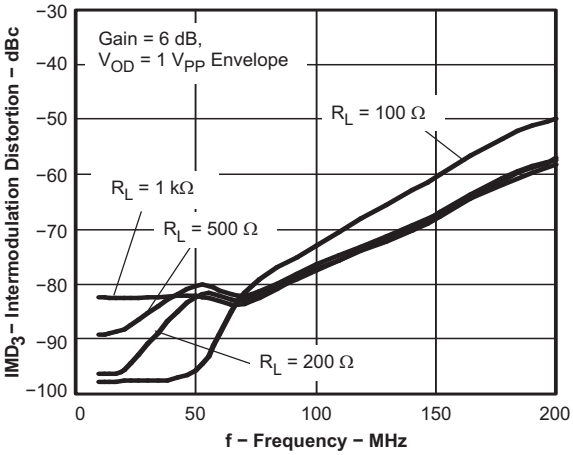

Figure 53.

IMD_2 vs FREQUENCY

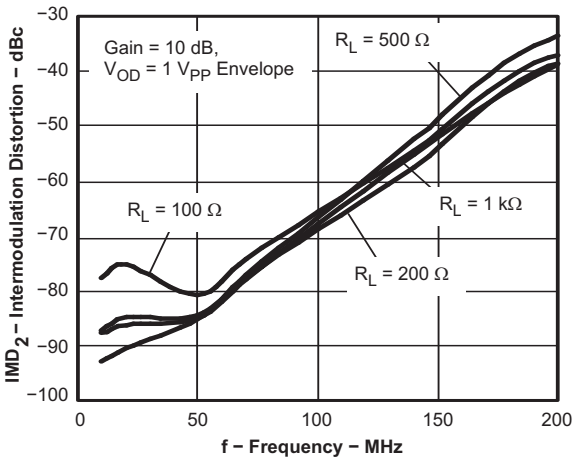

Figure 54.

IMD_3 vs FREQUENCY

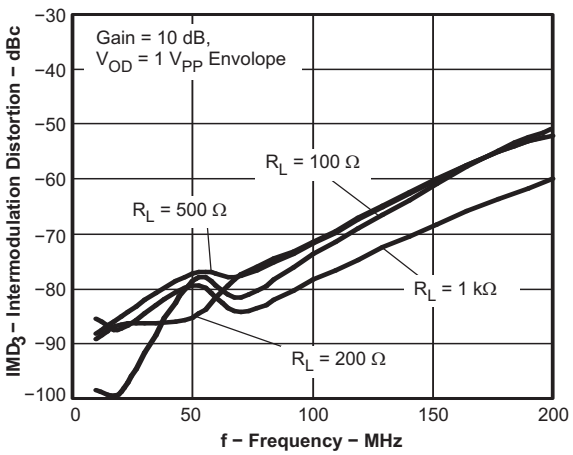

Figure 55.

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IMD_2 vs FREQUENCY

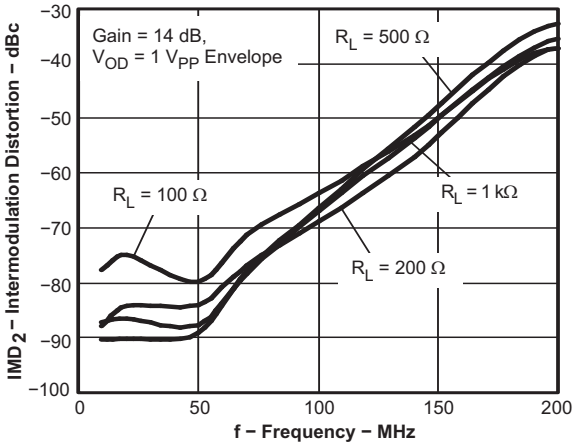

Figure 56.

IMD_3 vs FREQUENCY

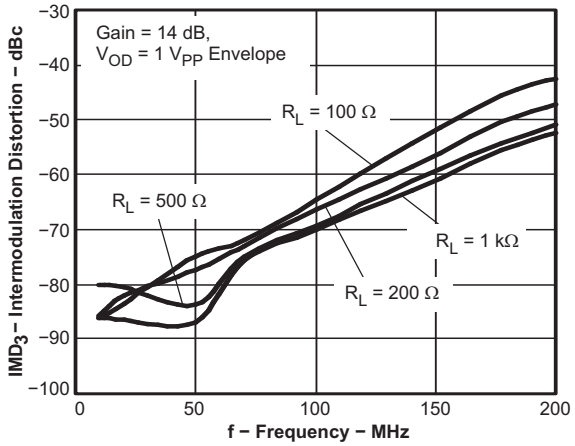

Figure 57.

OIP_2, dBm vs FREQUENCY

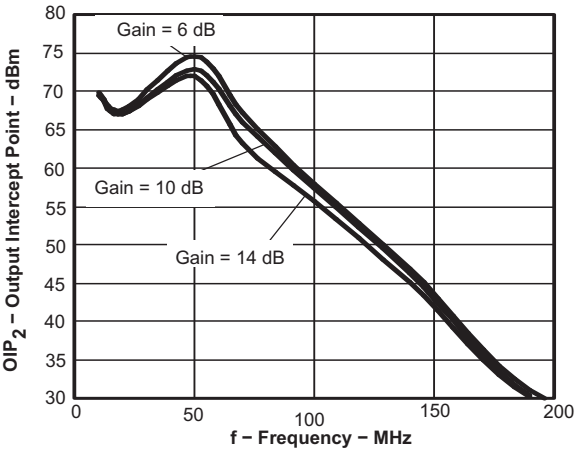

Figure 58.

OIP_3, dBm vs FREQUENCY

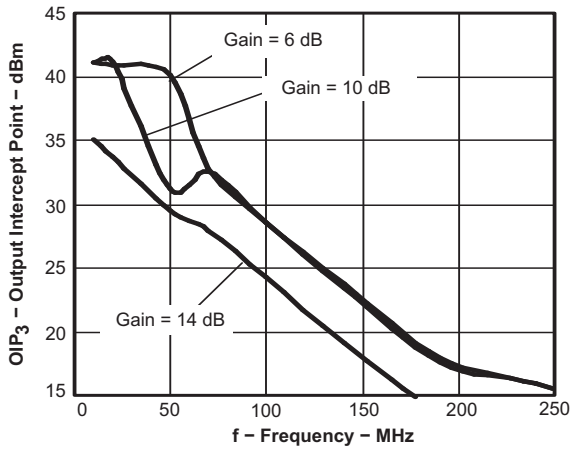

Figure 59.

0.1 dB FLATNESS

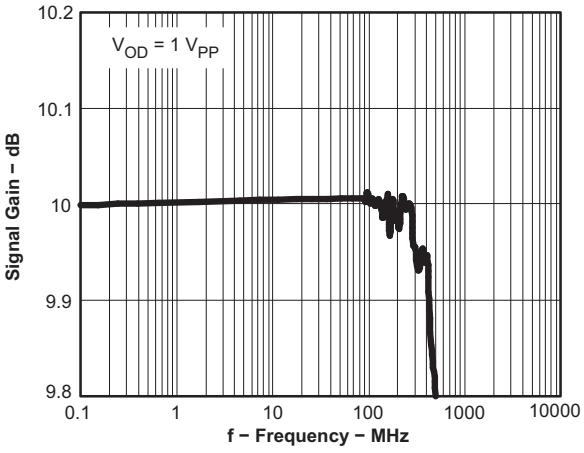

Figure 60.

S-PARAMETERS vs FREQUENCY

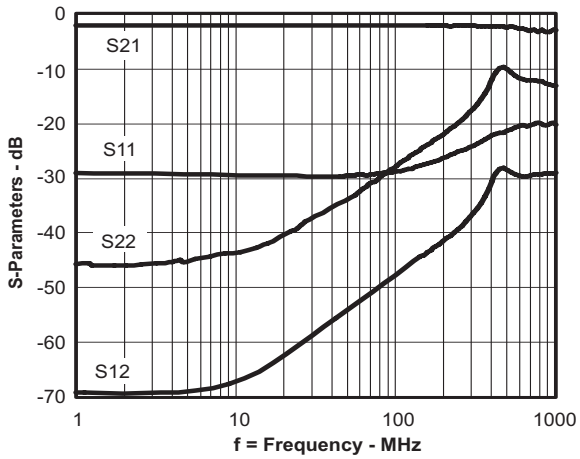

Figure 61.

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TRANSITION RATE vs OUTPUT VOLTAGE

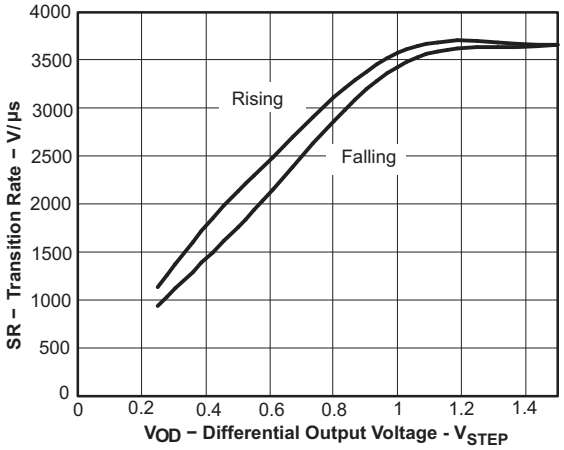

Figure 62.

TRANSIENT RESPONSE

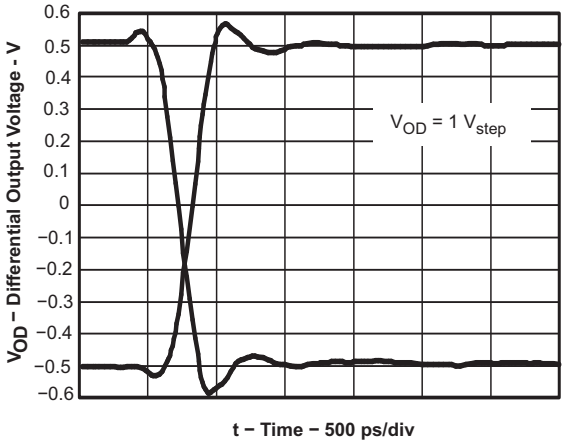

Figure 63.

SETTLING TIME

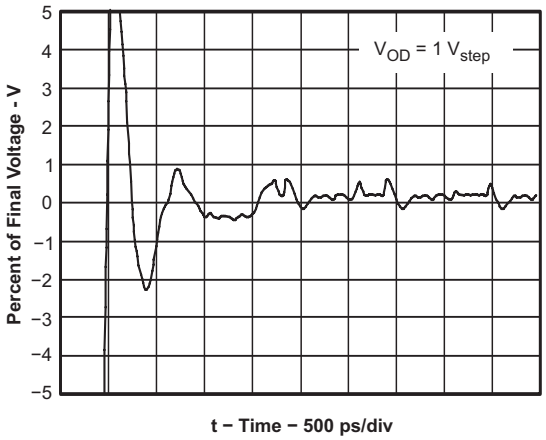

Figure 64.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

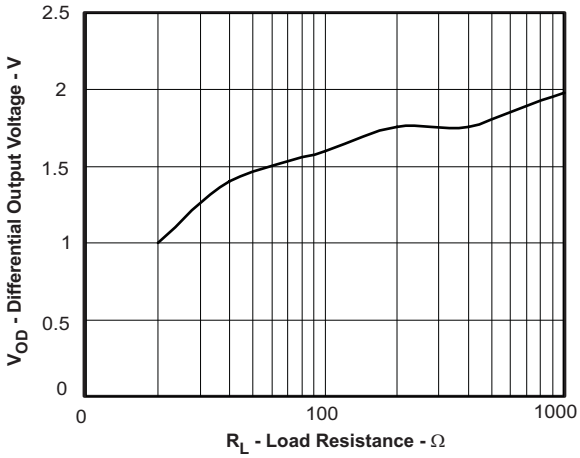

Figure 65.

REJECTION RATIO vs FREQUENCY

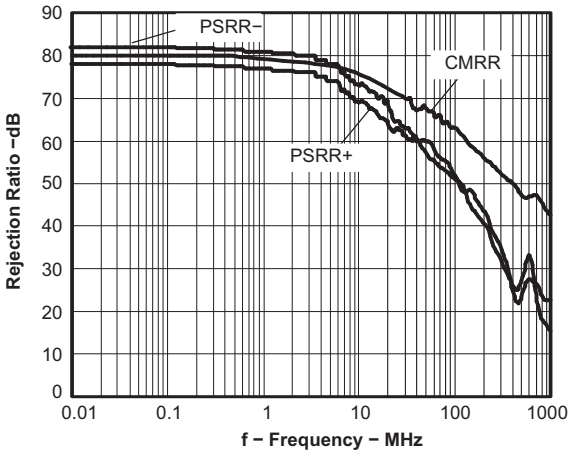

Figure 66.

OVERDRIVE RECOVERY

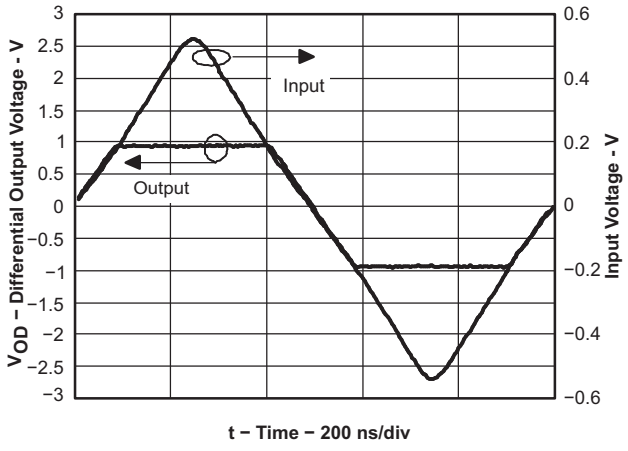

Figure 67.

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OUTPUT IMPEDANCE vs FREQUENCY

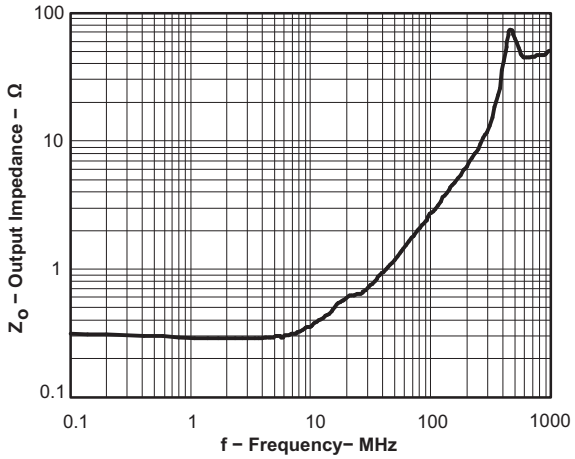

Figure 68.

TURN-OFF TIME

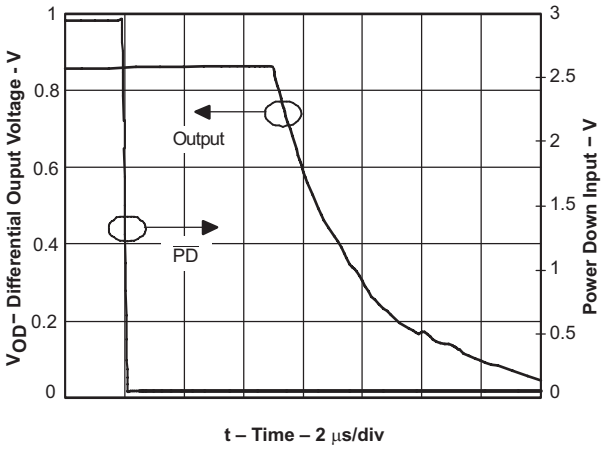

Figure 69.

TURN-ON TIME

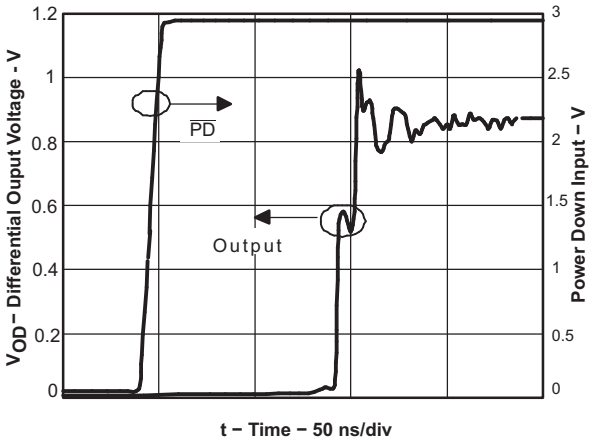

Figure 70.

OUTPUT BALANCE ERROR vs FREQUENCY

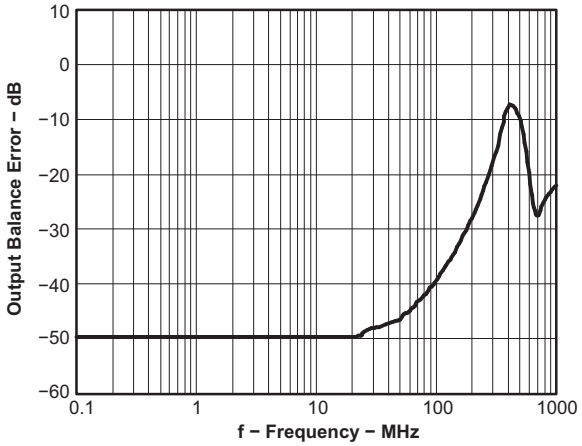

Figure 71.

NOISE FIGURE vs FREQUENCY

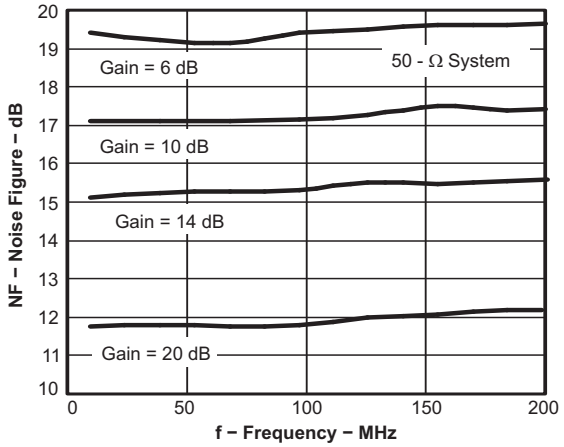

Figure 72.

CM INPUT IMPEDANCE vs FREQUENCY

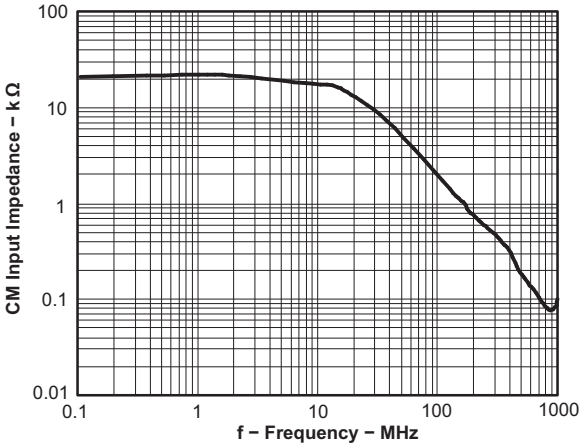

Figure 73.

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DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs CM INPUT VOLTAGE

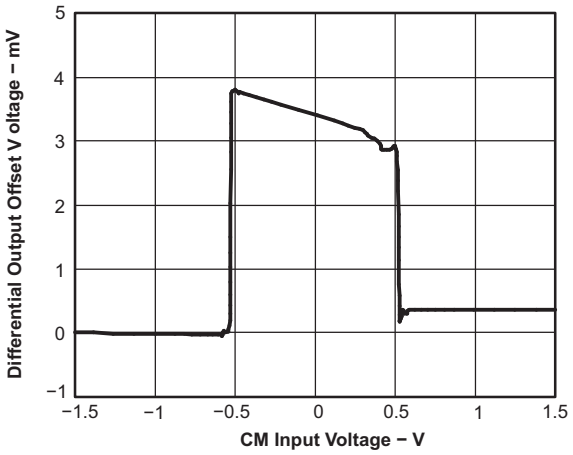

Figure 74.

OUTPUT COMMON-MODE OFFSET vs CM INPUT VOLTAGE

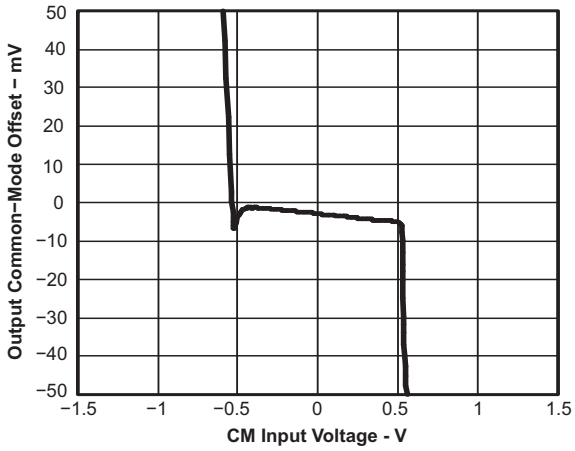

Figure 75.

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TEST CIRCUITS

The THS4509 is tested with the following test circuits built on the EVM. For simplicity, power supply decoupling is not shown – see layout in the applications section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50-Ω sources and a 0.22-µF capacitor and a 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in the applications section with no impact on performance.

Table 1. Gain Component Values

GAIN	R_F	R_G	R_{IT}
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

Note the gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-ΩΩ input termination.

Table 2. Load Component Values

R_L	R_O	R_{OT}	Atten.
100 Ω	25 Ω	open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 77, the signal will see slightly more loss, and these numbers will be approximate.

Frequency Response

The circuit shown in Figure 76 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

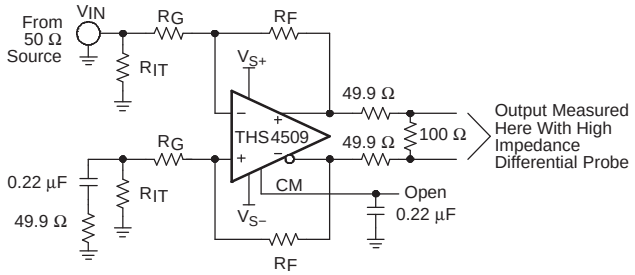

Figure 76. Frequency Response Test Circuit

Distortion and 1dB Compression

The circuit shown in Figure 77 is used to measure harmonic distortion, intermodulation distortion, and 1-db compression point of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1MHz.

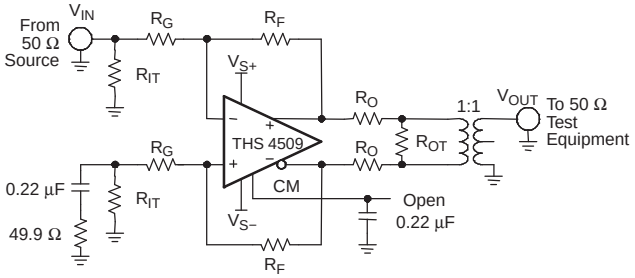

Figure 77. Distortion Test Circuit

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The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or 100-Ω termination as shown in Table 2. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to refer to the amplifier output.

S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in Figure 78 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open and the drop across the 49.9 Ω resistor is used to calculate the impedance seen looking into the amplifier's output.

Because S_{21} is measured single-ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier's output as a differential signal.

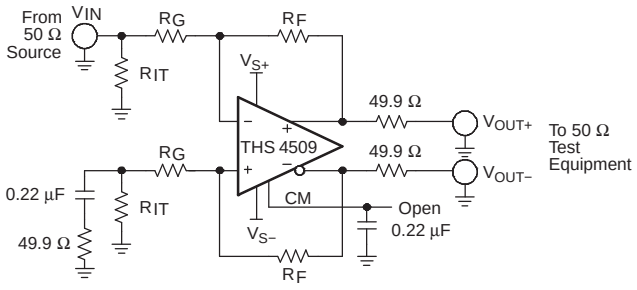

Figure 78. S-Parameter, SR, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turn-on/off Test Circuit

CM Input

The circuit shown in Figure 79 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at V_{OUT+} or $V_{OUT–}$ with the input injected at V_{IN}, R_{CM} = 0 Ω and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

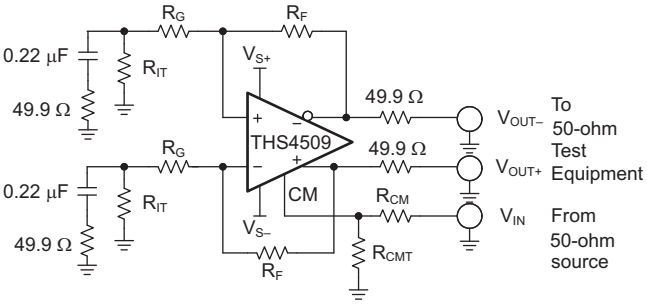

Figure 79. CM Input Test Circuit

CMRR and PSRR

The circuit shown in Figure 80 is used to measure the CMRR and PSRR of V_{S+} and $V_{S–}$. The input is switched appropriately to match the test being performed.

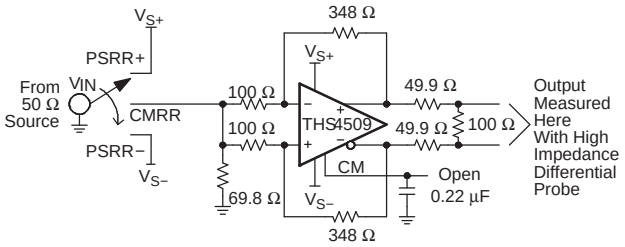

Figure 80. CMRR and PSRR Test Circuit

APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4509. For simplicity, power supply decoupling capacitors are not shown in these diagrams. Please see the SubSec2 0.1 section for recommendations. For more detail on the use and operation of fully differential op amps refer to application report *Fully-Differential Amplifiers* (SLOA054) .

Differential Input to Differential Output Amplifier

The THS4509 is a fully differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 81 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

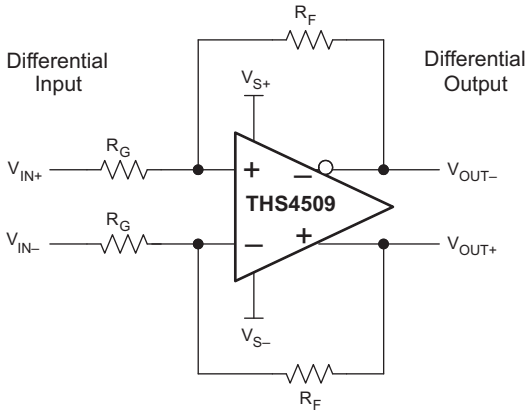

Figure 81. Differential Input to Differential Ouput Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

Single-Ended Input to Differential Output Amplifier

The THS4509 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 82 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

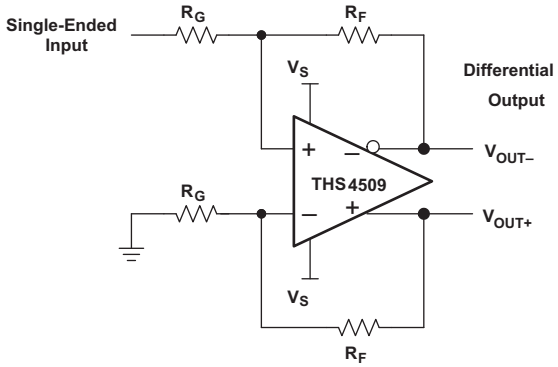

Figure 82. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-model voltage of a fully differential op amp is the voltage at the '+' and '–' input pins of the op amp.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4mV differential offset voltage. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 83 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which is required for best

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performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where V_{CM} is the voltage applied to the CM pin.

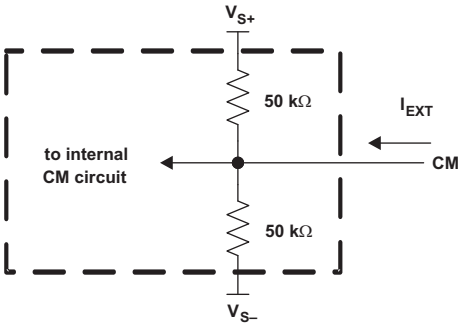

Figure 83. CM Input Circuit

Single-Supply Operation (3V to 5V)

To facilitate testing with common lab equipment, the THS4509 EVM allows split-supply operation, and the characterization data presented in this data sheet was taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 84, Figure 85, and Figure 86 show DC and AC-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to mid-supply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 84, the source is referenced to the same voltage as the CM pin (V_{CM}). V_{CM} is set by the internal circuit to mid-supply. R_T along with the input impedance of the amplifier circuit provides input termination, which is also referenced to V_{CM}.

Note R_S and R_T are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value R_G+ $R_S||R_T$ on this input. This is also true of the circuits shown in Figure 85 and Figure 86.

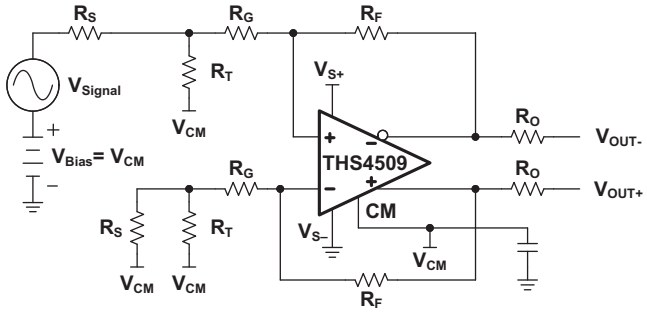

Figure 84. THS4509 DC Coupled Single-Supply with Input Biased to V_{CM}

In Figure 85 the source is referenced to ground and so is the input termination resistor. R_{PU} is added to the circuit to avoid violating the V_{ICR} of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{(V_{IC} - V_{S+})}{V_{CM}\left(\frac{1}{R_F}\right) - V_{IC}\left(\frac{1}{R_{IN}} + \frac{1}{R_F}\right)} \quad (3)$$

V_{IC} is the desire input common-mode voltage, V_{CM} = CM, and R_{IN} = R_G+ $R_S||R_T$. To set to mid-supply, make the value of R_{PU} = R_G+ $R_S||R_T$.

Table 3 is a modification of Table 1 to add the proper values with R_{PU} assuming a 50 Ω source impedance and setting the input and output common-mode voltage to mid-supply.

There are two drawbacks to this configuration. One is it requires additional current from the power supply. Using the values shown for a gain of 10 dB requires 37 mA more current with 5-V supply, and 22 mA more current with 3-V supply.

The other drawback is this configuration also increases the noise gain of the circuit. In the 10 dB gain case, noise gain increases by a factor of 1.5.

Table 3. RPU Values for Various Gains

Gain	R_F	R_G	R_{IT}	R_{PU}
6 dB	348 Ω	169 Ω	64.9 Ω	200 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	133 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	97.6 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	80.6 Ω

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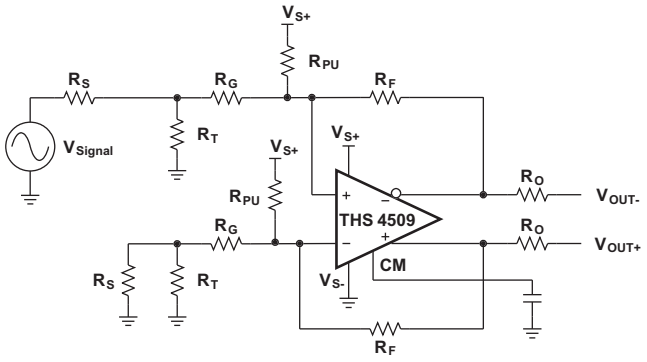

Figure 85. THS4509 DC Coupled Single-Supply with R_{PU} Used to Set V_{IC}

Figure 86 shows AC coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to mid-supply.

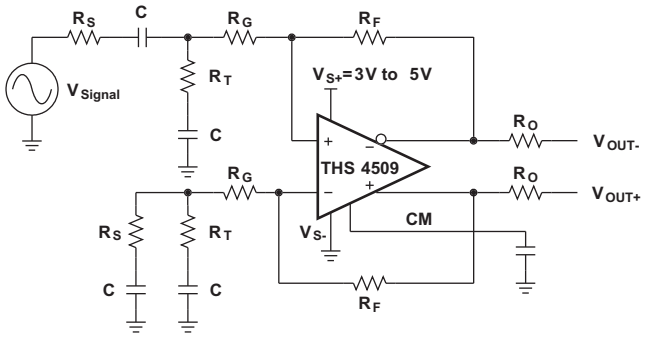

Figure 86. THS4509 AC Coupled Single-Supply

THS4509 + ADS5500 Combined Performance

The THS4509 is designed to be a high performance drive amplifier for high performance data converters like the ADS5500 14-bit 125-MSPS ADC. Figure 87 shows a circuit combining the two devices, and Figure 88 shows the combined SNR and SFDR performance versus frequency with –1 dBFS input signal level sampling at 125 MSPS. The THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500. The 100-Ω resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5500 inputs along with the input capacitance of the ADS5500 limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8-Ω resistor and 0.22-µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. Refer to Table 3 for component values to set proper 50-Ω termination for other common gains. A split power supply of +4V and -1V is used to set the input and output common-mode voltages to approximately mid-supply while setting the input common-mode of the ADS5500 to the recommended +1.55V. This maintains maximum headroom on the internal transistors of the THS4509 to insure optimum performance.

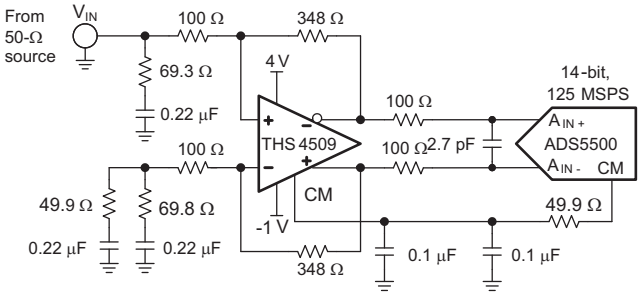

Figure 87. THS4509 + ADS5500 Circuit

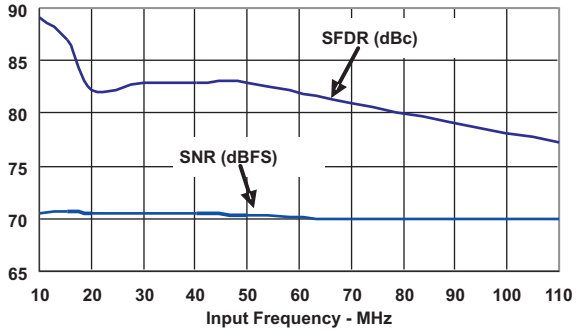

Figure 88. THS4509 + ADS5500 SFDR and SNR Performance versus Frequency

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Figure 89 shows the 2-tone FFT of the THS4509 + ADS5500 circuit with 65 MHz and 70 MHz input frequencies. The SFDR is 90 dBc.

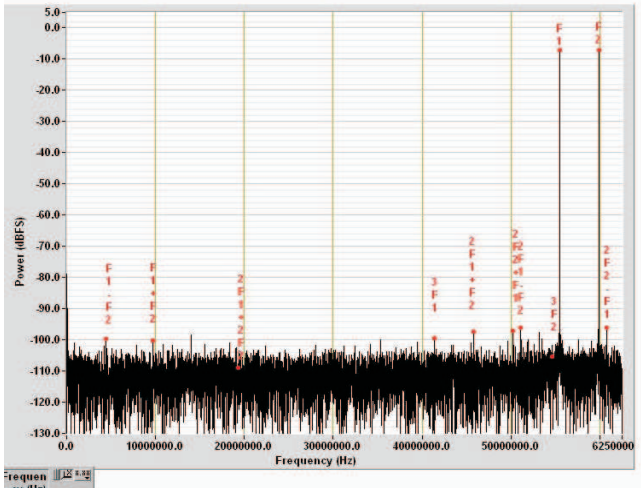

Figure 89. THS4509 + ADS5500 2-Tone FFT with 65 MHz and 70 MHz Input

THS4509 + ADS5424 Combined Performance

Figure 90 shows the THS4509 driving the ADS5424 ADC, and Figure 91 shows their combined SNR and SFDR performance versus frequency with –1 dBFS input signal level and sampling at 80 MSPS.

As before, the THS4509 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4509 + ADS5500 circuit.

The 225-Ω resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100MHz (-3dB).

Since the ADS5424s recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with V_{S+} = 5 V and V_{S-} = 0 V (ground).

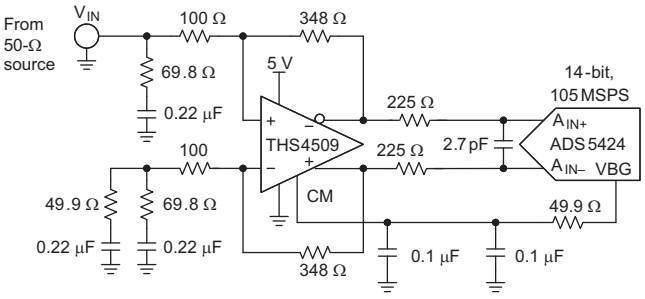

Figure 90. THS4509 + ADS5424 Circuit

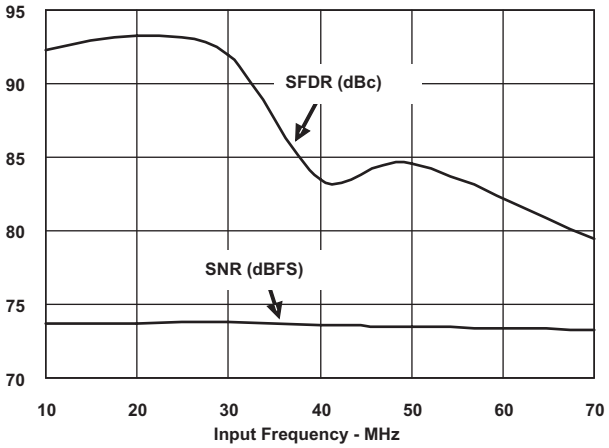

Figure 91. THS4509 + ADS5424 SFDR and SNR Performance vs Frequency

Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the opamp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-µF and two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1-µF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4509 recommended PCB footprint is shown in Figure 92.

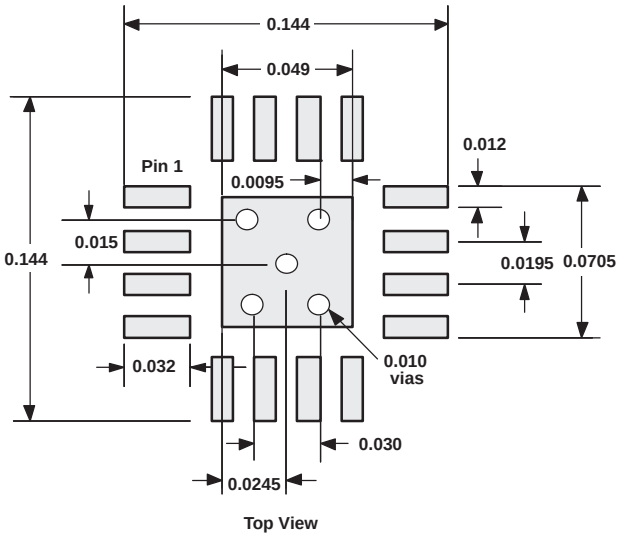

Figure 92. QFN Etch and Via Pattern

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THS4509 EVM

Figure 93 is the THS4509 EVAL1 EVM schematic, layers 1 through 4 of the PCB are shown Figure 94, and Table 4 is the bill of material for the EVM as supplied from TI.

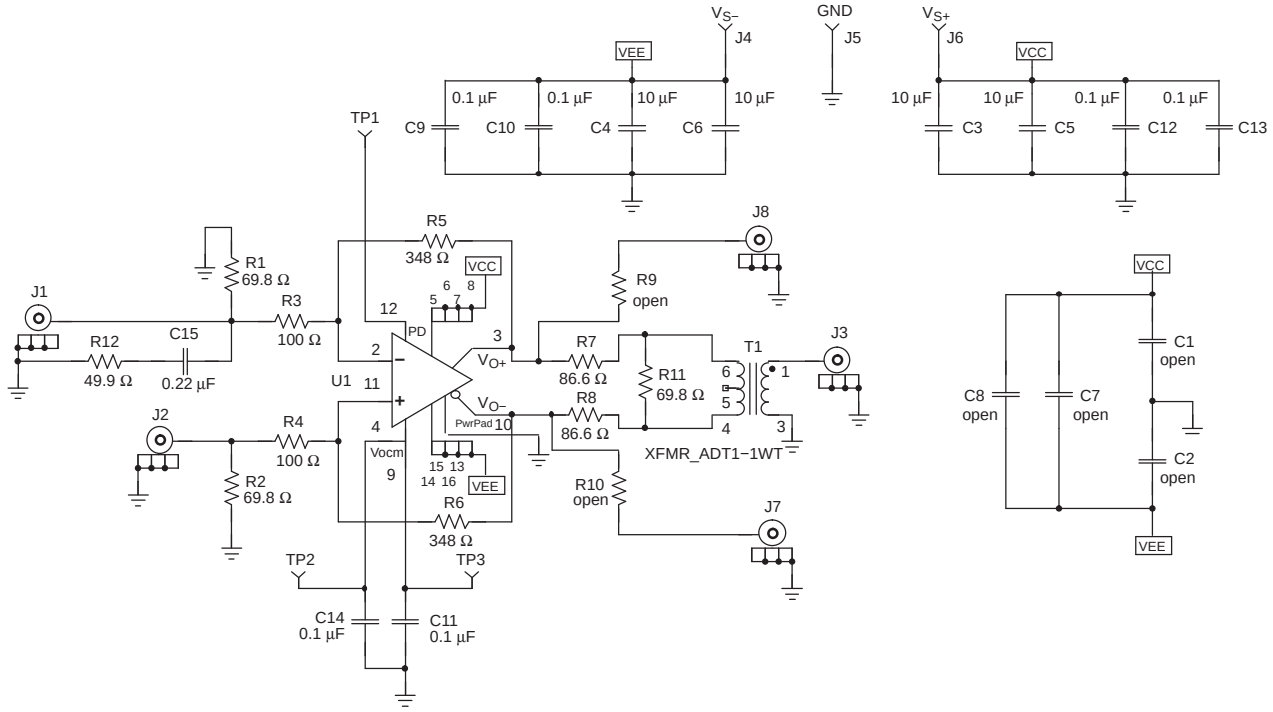

Figure 93. THS4509 EVAL1 EVM Schematic

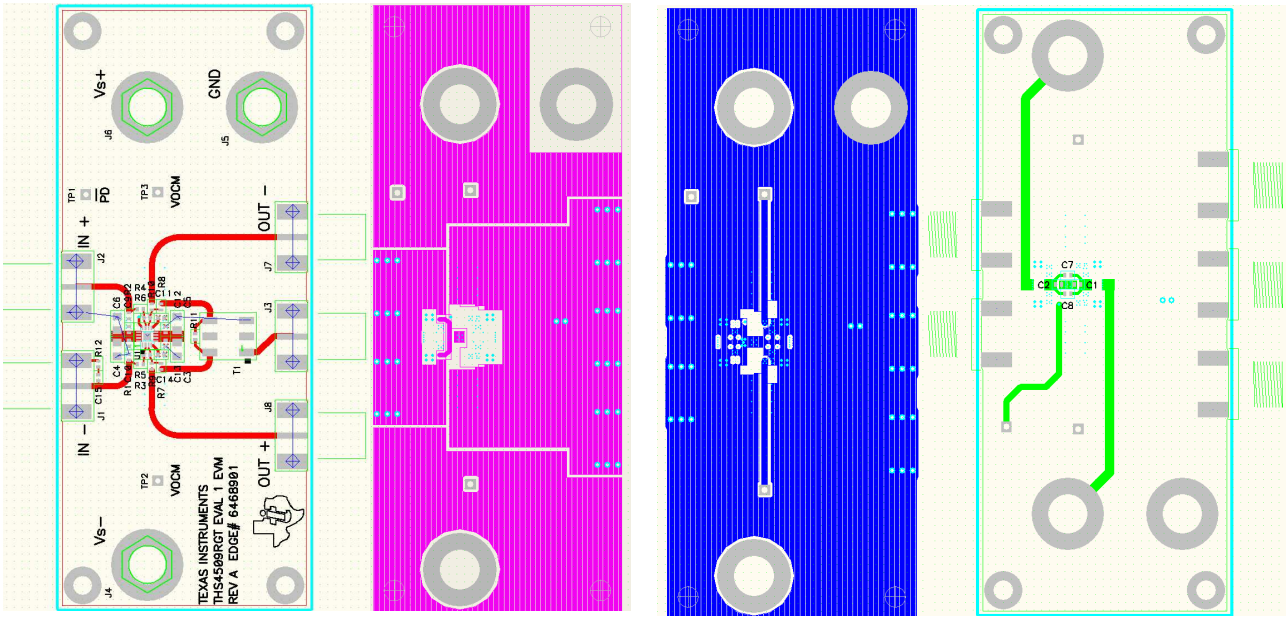

Figure 94. THS4509 EVAL1 EVM Layer 1 through 4

Table 4. THS4509 EVAL1 EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER
1	CAP, 10.0 µF, Ceramic, X5R, 6.3V	0805	C3, C4, C5, C6	4	(AVX) 08056D106KAT2A
2	CAP, 0.1 µF, Ceramic, X5R, 10V	0402	C9, C10, C11, C12, C13, C14	6	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 µF, Ceramic, X5R, 6.3V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8	4	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
8	Resistor, 69.8 Ω, 1/16W, 1%	0402	R1, R2, R11	3	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 100 Ω, 1/16W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP1000F
11	Resistor, 348 Ω, 1/16W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
13	Jack, banana receptance, 0.25" diameter hole		J4, J5, J6	3	(HH SMITH) 101
14	OPEN		J1, J7, J8	3	
15	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
16	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
17	IC, THS4509		U1	1	(TI) THS4509RGT
18	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
19	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
20	Printed circuit board			1	(TI) EDGE# 6468901

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input and output voltage ranges as specified in the table provided below.

Input Range, V_{S+} to V_{S-}	**3.0 V to 6.0 V**
Input Range, V_I	3.0 V to 6.0 V NOT TO EXCEED V_{S+} or V_{S-}
Output Range, V_O	3.0 V to 6.0 V NOT TO EXCEED V_{S+} or V_{S-}

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS4509RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4509RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4509RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4509RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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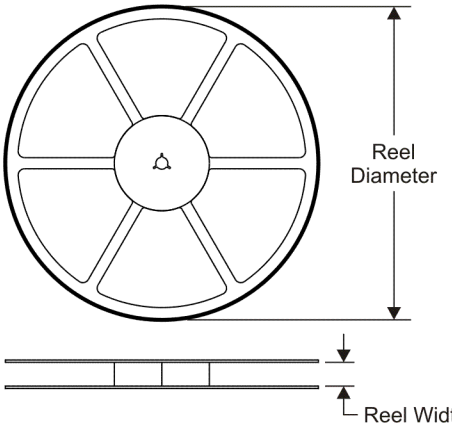
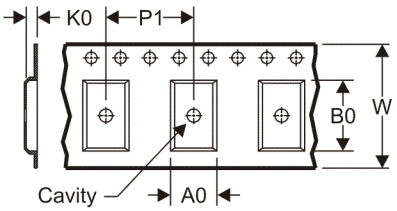
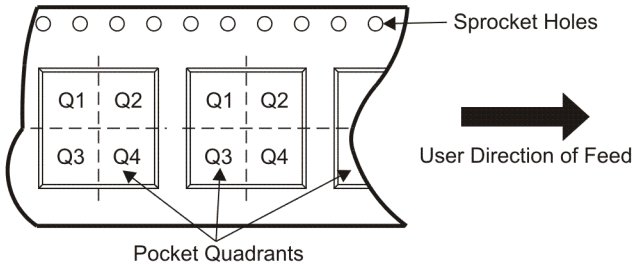


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

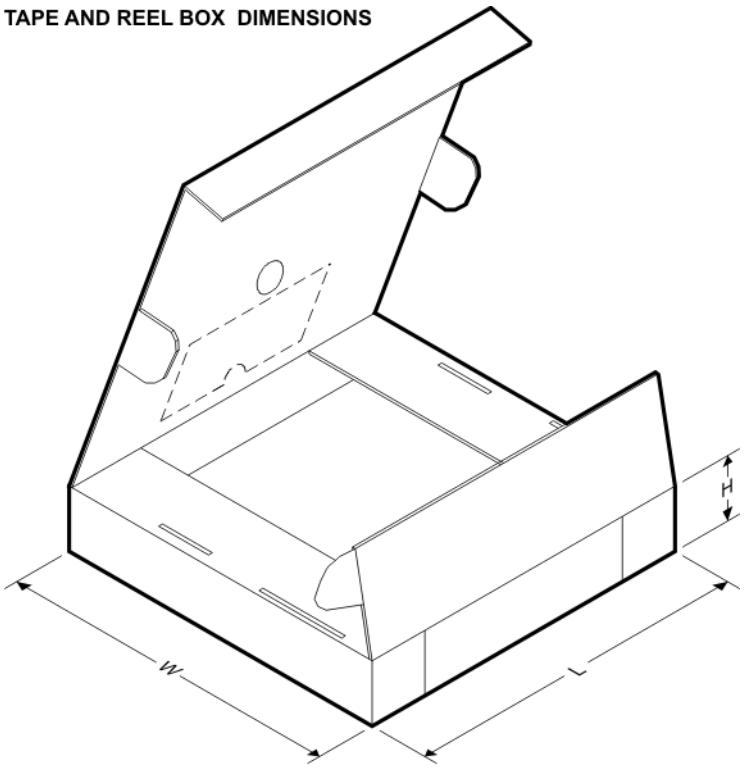
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4509RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4509RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

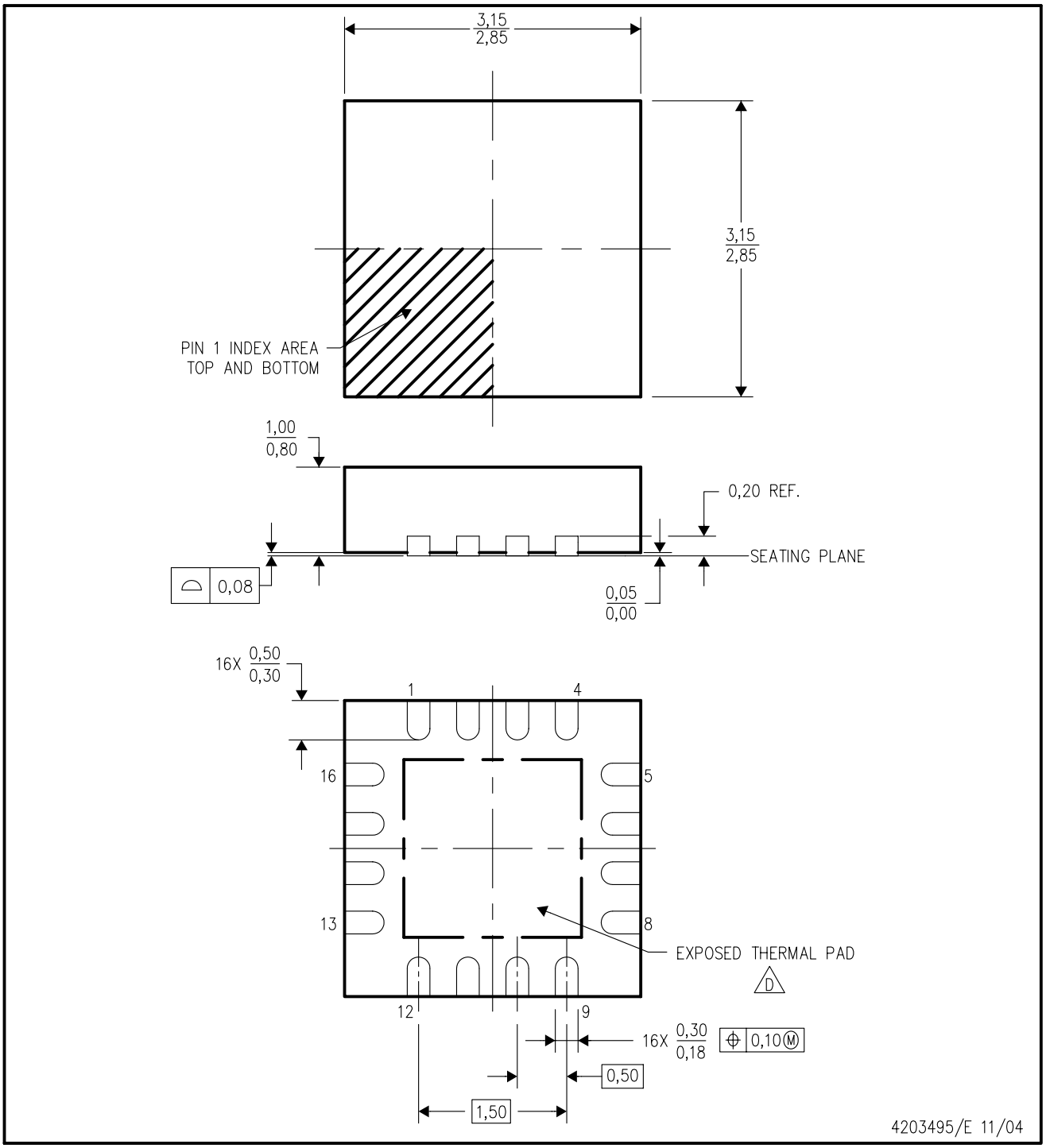
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4509RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
THS4509RGTT	QFN	RGT	16	250	190.5	212.7	31.8

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

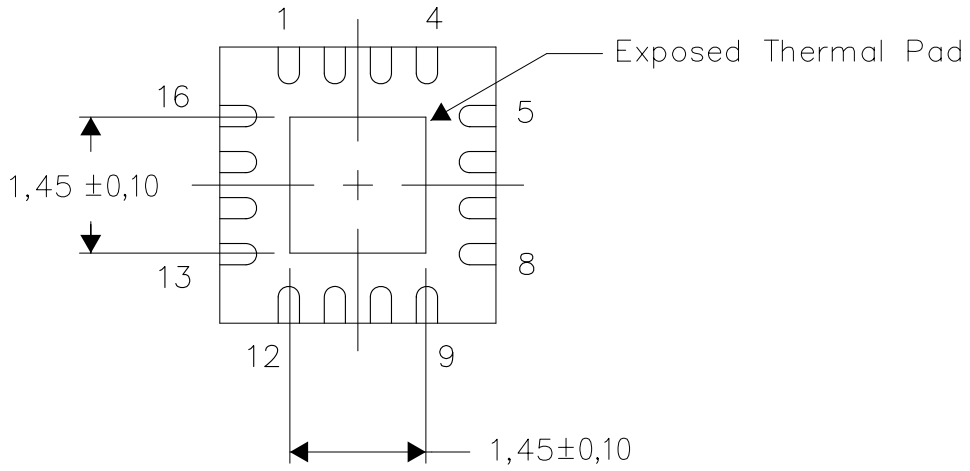
RGT (S–PVQFN–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

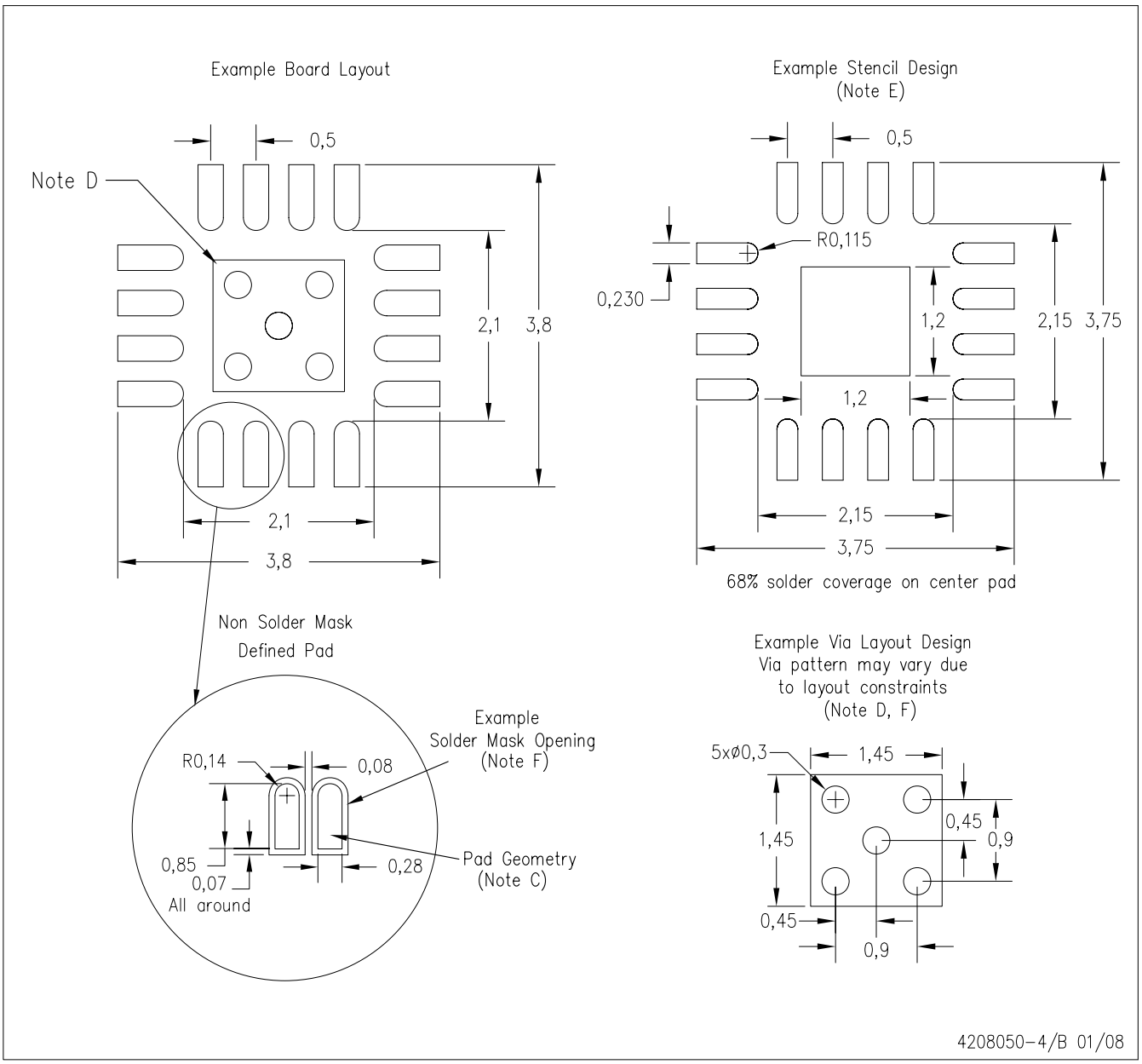


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S–PQFP–N16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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