M74LS165AP

8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

DESCRIPTION

The M74LS165AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input – serial output shift register function.

FEATURES

- Parallel-to-serial data conversion
- Complementary output (Q_7 and $\overline{Q_7}$)
- Direct overriding load (data) input
- Clock inhibit input
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

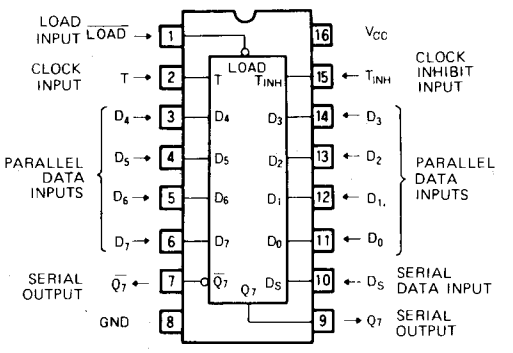
This device is configured from eight R-S-T flip-flop circuits and is designed to accept serial data input through D_S, or parallel data input through D_0 ~ D_7.

When D_S is used as the input, a clock pulse is applied to clock input T when load input $\overline{LOAD}$ is high-level and the clock inhibit input T_{INH} is low-level.

Shift operations are initiated upon T transiting from low to high, and the data present at D_S appears as an output pulse from Q_7, $\overline{Q_7}$ of the 8th flip-flop circuit. The output at $\overline{Q_7}$ is always an inverted value of that present at Q_7.

When D_0 ~ D_7 is used as the input, $\overline{LOAD}$ is active-low. Since D_0 ~ D_7 are entered at the direct-set, direct-reset input of each flip-flop, read is executed regardless of the status of other inputs.

PIN CONFIGURATION (TOP VIEW)

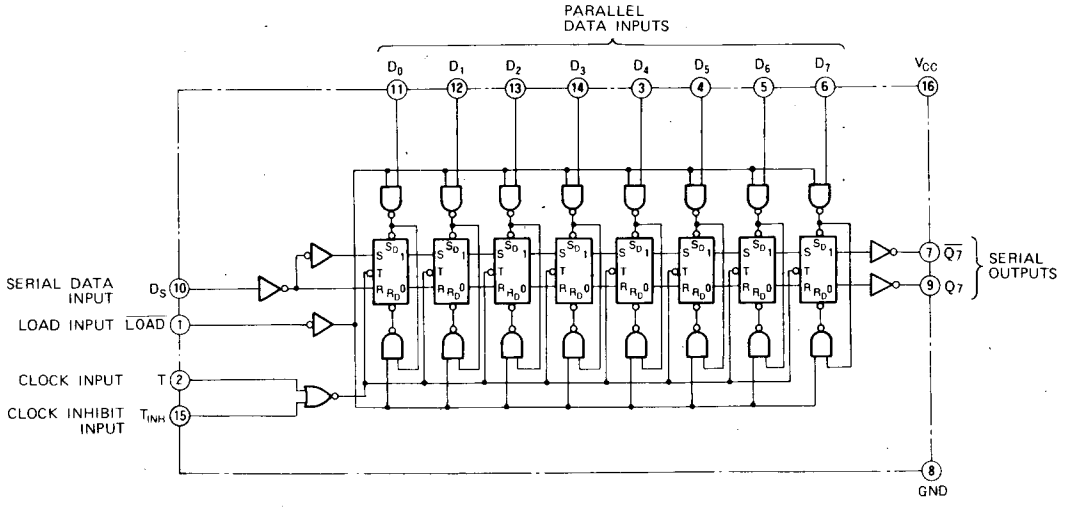


Outline 16P4

Care should be exercised to prevent the recording of erroneous data caused by a change in the value of D_0 ~ D_7 when $\overline{LOAD}$ switches from low to high-value. Also, when T_{INH} is high, a shift operation will not be effected with clock pulse input. When T is low-level, and T_{INH} transits from low to high, a 1-bit shift operation will be executed.

M74LS165AP is an enhanced-performance version of M74LS165P having modified switching characteristics.

BLOCK DIAGRAM



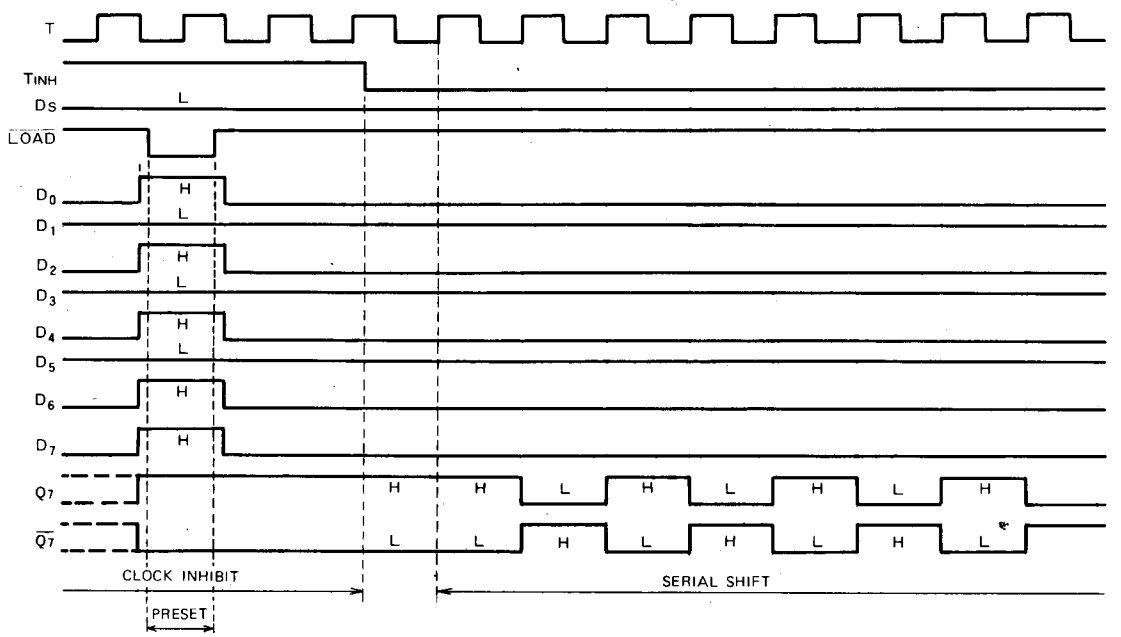
8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

Inputs					Internal Outputs		Output
$\overline{LOAD}$	T_{INH}	T	D_S	$D_0 \cdots D_7$	Q_0	Q_1	Q_7
L	X	X	X	$D_0 \cdots D_7$	D_0	D_1	D_7
H	L	L	X	X	Q_0^0	Q_1^0	Q_7^0
H	L	↑	H	X	H	Q_0^0	Q_6^0
H	L	↑	L	X	L	Q_0^0	Q_6^0
H	H	X	X	X	Q_0^0	Q_1^0	Q_7^0

Note 1. X : Irrelevant
↑ : Transition from low to high (positive edge trigger)
Q^0 : Status of output before ↑ of T

TIMING DIAGRAM



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8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−400	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 3)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 4)			18	30	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

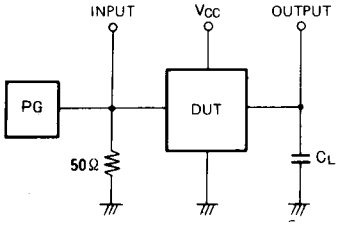
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the $\overline{LOAD}$ input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=15pF (Note 4)	25	38		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{LOAD}$ to outputs Q_7 and $\overline{Q_7}$			17	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_7 and $\overline{Q_7}$			14	25	ns
t_{PHL}				13	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_7 to output Q_7			9	25	ns
t_{PHL}				20	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_7 to output $\overline{Q_7}$			16	30	ns
t_{PHL}				12	25	ns

Note 4. Measurement Circuit

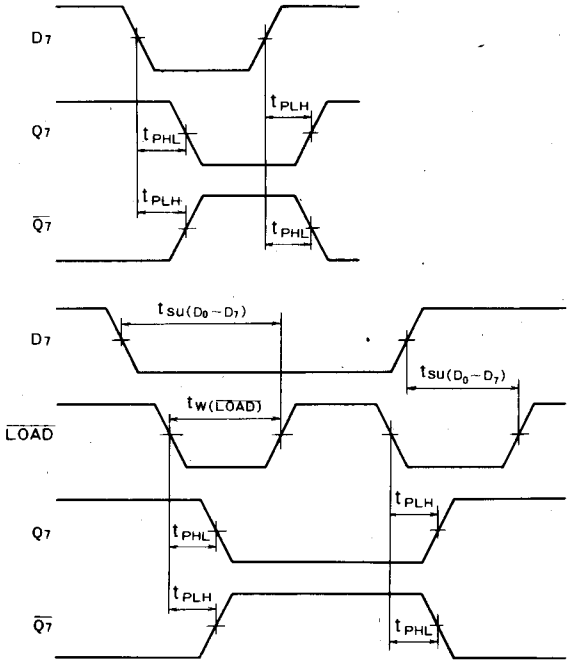


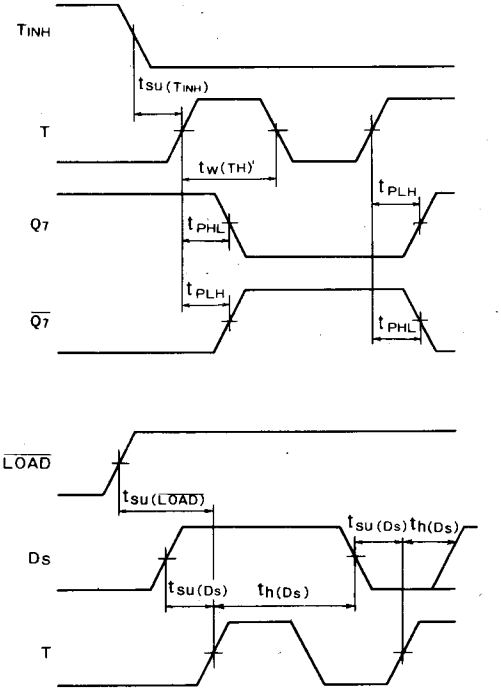
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_o = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock pulse width		25	13		ns
$t_{w(\overline{LOAD})}$	$\overline{LOAD}$ low-level pulse width		15	12		ns
$t_{su(T_{INH})}$	Setup time T_{INH} to T		30	13		ns
$t_{su(D_0 \sim D_7)}$	Setup time $D_0 \sim D_7$ to $\overline{LOAD}$		10	9		ns
$t_{su(D_S)}$	Setup time D_S to T		20	8		ns
$t_{su(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T		45	0		ns
t_h	Hold time		0	0		ns

TIMING DIAGRAM (Reference level = 1.3V)





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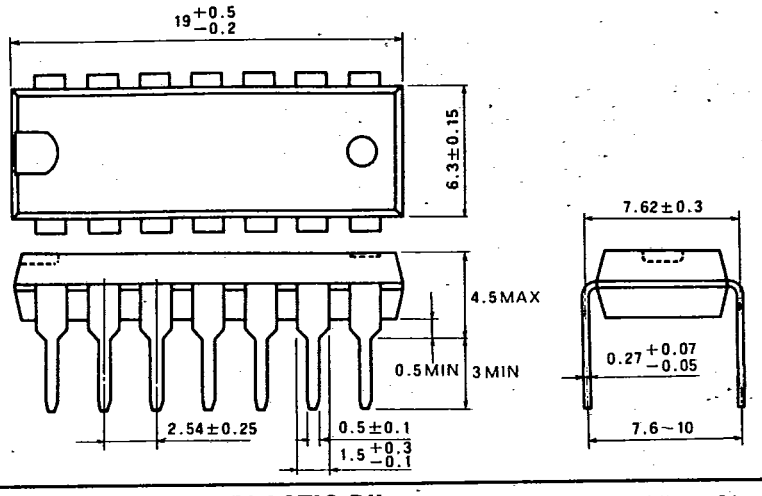
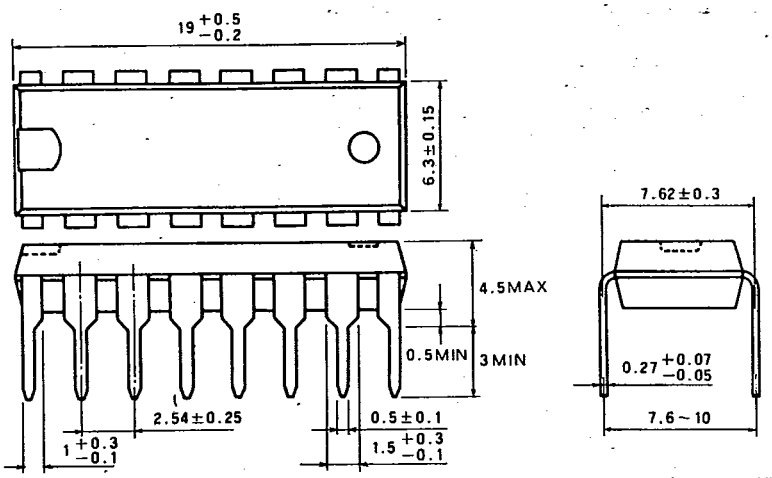
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm