锦州市圣合科技电子有限责任公司
Jinzhou Shenghe Power Electronic Co.,Ltd.
圣 合

KP 1400A-2000~2600V

Phase Control Thyristor

Key Parameters

V_{DRM}	2000~2600	V
$I_{T(AV)}$	1400	A
I_{TSM}	24.0	kA
V_{TO}	0.89	V
r_T	0.27	mΩ

Voltage Ratings

Device Type	V_{DRM}/V_{RRM}(V)	Test Conditions
KP 1400-20	2000	T_{vj} = 125 °C
KP 1400-22	2200	I_{DRM} = 150 mA
KP 1400-24	2400	I_{RRM} = 150 mA
KP 1400-26	2600	
		$V_{DM}=V_{DRM}$, $V_{RM}=V_{RRM}$
		t_p = 10 ms
		$V_{DSM}=V_{DRM}$
		$V_{RSM}=V_{RRM}+100$

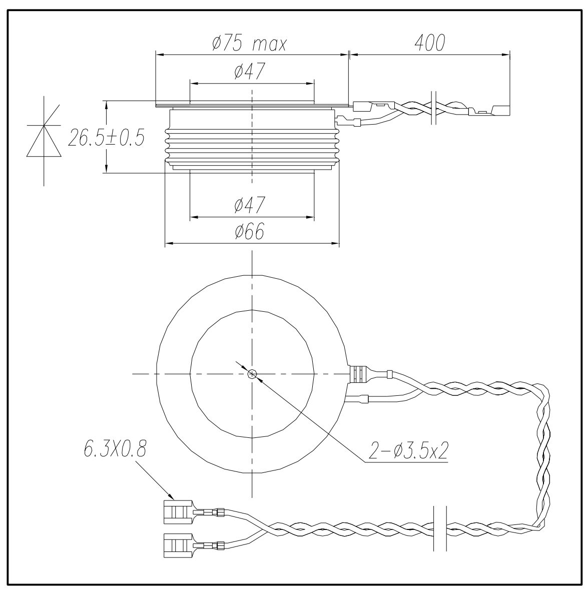
Applications

- ●Traction drive
- ●Motor drive
- ●Industry converter

Features

- ●Double-side cooling
- ●High power capability
- ●Low loss

Outline



Thermal & Mechanical Data

Symb.	Parameter	Min	Type	Max	Unit
R_{thjc}	Thermal Resistance Junction to Case	-	-	0.02	K / W
R_{thcs}	Thermal Resistance Case ro Heatsink	-	-	0.005	K / W
T_{vj}	Junction Temperature	-40	-	125	°C
T_{stg}	Storage Temperature	-40	-	140	°C
F	Mounting Force	-	22	-	kN
m	Weight	-	0.47	-	kg

Current Ratings

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
$I_{T(AV)}$	Mean On-State Current	Half Sine Wave, T_C=70 °C	-	-	1400	A
$I_{T(RMS)}$	RMS On-State Current	T_C =70 °C	-	-	2198	A
I_{TSM}	Surge (non-repetitive) On-State Current	10ms, Half Sine Wave, T_C =125 °C, V_R = 0	-	-	24.0	kA
I^2t	Limiting load integral	Sine Wave, 10ms	-	-	288	10^4A^2s

Characteristics

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
V_{TM}	Peak on-state voltage	T_{vj} = 125 °C，I_{TM} = 1500 A	-	-	1.30	V
I_{DRM}	Forward leakage current	T_{vj} = 125 °C，V_{DRM}	-	-	150	mA
I_{RRM}	Reverse leakage current	T_{vj} = 125 °C，V_{RRM}	-	-	150	mA
V_{TO}	Threshold voltage	T_{vj} = 125 °C	-	-	0.89	V
r_T	Slope resistance	T_{vj} = 125 °C	-	-	0.27	mΩ
I_H	Holding current	T_{vj} = 25 °C	-	-	200	mA
I_L	Latching current	T_{vj} = 25 °C	-	-	1000	mA

Dynamic Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
dv/dt	Critical rate of rise of off-state voltage	T_{vj} = 125 °C，0.67V_{DRM}	1000	-	-	V/μs
di/dt	Critical rate of rise of on-state current	T_{vj} =125°C，V_{DM} =0.67V_{DRM}，I_{TM} =2000A I_{FG} = 2 A，tr = 0.5 μs, f = 50 Hz	-	-	200	A/μs
t_d	Delay time	T_{vj} = 25 °C，V_{DM} = 0.5V_{DRM}，I_{TM} = 2000 A I_{FG} = 2 A，tr = 0.5 μs	-	-	3.0	μs
t_q	Turn-off time	T_{vj}=125°C，V_{DM}=0.67V_{DRM}，dv/dt=20V/μs，V_R=200V di_T / dt = -10 A/μs，I_T = 2000 A	-	300	-	μs
Q_{rr}	Recovery Charge	T_{vj} = 125°C，di_T / dt = -10A / μs，V_R = 200V， I_T = 2000A	-	-	3200	μC
I_{rr}	Reverse recovery current		-	-	160	A

Gate Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
I_{GT}	Gate trigger current	T_{vj} = 25 °C	-	-	300	mA
V_{GT}	Gate trigger voltage	T_{vj} = 25 °C	-	-	3.0	V
I_{GD}	Gate non-trigger current	T_{vj} = 125 °C，V_D = 0.4V_{DRM}	10	-	-	mA
V_{GD}	Gate non-trigger voltage	T_{vj} = 125 °C，V_D = 0.4V_{DRM}	0.3	-	-	V
V_{FGM}	Peak forward gate voltage		-	-	12	V
V_{RGM}	Peak reverse gate voltage		-	-	5	V
I_{FGM}	Peak forward gate current		-	-	4	A
P_{GM}	Gate power losses		-	-	20	W
$P_{G(AV)}$	Gate power losses (mean)		-	-	4	W

Max. on-state characteristic model

$$V_T = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

	25 °C	125 °C
A	0.805933	0.351731
B	0.0171905	0.0795715
C	0.00012463	0.00017343
D	0.0063573	0.0025590

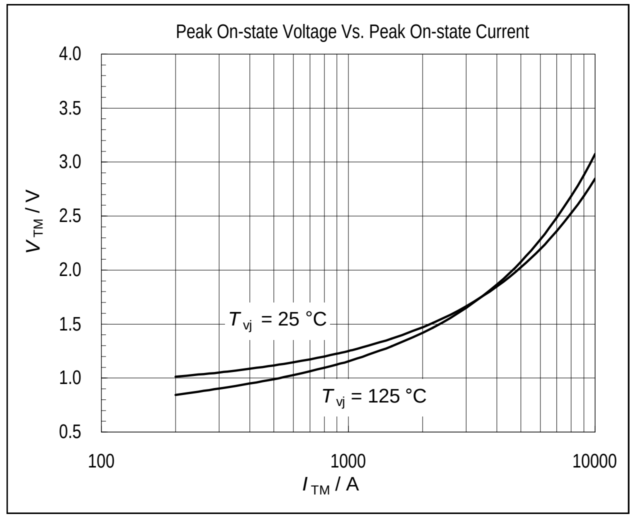


Fig1. Peak On-state Voltage Vs. Peak On-state Current

Transient thermal impedance function (double side cooled)

$$R_{thjc}(t) = \sum_{i=1}^{n} R_{thi} \cdot \left(1 - e^{-\frac{t}{t_i}}\right)$$

i	1	2	3	4
R_{thi} (K/kW)	13.267	4.05	1.585	1.102
τ_i (s)	0.6894	0.0872	0.0217	0.0043

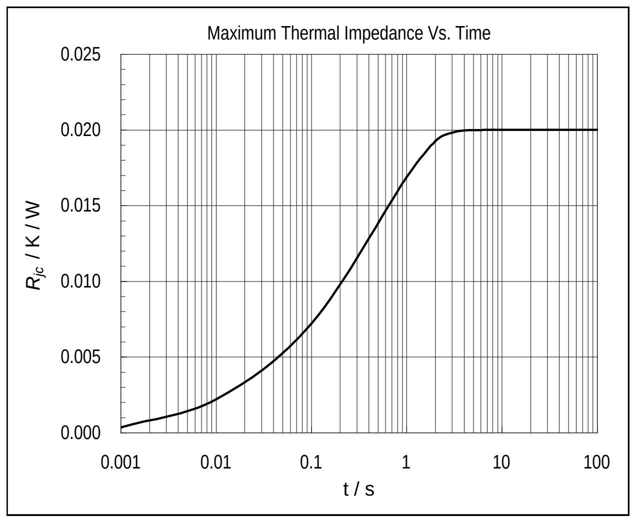


Fig2. Maximum Thermal Impedance Vs. Time

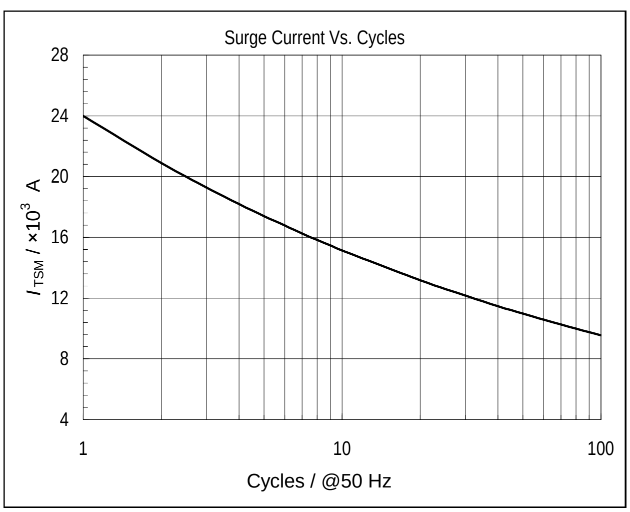


Fig3. Surge Current Vs. Cycles

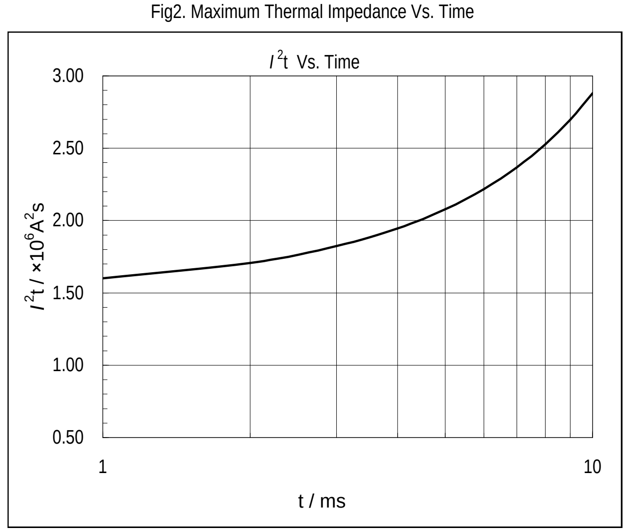


Fig4. I^2t Vs. Time

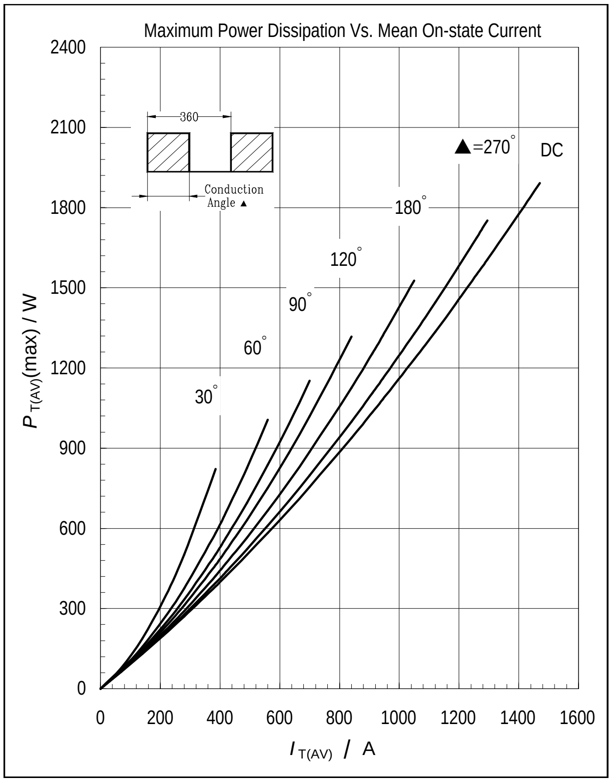


Fig5. Maximum Power Dissipation Vs. Mean On-state Current

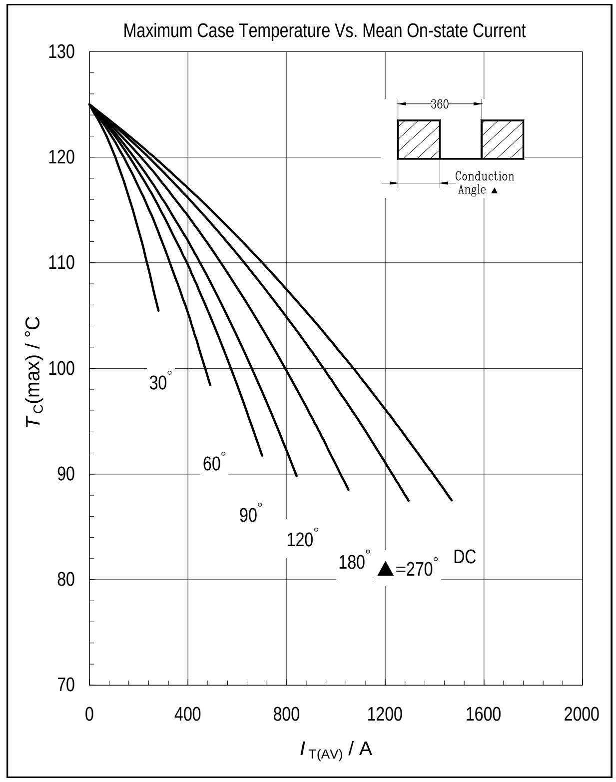


Fig6. Maximum Case Temperature Vs. Mean On-state Current

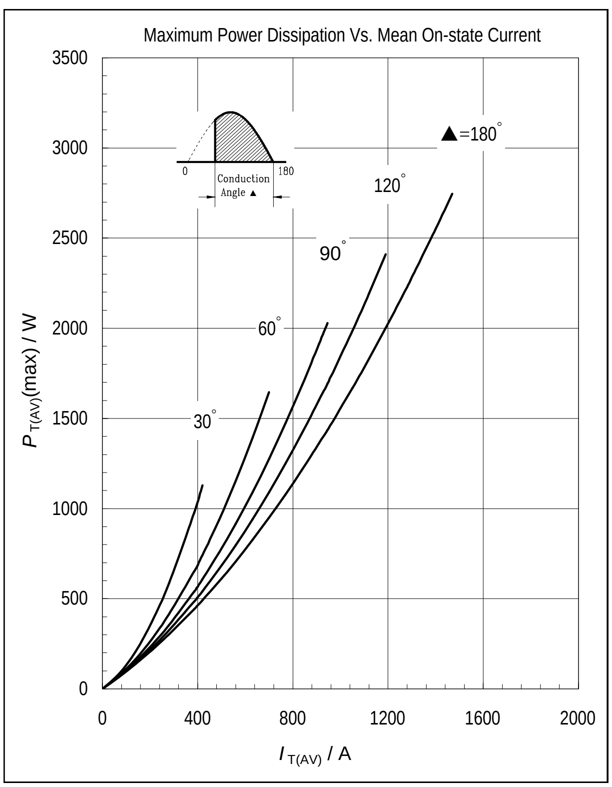


Fig7. Maximum Power Dissipation Vs. Mean On-state Current

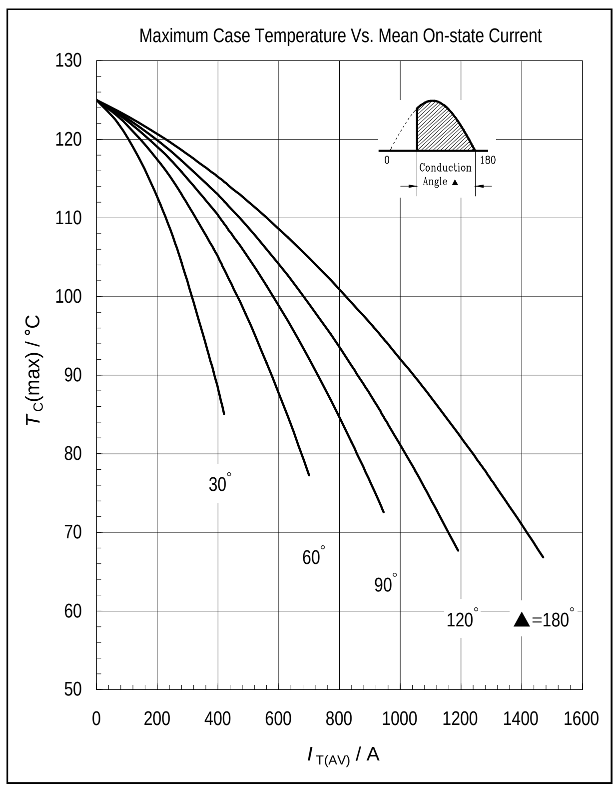


Fig8. Maximum Case Temperature Vs. Mean On-state Current

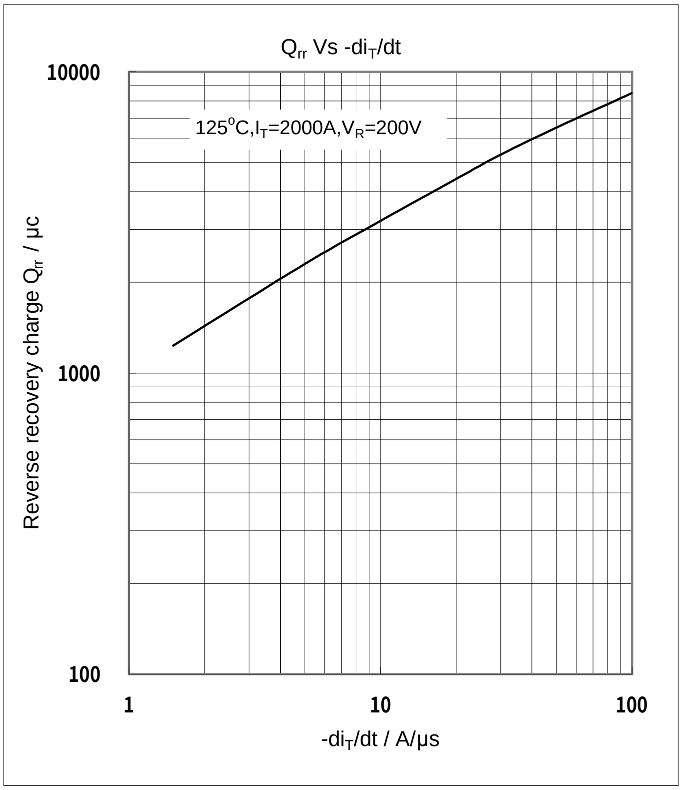


Fig9. Reverse recovery charge Vs. $-di_T/dt$

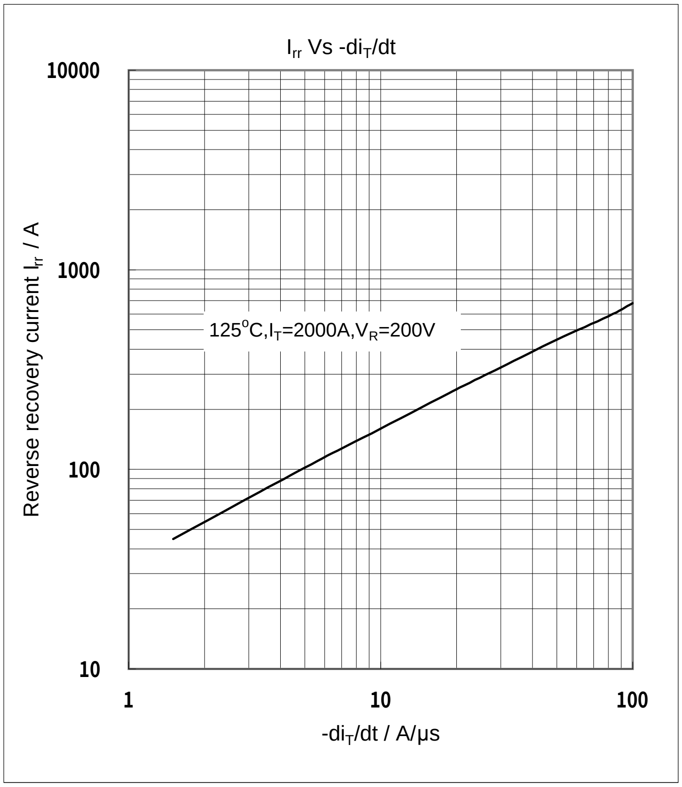


Fig10. Reverse recovery current Vs. $-di_T/dt$

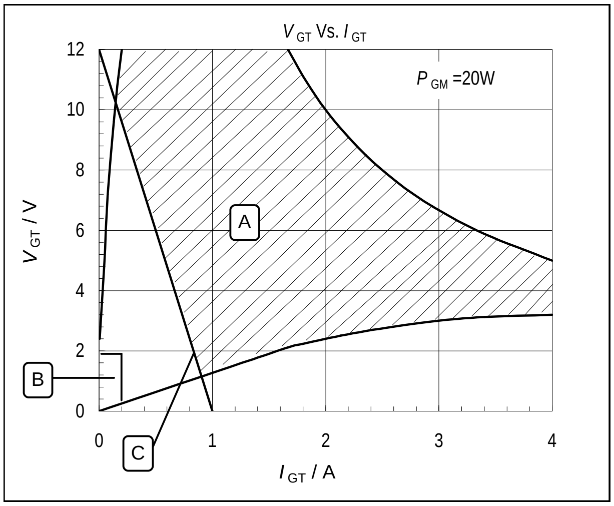


Fig11. V_{GT} Vs. I_{GT}

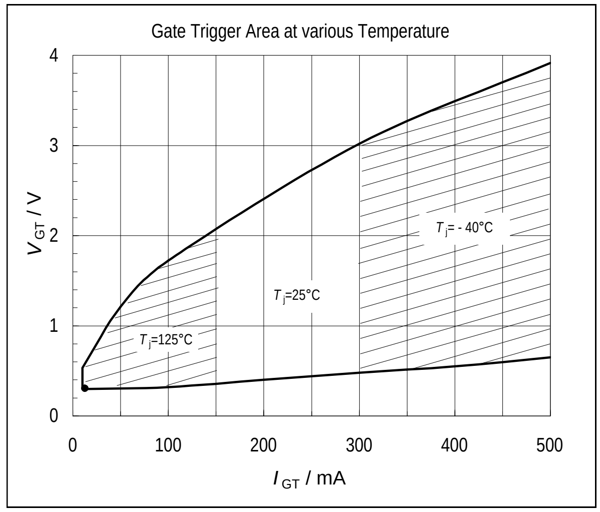


Fig12. Gate Trigger Area at various Temperature

A is Recommended Triggering Area.

B is Unreliable Triggering Area.

C is Recommended Gate Load Line.

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