

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

- Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noise Environments
- Driver Positive- and Negative-Current Limiting
- Thermal Shutdown Protection
- Driver 3-State Outputs
- Receiver Common-Mode Input Voltage Range of -12 V to 12 V
- Receiver Input Sensitivity . . . $\pm 200\text{ mV}$
- Receiver Hysteresis . . . 50 mV Typ
- Receiver Input Impedance . . . $12\text{ k}\Omega\text{ Min}$
- Receiver 3-State Outputs (SN751177 Only)
- Operate From Single 5-V Supply

description

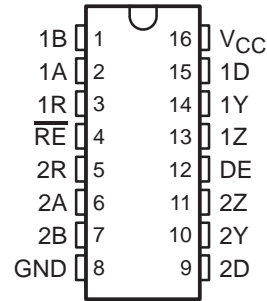
The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 Mbit/s. They are designed to improve the performance of full-duplex data communications over long bus lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal-shutdown protection from line-fault conditions on the transmission bus line.

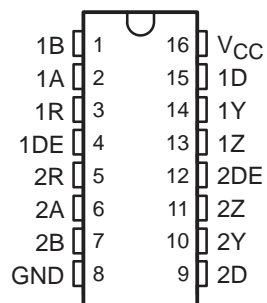
The receiver features high input impedance of at least $12\text{ k}\Omega$, an input sensitivity of $\pm 200\text{ mV}$ over a common-mode input voltage range of -12 V to 12 V , and typical input hysteresis of 50 mV . Fail-safe design ensures that if the receiver inputs are open, the receiver outputs always will be high.

The SN751177 and SN751178 are characterized for operation from -20°C to 85°C .

SN751177 . . . N OR NS† PACKAGE
(TOP VIEW)



SN751178 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available taped and reeled.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

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Function Tables

SN751177, SN751178
(each driver)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN751177
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

SN751178
(each receiver)

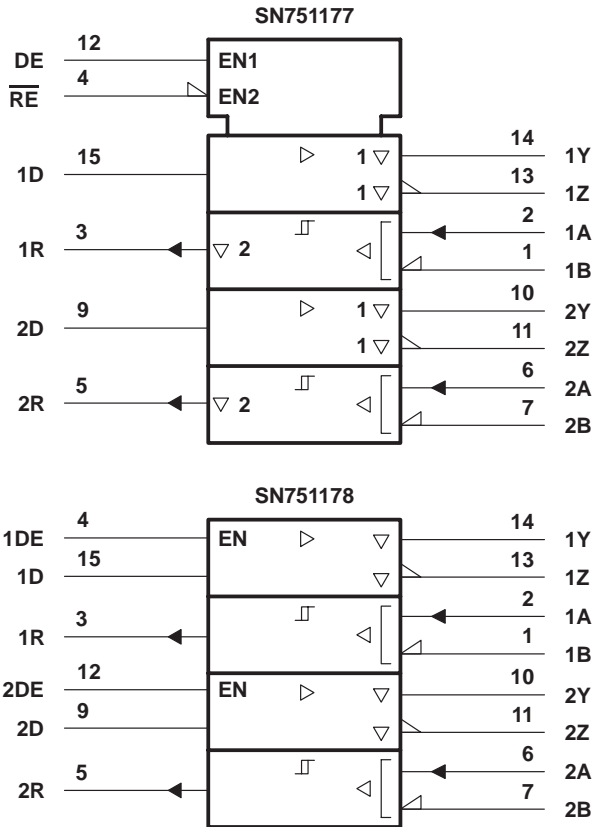
DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2 V$	H
$-0.2 V < V_{ID} < 0.2 V$?
$V_{ID} \leq -0.2 V$	L

H = high level, L = low level,
? = indeterminate

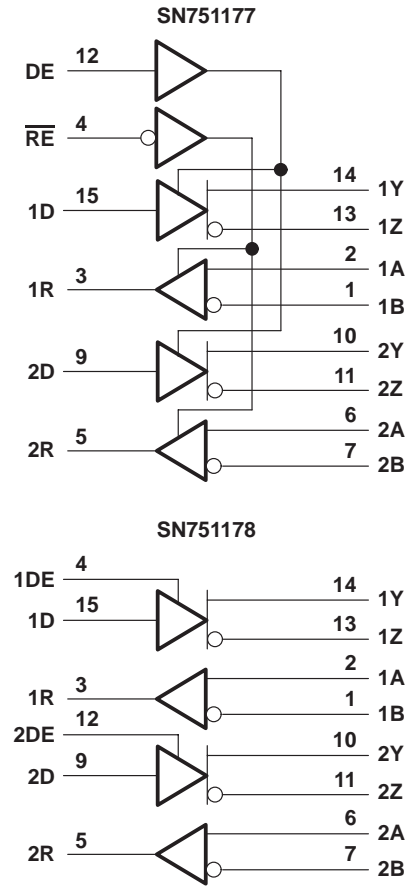
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logic symbols†

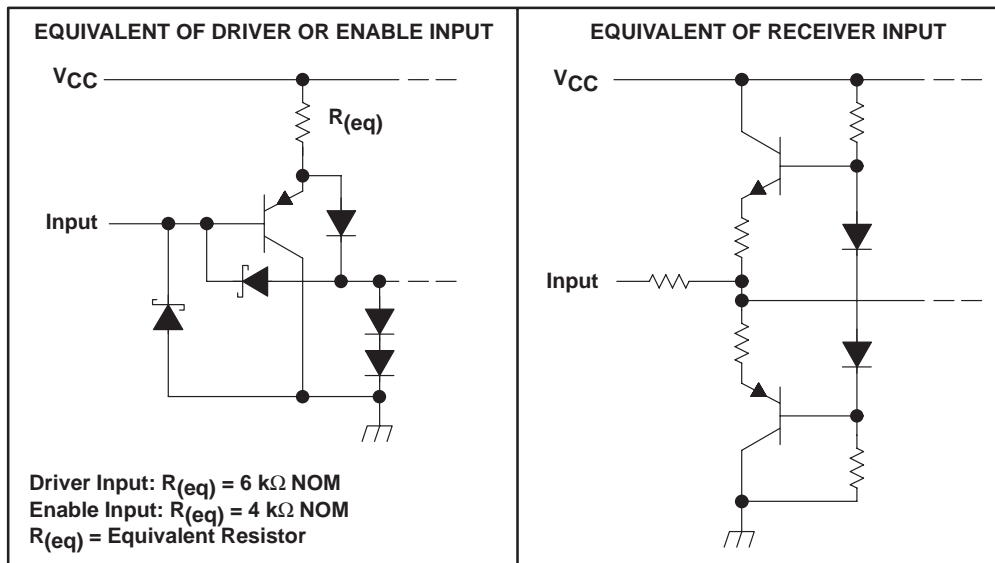


logic diagrams (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs

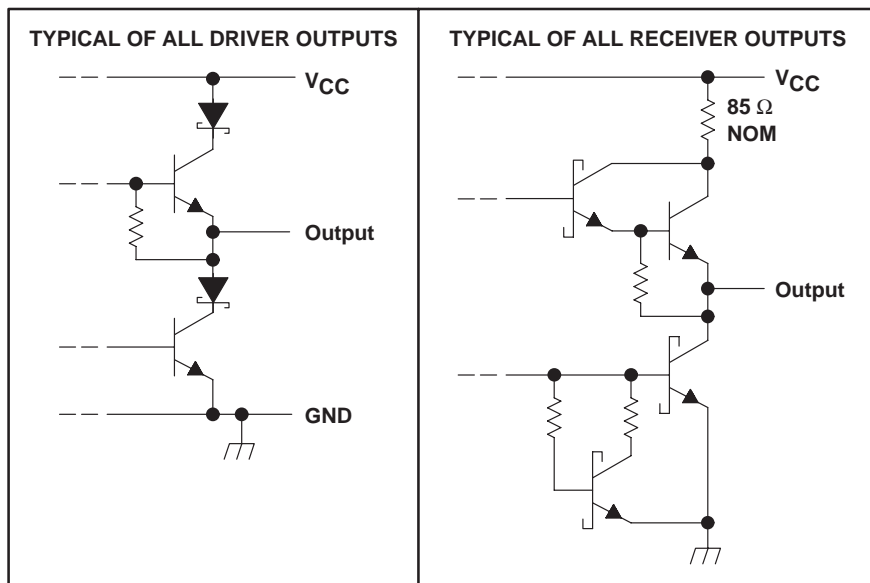


All resistor values are nominal.

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schematics of outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (DE, \overline{RE} , and D inputs)	7 V
Receiver input voltage range, V_I (A or B inputs)	-25 V to 25 V
Receiver differential input voltage range, V_{ID} (see Note 2)	-25 V to 25 V
Driver output voltage range, V_O	-10 V to 15 V
Receiver low-level output current, I_{OL}	50 mA
Package thermal impedance, θ_{JA} (see Note 3): N package	78°C/W
NS package	111°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
 2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DE, \overline{RE} , and D inputs	2			V
Low-level input voltage, V_{IL}		0.8			V
Common-mode output voltage, V_{OC}	Driver	-7^\dagger		12	V
High-level output current, I_{OH}				-60	mA
Low-level output current, I_{OL}				60	mA
Common-mode input voltage, V_{IC}	Receiver			± 12	V
Differential input voltage, V_{ID}				± 12	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		-20		85	$^\circ C$

[†] The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

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DRIVER SECTIONS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -33 mA		3.7		V
V _{OL}	Low-level output voltage	V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = 33 mA		1.1		V
V _{OD1}	Differential output voltage	I _O = 0	1.5		6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω, See Figure 1	2 or 1/2 V _{OD1} ‡			V
		R _L = 54 Ω, See Figure 1	1.5		5	
V _{OD3}	Differential output voltage	See Note 4	1.5		5	V
Δ V _{OD}	Change in magnitude of differential output voltage (see Note 5)	R _L = 54 Ω or 100 Ω, See Figure 1			±0.2	V
V _{OC}	Common-mode output voltage		-1§		3	V
Δ V _{OC}	Change in magnitude of common-mode output voltage (see Note 5)				±0.2	V
I _O	Output current with power off	V _{CC} = 0, V _O = -7 V to 12 V			±100	μA
I _{OZ}	High-impedance-state output current	V _O = -7 V to 12 V			±100	μA
I _{IH}	High-level input current	V _{IH} = 2.7 V			20	μA
I _{IL}	Low-level input current	V _{IL} = 0.4 V			-100	μA
I _{OS}	Short-circuit output current (see Note 6)	V _O = -7 V			-250	mA
		V _O = V _{CC}			250	
		V _O = 12 V			250	
I _{CC}	Supply current	No load	Outputs enabled	80	110	mA
			Outputs disabled	50	80	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

§ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See TIA/EIA-485-A Figure 3.5, Test Termination Measurement 2

5. Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _d (OD)	Differential output delay time	R _L = 54 Ω, See Figure 3		20	25	ns
t _t (OD)	Differential output transition time			27	35	
t _{PLH}	Propagation delay time, low- to high-level output	R _L = 27 Ω, See Figure 4		20	25	ns
t _{PHL}	Propagation delay time, high- to low-level output			20	25	
t _{PZH}	Output enable time to high level	R _L = 110 Ω, See Figure 5		80	120	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω, See Figure 6		40	60	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω, See Figure 5		90	120	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω, See Figure 6		30	45	ns



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SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V _{OD1}	V _O	V _O
V _{OD2}	V _t (R _L = 100 Ω)	V _t (R _L = 54 Ω)
V _{OD3}		V _t (Test Termination Measurement 2)
Δ V _{OD}	V _t - V̄ _t	V _t - V̄ _t
V _{OC}	V _{OS}	V _{OS}
Δ V _{OC}	V _{OS} - V̄ _{OS}	V _{OS} - V̄ _{OS}
I _{OS}	I _{sa} , I _{sb}	
I _O	I _{xa} , I _{xb}	I _{ia} , I _{ib}

RECEIVER SECTIONS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V, I _O = -0.4 mA			0.2	V
V _{IT-}	Negative-going input threshold voltage	V _O = 0.5 V, I _O = 16 mA	-0.2‡			V
V _{hys}	Input hysteresis voltage (V _{IT+} - V _{IT-})			50		mV
V _{IK}	Enable clamp voltage	SN751177 I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{ID} = 200 mV, I _{OH} = -400 μA		2.7		V
V _{OL}	Low-level output voltage	V _{ID} = -200 mV			0.45	V
					0.5	
I _{OZ}	High-impedance-state output current	SN751177 V _O = 0.4 V to 2.4 V			±20	μA
I _I	Line input current (see Note 7)	Other input at 0 V			1	mA
					-0.8	
I _{IH}	High-level enable input current	SN751177 V _{IH} = 2.7 V			20	μA
I _{IL}	Low-level enable input current	SN751177 V _{IL} = 0.4 V			-100	μA
I _{OS}	Short-circuit output current (see Note 6)		-15		-85	μA
I _{CC}	Supply current	No load, Outputs enabled		80	110	mA
r _i	Input resistance			12		kΩ

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7. Refer to ANSI Standards TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.



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switching characteristics at $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, See Figure 7		20	35	ns
t_{PHL} Propagation delay time, high- to low-level output			22	35	ns
t_{PZH} Output enable time to high level	SN751177 See Figure 8		17	25	ns
t_{PZL} Output enable time to low level			20	27	ns
t_{PHZ} Output disable time from high level			25	40	ns
t_{PLZ} Output disable time from low level			30	40	ns

PARAMETER MEASUREMENT INFORMATION

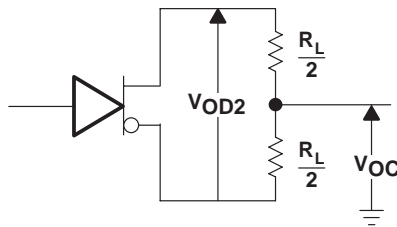


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

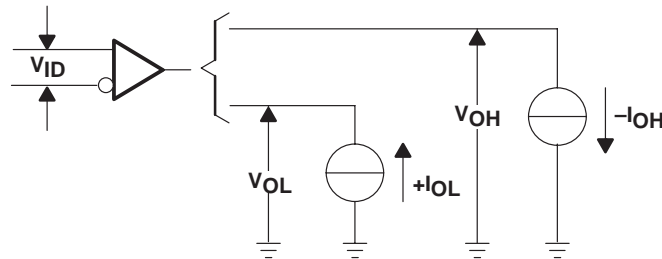
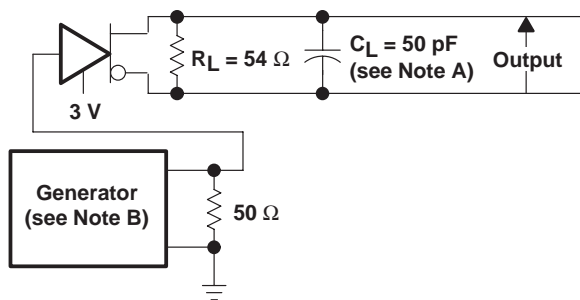
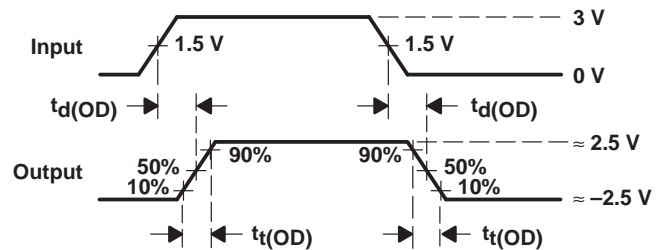


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



TEST CIRCUIT



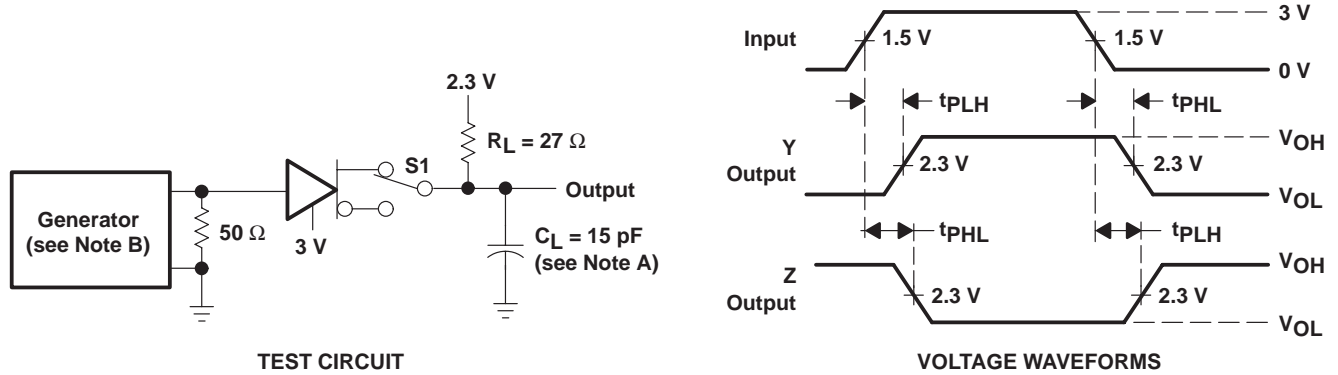
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.

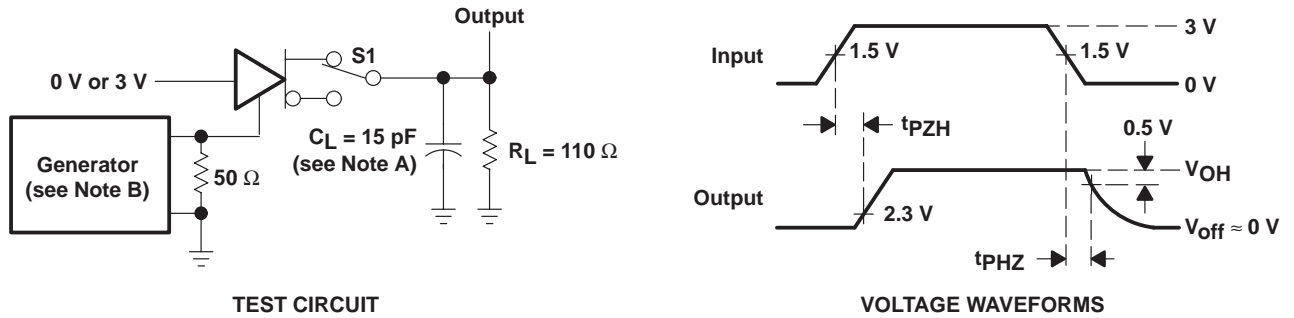
Figure 3. Driver Differential Output-Delay and Transition-Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



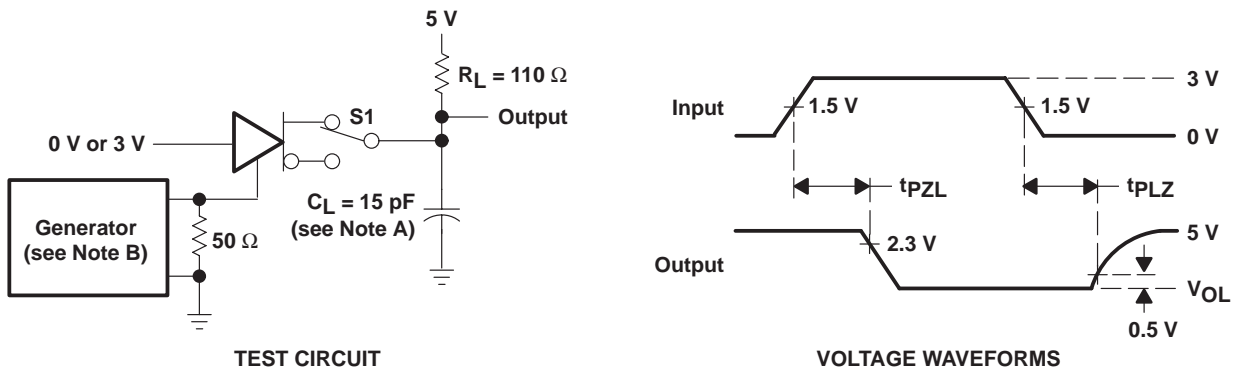
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.

Figure 4. Driver Propagation-Time Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.

Figure 5. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms



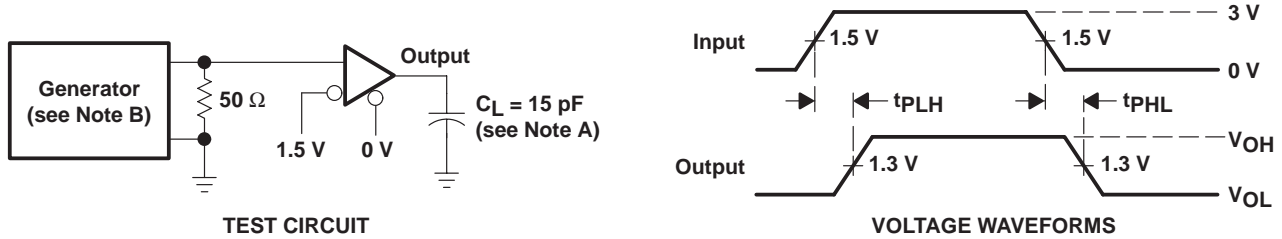
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.

Figure 6. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms

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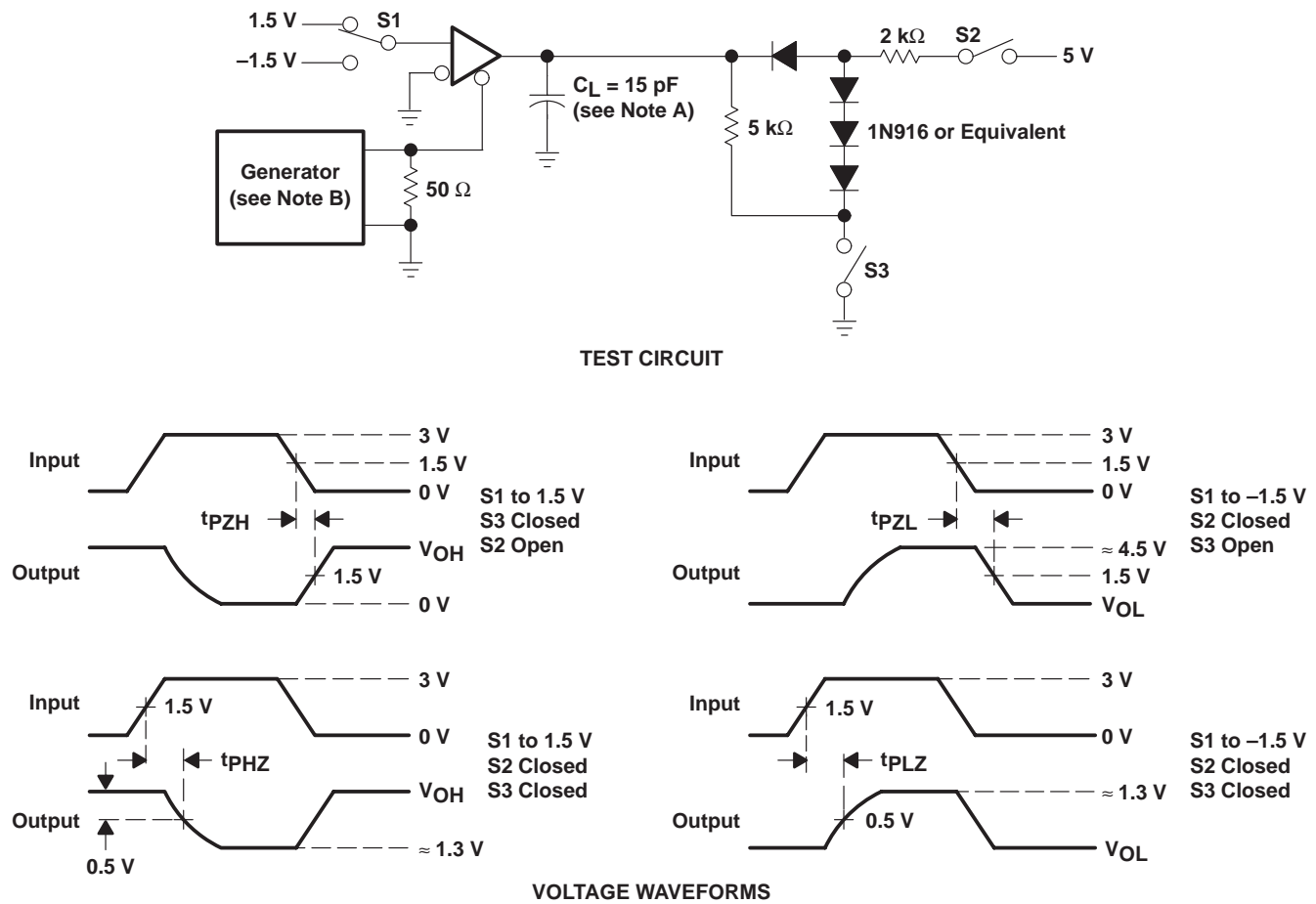
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\ \text{MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\ \text{ns}$, $t_f \leq 6\ \text{ns}$.

Figure 7. Receiver Propagation-Time Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR \leq 1\ \text{MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\ \text{ns}$, $t_f \leq 6\ \text{ns}$.

Figure 8. Receiver Output Enable- and Disable-Time Test Circuit and Voltage Waveforms

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