

# CD74HC259, CD74HCT259

## High Speed CMOS Logic 8-Bit Addressable Latch

### Features

- Buffered Inputs and Outputs
- Four Operating Modes
- Typical Propagation Delay of 15ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC259 and CD74HCT259 Addressable Latch features the low-power consumption associated with CMOS circuitry and has speeds comparable to low-power Schottky.

This latches three active modes and one reset mode. When both the Latch Enable ( $\overline{LE}$ ) and Master Reset ( $\overline{MR}$ ) inputs are low (8-line Demultiplexer mode) the output of the addressed latch follows the Data input and all other outputs are forced low. When both  $\overline{MR}$  and  $\overline{LE}$  are high (Memory Mode), all outputs are isolated from the Data input, i.e., all latches hold the last data presented before the  $\overline{LE}$  transition from low to high. A condition of  $\overline{LE}$  low and  $\overline{MR}$  high (Addressable Latch mode) allows the addressed latch's output to follow the data input; all other latches are unaffected. The Reset mode (all outputs low) results when  $\overline{LE}$  is high and  $\overline{MR}$  is low.

### Ordering Information

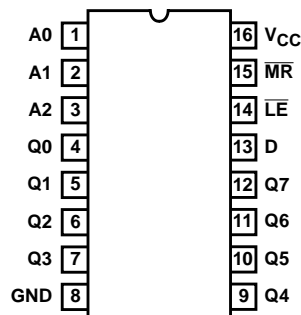
| PART NUMBER | TEMP. RANGE ( $^\circ C$ ) | PACKAGE    | PKG. NO. |
|-------------|----------------------------|------------|----------|
| CD74HC259E  | -55 to 125                 | 16 Ld PDIP | E16.3    |
| CD74HCT259E | -55 to 125                 | 16 Ld PDIP | E16.3    |
| CD74HC259M  | -55 to 125                 | 16 Ld SOIC | M16.15   |
| CD74HCT259M | -55 to 125                 | 16 Ld SOIC | M16.15   |

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

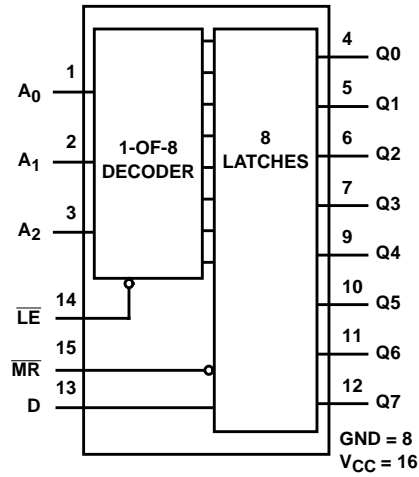
### Pinout

CD74HC259, CD74HCT259  
(PDIP, SOIC)  
TOP VIEW



**CD74HC259, CD74HCT259**

**Functional Diagram**



**TRUTH TABLE**

| INPUTS |    | OUTPUT OF ADDRESS LATCH | EACH OTHER OUTPUT | FUNCTION             |
|--------|----|-------------------------|-------------------|----------------------|
| MR     | LE |                         |                   |                      |
| H      | L  | D                       | Q <sub>i0</sub>   | Addressable Latch    |
| H      | H  | Q <sub>i0</sub>         | Q <sub>i0</sub>   | Memory               |
| L      | L  | D                       | L                 | 8-Line Demultiplexer |
| L      | H  | L                       | L                 | Reset                |

**LATCH SELECTION TABLE**

| SELECT INPUTS |    |    | LATCH ADDRESSED |
|---------------|----|----|-----------------|
| A2            | A1 | A0 |                 |
| L             | L  | L  | 0               |
| L             | L  | H  | 1               |
| L             | H  | L  | 2               |
| L             | H  | H  | 3               |
| H             | L  | L  | 4               |
| H             | L  | H  | 5               |
| H             | H  | L  | 6               |
| H             | H  | H  | 7               |

**NOTE:**

H = High Voltage Level

L = Low Voltage Level

D = The level at the data input

Q<sub>i0</sub> = The level of Q<sub>i</sub> (i = 0, 1...7, as appropriate) before the indicated steady-state input conditions were established.

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## Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                          | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                           |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....           | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                          |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....           | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                        |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$ .....                    | $\pm 25mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$     |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....           | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ ..... | $\pm 50mA$  |

## Thermal Information

|  |                                  |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 3)           | $\theta_{JA}$ (°C/W)             |
| PDIP Package .....                             | 90                               |
| SOIC Package .....                             | 115                              |
| Maximum Junction Temperature .....             | 150°C                            |
| Maximum Storage Temperature Range .....        | -65°C to 150°C                   |
| Maximum Lead Temperature (Soldering 10s) ..... | 300°C<br>(SOIC - Lead Tips Only) |

## Operating Conditions

|  |                |
|--|----------------|
| Temperature Range, $T_A$ .....               | -55°C to 125°C |
| Supply Voltage Range, $V_{CC}$               |                |
| HC Types .....                               | .2V to 6V      |
| HCT Types .....                              | 4.5V to 5.5V   |
| DC Input or Output Voltage, $V_I, V_O$ ..... | 0V to $V_{CC}$ |
| Input Rise and Fall Time                     |                |
| 2V .....                                     | 1000ns (Max)   |
| 4.5V .....                                   | 500ns (Max)    |
| 6V .....                                     | 400ns (Max)    |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL   | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |      |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |   |
|---|----------|----------------------|------------|--------------|------|------|-----------|---------------|---------|----------------|---------|---------|---|
|   |          | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP  | MAX       | MIN           | MAX     | MIN            | MAX     |         |   |
| <b>HC TYPES</b>                         |          |                      |            |              |      |      |           |               |         |                |         |         |   |
| High Level Input Voltage                | $V_{IH}$ | -                    | -          | 2            | 1.5  | -    | -         | 1.5           | -       | 1.5            | -       | V       |   |
|   |          |                      |            | 4.5          | 3.15 | -    | -         | 3.15          | -       | 3.15           | -       | V       |   |
|   |          |                      |            | 6            | 4.2  | -    | -         | 4.2           | -       | 4.2            | -       | V       |   |
| Low Level Input Voltage                 | $V_{IL}$ | -                    | -          | 2            | -    | -    | 0.5       | -             | 0.5     | -              | 0.5     | V       |   |
|   |          |                      |            | 4.5          | -    | -    | 1.35      | -             | 1.35    | -              | 1.35    | V       |   |
|   |          |                      |            | 6            | -    | -    | 1.8       | -             | 1.8     | -              | 1.8     | V       |   |
| High Level Output Voltage<br>CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02      | -0.02        | 2    | 1.9  | -         | -             | 1.9     | -              | 1.9     | -       | V |
|   |          |                      | -0.02      | -0.02        | 4.5  | 4.4  | -         | -             | 4.4     | -              | 4.4     | -       | V |
|   |          |                      | -0.02      | -0.02        | 6    | 5.9  | -         | -             | 5.9     | -              | 5.9     | -       | V |
| High Level Output Voltage<br>TTL Loads  | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -          | -            | -    | -    | -         | -             | -       | -              | -       | V       |   |
|   |          |                      | -4         | -4           | 4.5  | 3.98 | -         | -             | 3.84    | -              | 3.7     | -       | V |
|   |          |                      | -5.2       | -5.2         | 6    | 5.48 | -         | -             | 5.34    | -              | 5.2     | -       | V |
| Low Level Output Voltage<br>CMOS Loads  | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02       | 0.02         | 2    | -    | -         | 0.1           | -       | 0.1            | -       | 0.1     | V |
|   |          |                      | 0.02       | 0.02         | 4.5  | -    | -         | 0.1           | -       | 0.1            | -       | 0.1     | V |
|   |          |                      | 0.02       | 0.02         | 6    | -    | -         | 0.1           | -       | 0.1            | -       | 0.1     | V |
| Low Level Output Voltage<br>TTL Loads   | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | -          | -            | -    | -    | -         | -             | -       | -              | -       | V       |   |
|   |          |                      | 4          | 4            | 4.5  | -    | -         | 0.26          | -       | 0.33           | -       | 0.4     | V |
|   |          |                      | 5.2        | 5.2          | 6    | -    | -         | 0.26          | -       | 0.33           | -       | 0.4     | V |
| Input Leakage Current                   | $I_I$    | $V_{CC}$ or GND      | -          | 6            | -    | -    | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |   |

## CD74HC259, CD74HCT259

### DC Electrical Specifications (Continued)

| PARAMETER  | SYMBOL           | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|--|------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|  |                  | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| Quiescent Device Current                                       | I <sub>CC</sub>  | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| <b>HCT TYPES</b>   |                  |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>  | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage  | V <sub>IL</sub>  | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>  | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                  |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>  | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                  |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current  | I <sub>I</sub>   | V <sub>CC</sub> and GND            | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>  | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> | V <sub>CC</sub> -2.1               | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

| INPUT                    | UNIT LOADS |
|--------------------------|------------|
| A0 - A2, $\overline{LE}$ | 1.5        |
| D                        | 1.2        |
| $\overline{MR}$          | 0.75       |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

### Prerequisite for Switching Specifications

| PARAMETER                      | SYMBOL          | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     |     | -55°C TO 125°C |     |     | UNITS |    |
|--------------------------------|-----------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|----|
|                                |                 |                     | MIN  | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |       |    |
| <b>HC TYPES</b>                |                 |                     |      |     |     |               |     |     |                |     |     |       |    |
| Pulse Width<br>$\overline{LE}$ | t <sub>WL</sub> | 2                   | 70   | -   | -   | 90            | -   | -   | 105            | -   | -   | ns    |    |
|                                |                 |                     | 4.5  | 14  | -   | -             | 18  | -   | -              | 21  | -   | -     | ns |
|                                |                 |                     | 6    | 12  | -   | -             | 15  | -   | -              | 18  | -   | -     | ns |

**CD74HC259, CD74HCT259**

**Prerequisite for Switching Specifications (Continued)**

| PARAMETER  | SYMBOL          | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     |     | -55°C TO 125°C |     |     | UNITS |
|--|-----------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|
|  |                 |                     | MIN  | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |       |
| MR   | t <sub>WL</sub> | 2                   | 70   | -   | -   | 90            | -   | -   | 105            | -   | -   | ns    |
|  |                 | 4.5                 | 14   | -   | -   | 18            | -   | -   | 21             | -   | -   | ns    |
|  |                 | 6                   | 12   | -   | -   | 15            | -   | -   | 18             | -   | -   | ns    |
| Setup Time<br>D to $\overline{LE}$<br>A to $\overline{LE}$ | t <sub>SU</sub> | 2                   | 80   | -   | -   | 100           | -   | -   | 120            | -   | -   | ns    |
|  |                 | 4.5                 | 16   | -   | -   | 20            | -   | -   | 24             | -   | -   | ns    |
|  |                 | 6                   | 14   | -   | -   | 17            | -   | -   | 20             | -   | -   | ns    |
| Hold Time<br>D to $\overline{LE}$<br>A to $\overline{LE}$  | t <sub>H</sub>  | 2                   | 0    | -   | -   | 0             | -   | -   | 0              | -   | -   | ns    |
|  |                 | 4.5                 | 0    | -   | -   | 0             | -   | -   | 0              | -   | -   | ns    |
|  |                 | 6                   | 0    | -   | -   | 0             | -   | -   | 0              | -   | -   | ns    |
| <b>HCT TYPES</b>   |                 |                     |      |     |     |               |     |     |                |     |     |       |
| Pulse Width<br>$\overline{LE}$<br>MR                       | t <sub>WL</sub> | 4.5                 | 18   | -   | -   | 23            | -   | -   | 27             | -   | -   | ns    |
| Setup Time<br>D to $\overline{LE}$<br>A to $\overline{LE}$ | t <sub>SU</sub> | 4.5                 | 17   | -   | -   | 21            | -   | -   | 26             | -   | -   | ns    |
| Hold Time<br>D to $\overline{LE}$<br>A to $\overline{LE}$  | t <sub>H</sub>  | 4.5                 | 0    | -   | -   | 0             | -   | -   | 0              | -   | -   | ns    |

**Switching Specifications** C<sub>L</sub> = 50pF, Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                   | SYMBOL           | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------|------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                             |                  |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| <b>HC TYPES</b>             |                  |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay<br>D to Q | t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 185 | -             | 230 | -              | 280 | ns    |
|                             |                  |                       | 4.5                 | -    | -   | 37  | -             | 46  | -              | 56  | ns    |
|                             |                  | C <sub>L</sub> = 15pF | 5                   | -    | 15  | -   | -             | -   | -              | -   | ns    |
|                             |                  | C <sub>L</sub> = 50pF | 6                   | -    | -   | 31  | -             | 39  | -              | 48  | ns    |
| $\overline{LE}$ to Q        | t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 170 | -             | 215 | -              | 255 | ns    |
|                             |                  |                       | 4.5                 | -    | -   | 34  | -             | 43  | -              | 51  | ns    |
|                             |                  | C <sub>L</sub> = 15pF | 5                   | -    | 14  | -   | -             | -   | -              | -   | ns    |
|                             |                  | C <sub>L</sub> = 50pF | 6                   | -    | -   | 29  | -             | 37  | -              | 43  | ns    |

## CD74HC259, CD74HCT259

### Switching Specifications $C_L = 50\text{pF}$ , Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER                                  | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V)        | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--|--------------------|---------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|  |                    |                     |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| A to Q                                     | $t_{PHL}$          | $C_L = 50\text{pF}$ | 2                   | -    | -   | 185 | -             | 230 | -              | 280 | ns    |
|  |                    |                     | 4.5                 | -    | -   | 37  | -             | 46  | -              | 56  | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5                   | -    | 15  | -   | -             | -   | -              | -   | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6                   | -    | -   | 31  | -             | 39  | -              | 48  | ns    |
| $\overline{MR}$ to Q                       | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 2                   | -    | -   | 155 | -             | 195 | -              | 235 | ns    |
|  |                    |                     | 4.5                 | -    | -   | 31  | -             | 39  | -              | 47  | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5                   | -    | 13  | -   | -             | -   | -              | -   | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6                   | -    | -   | 26  | -             | 33  | -              | 40  | ns    |
| Output Transition Time                     | $t_{THL}, t_{TLH}$ | $C_L = 50\text{pF}$ | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|  |                    |                     | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|  |                    |                     | 6                   | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Power Dissipation Capacitance (Notes 4, 5) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5                   | -    | 21  | -   | -             | -   | -              | -   | pF    |
| Input Capacitance                          | $C_I$              | $C_L = 50\text{pF}$ | -                   | 10   | -   | 10  | -             | 10  | -              | 10  | pF    |
| <b>HCT TYPES</b>                           |                    |                     |                     |      |     |     |               |     |                |     |       |
| Propagation Delay<br>D to Q                | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 4.5                 | -    | -   | 39  | -             | 49  | -              | 59  | ns    |
|  |                    |                     | $C_L = 15\text{pF}$ | 5    | -   | 16  | -             | -   | -              | -   | -     |
| $\overline{LE}$ to Q                       | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 4.5                 | -    | -   | 38  | -             | 48  | -              | 57  | ns    |
|  |                    |                     | $C_L = 15\text{pF}$ | 5    | -   | 16  | -             | -   | -              | -   | -     |
| A to Q                                     | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 4.5                 | -    | -   | 41  | -             | 51  | -              | 61  | ns    |
|  |                    |                     | $C_L = 15\text{pF}$ | 5    | -   | 17  | -             | -   | -              | -   | -     |
| $\overline{MR}$ to Q                       | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 4.5                 | -    | -   | 39  | -             | 49  | -              | 59  | ns    |
|  |                    |                     | $C_L = 15\text{pF}$ | 5    | -   | 16  | -             | -   | -              | -   | -     |
| Power Dissipation Capacitance (Notes 4, 5) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5                   | -    | 22  | -   | -             | -   | -              | -   | pF    |
| Input Capacitance                          | $C_I$              | $C_L = 50\text{pF}$ | -                   | 10   | -   | 10  | -             | 10  | -              | 10  | pF    |
| Output Transition Time                     | $t_{THL}, t_{TLH}$ | $C_L = 50\text{pF}$ | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |

**NOTES:**

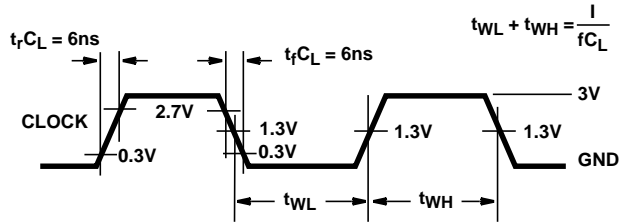
4.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
5.  $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_O$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

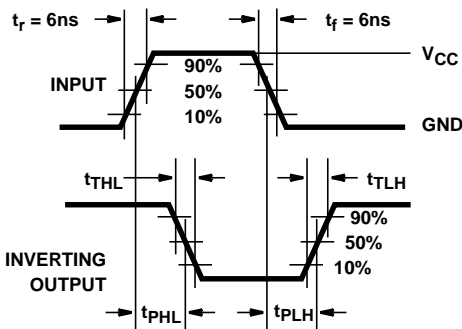


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

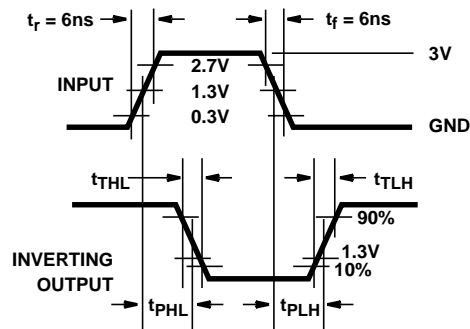


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

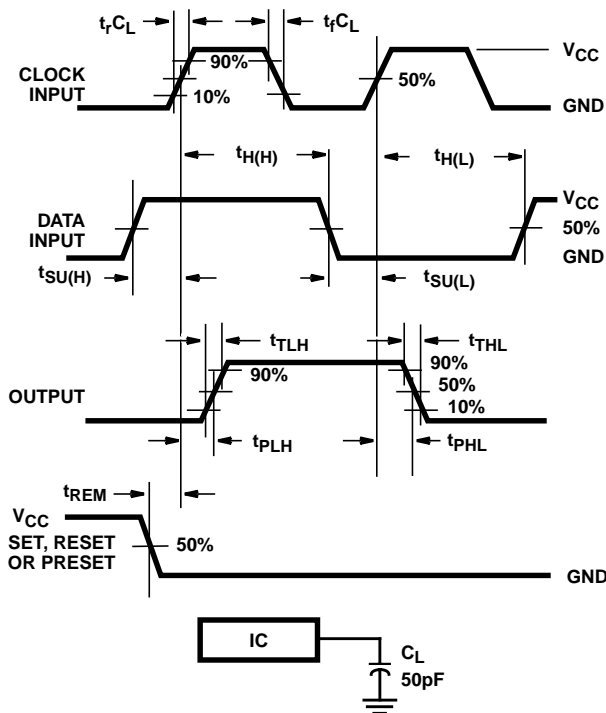


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

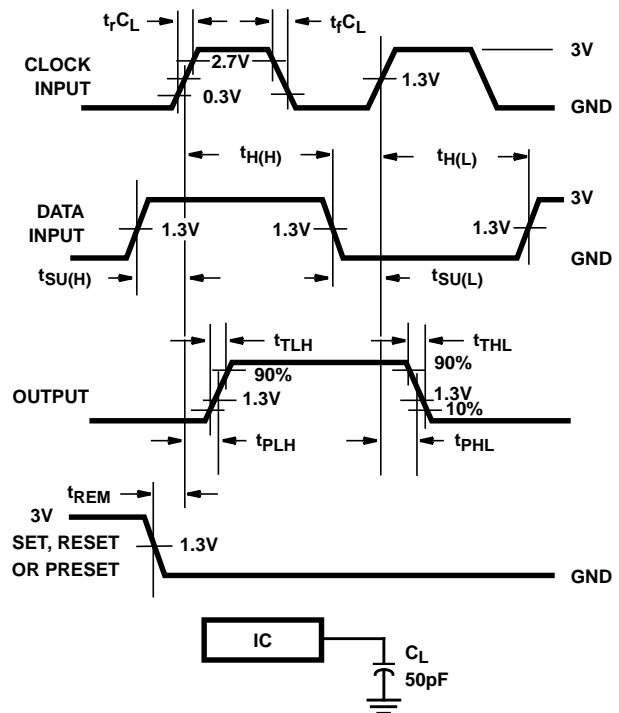


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**Test Circuits and Waveforms** (Continued)

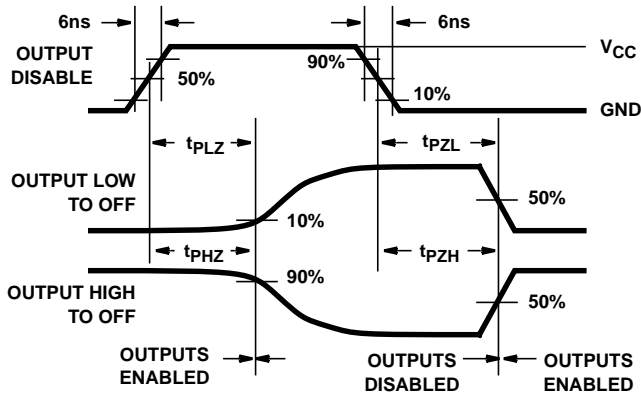


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

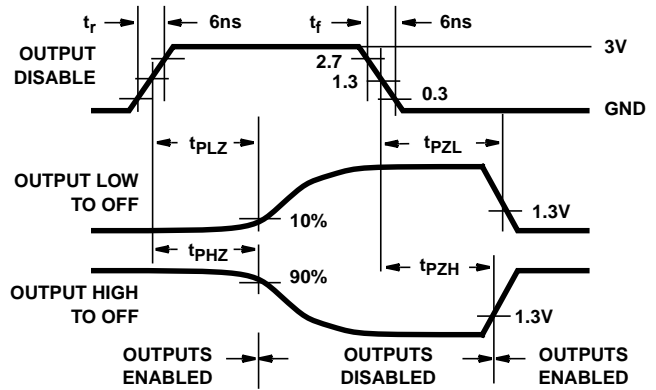
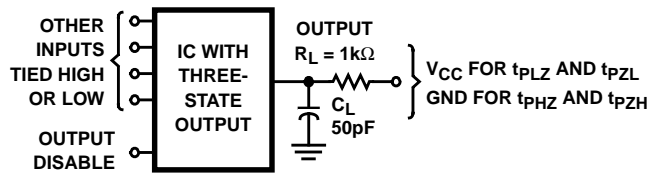


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT



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