DAP018A/B/C/D/F

PWM Current-Mode Controller for High-Power Universal Off-Line Supplies

Housed in a SO−14 package, the DAP018X represents an enhanced version of the currently available Speedking controller, the DAP011.

With an internal structure operating at a fixed 65 kHz or 100 kHz frequency, the controller directly connects to the high−voltage rail for a lossless and clean startup sequence. Current−mode control also provides an excellent input audio−susceptibility and inherent pulse−by−pulse control. Internal ramp compensation easily prevents sub−harmonic oscillations from taking place in continuous conduction mode designs. On top of these features, the device takes advantage of the auxiliary winding negative swing to let the user adjust the maximum power the converter can deliver in high line conditions (OPP).

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically freezes the peak current and reduces its switching frequency down to 25 kHz. At this point, if further output power reduction occurs, the controller enters skip−cycle.

The DAP018X features an efficient protective circuitry which, in presence of an overcurrent condition, disables the output pulses while the device enters a safe burst mode, trying to re−start. Once the fault has gone, the device auto−recovers. By implementing a timer to acknowledge a fault condition, independently from the auxiliary supply, the designer's task is eased when stringent fault mode conditions need to be met.

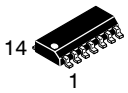
A dedicated input helps triggering a latch−off circuitry which permanently disables output pulses, for instance to implement an over voltage protection (OVP). A separate input accepts a direct NTC connection to ground for a simple and efficient over temperature protection (OTP).

Features

- Fixed−frequency 65 kHz (A and B versions) or 100 kHz (C and D versions) Current−mode Control Operation
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Frequency Foldback down to 25 kHz and Skip−cycle in Light Load Conditions
- Reduced Internal Bias Currents for Improved Standby Performance
- Adjustable Brown−out Protection (B and D versions)
- Internal Ramp Compensation
- Internal Fixed 5 ms Soft−Start
- Adjustable Frequency Jittering for Better EMI Signature
- Auto−recovery internal output short−circuit protection for A, B, C and D versions. F is latched
- Adjustable Timer for Improved Short−circuit Protection
- OTP and OVP Inputs for Improved Robustness
- +500 mA / −800 mA Peak Current Capability
- Up to 28 V V_{CC} Operation
- Improved Creepage Distance between High−voltage and Adjacent Pin
- Extremely Low No−load Standby Power
- This is a Pb−Free Device
- This Device uses Halogen−Free Molding Compound

Typical Applications

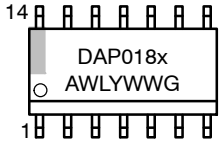
- High Power ac−dc Converters for TVs, Set−top Boxes etc.
- Offline Adapters for Notebooks



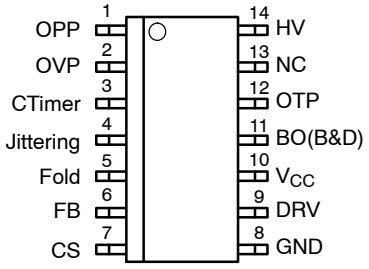
SOIC−14
D SUFFIX
CASE 751A

MARKING DIAGRAM

x	= Device Version
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

July, 2009 − Rev. 0

Publication Order Number:
DAP018/D

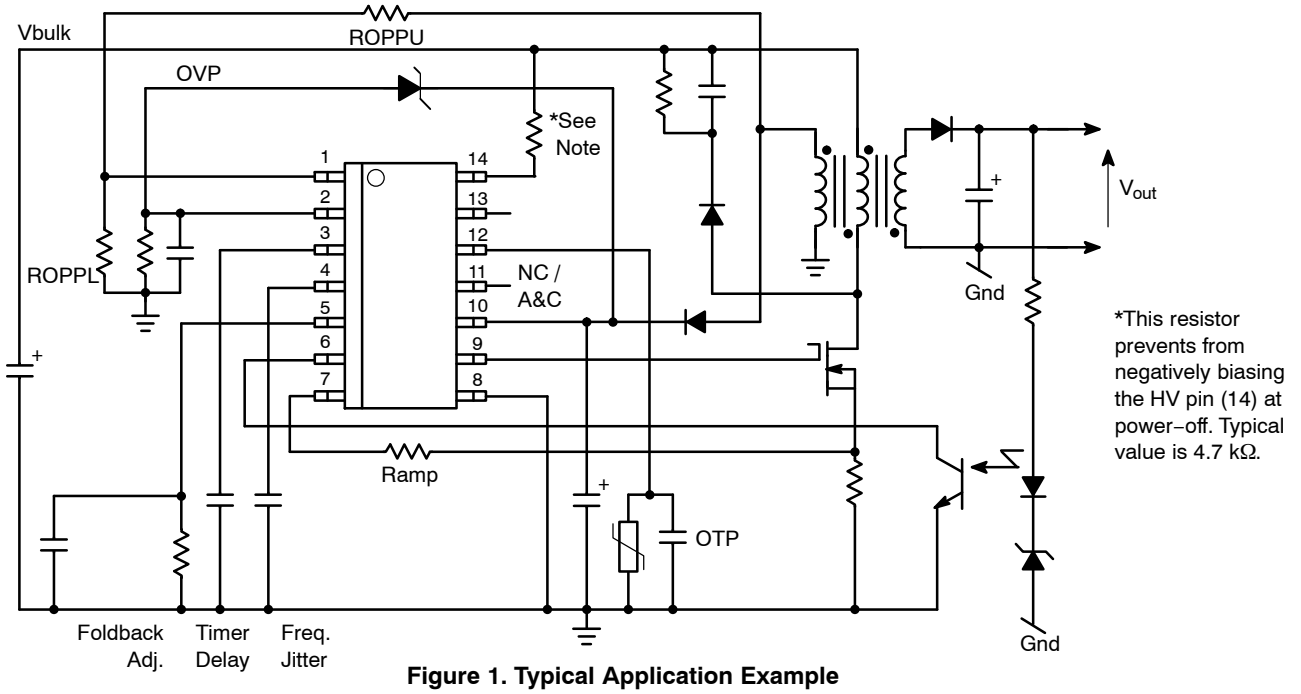


Figure 1. Typical Application Example

Pin No.	Pin Name	Function	Pin Description
1	OPP	Adjust the Over Power Protection	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level.
2	OVP	Input voltage to latch comparator	This pin offers an over−voltage protection input.
3	CTimer	Timer	Wiring a capacitor to ground helps selecting the timer duration.
4	Jitter	Frequency jittering speed	This pin offers a way to adjust the frequency modulation pace.
5	Foldback / skip	Frequency foldback / skip cycle adjustment	By connecting a resistor to ground, it becomes possible to reduce the level at which frequency foldback occurs.
6	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
7	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a means to introduce ramp compensation.
8	GND	−	The controller ground.
9	DRV	Driver output	The driver's output to an external MOSFET gate.
10	V_{CC}	Supplies the controller	This pin is connected to an external auxiliary voltage.
11	BO	Brown−out, B and D versions	For B and D versions, this pin offers a brown−out input.
12	OTP	NTC connection	This pin connects to a pulldown NTC resistor for over temperature protection (OTP).
13	NC	−	Non−connected for improved creepage.
14	HV	High−voltage input	Connected to the bulk capacitor, this pin powers the internal current source to deliver a startup current.

ORDERING INFORMATION

Delta Device	ON Semiconductor Device	Frequency	Brown–Out	Short–Circuit	Package	Shipping†
DAP018ADR2G	SCY99079ADR2G	65 kHz	No	Auto–Recovery	SOIC–14 (Pb–Free)	2500 / Tape & Reel
DAP018BDR2G	SCY99079BDR2G	65 kHz	Yes	Auto–Recovery	SOIC–14 (Pb–Free)	2500 / Tape & Reel
DAP018CDR2G	SCY99079CDR2G	100 kHz	No	Auto–Recovery	SOIC–14 (Pb–Free)	2500 / Tape & Reel
DAP018DDR2G	SCY99079DDR2G	100 kHz	Yes	Auto–Recovery	SOIC–14 (Pb–Free)	2500 / Tape & Reel
DAP018FDR2G	SCY99079FDR2G	65 kHz	Yes	Latched	SOIC–14 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

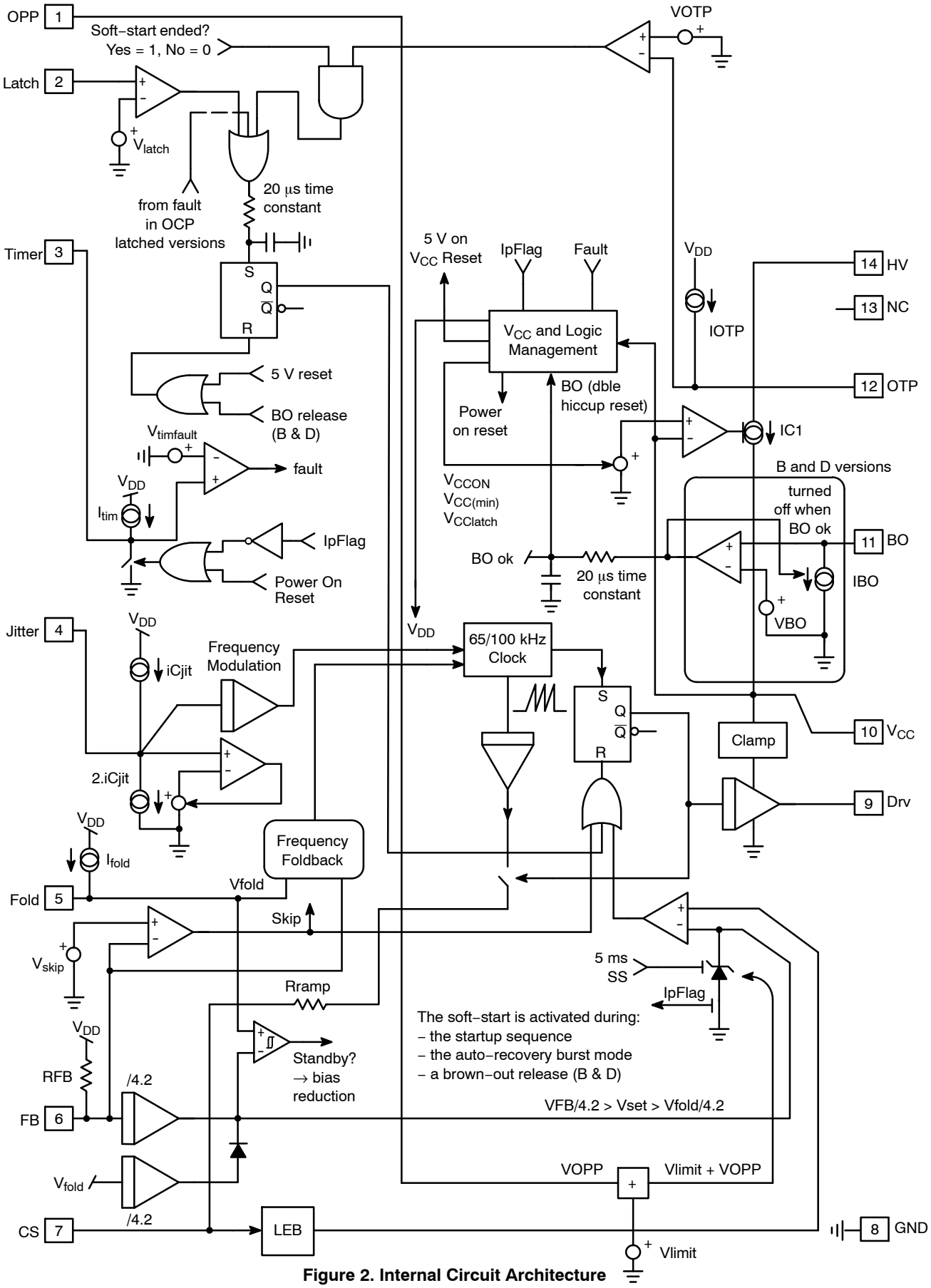


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{CCmax}	Maximum Power Supply Voltage, V_{CC} Pin, Continuous Voltage	−0.3 to 28	V
I_{CCmax}	Maximum Current for V_{CC} Pin	±30	mA
	Maximum Voltage on Low Power Pins (Except Pins 9, 10 and 14)	−0.3 to 10	V
IOPP	Maximum Injected Negative Current into the OPP Pin (Pin 1)	−2	mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	120	°C/W
TJ_{MAX}	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model (All pins except HV)	2	kV
	ESD Capability, Machine Model	180	V
	Maximum Voltage on Pin 14 (HV)	−0.3 to 500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTES: This device(s) contains ESD protection and exceeds the following tests:
Human Body Model 2000V per JEDEC Standard JESD22−A114E
Machine Model 200V per JEDEC Standard JESD22−A115−A
This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78 except pin 12.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
V_{CC}ON	V_{CC} increasing level at which the current source turns−off	10	14	15	16	V
V_{CC}(min)	V_{CC} level below which output pulses are stopped	10	8	9	10	V
V_{CC}latch	V_{CC} decreasing level at which the latch−off phase ends	10	7.2	7.5	8.0	V
V_{CC}reset	Internal latch reset level	10		5		V
resetHyst	Minimum voltage difference between V_{CC}latch and V_{CC}reset, T_J > 0°C	−	0.8			V
V_{CC}TSD	V_{CC} voltage when the TSD is activated (Note 2)	−		6.5	7.1	V
I_{CC1}	Internal IC consumption, no output load on pin 9	10		1.9		mA
$I_{CC1light}$	ICC1 for a feedback voltage equal to Vfold (internal bias reduction)	10		1.5		mA
I_{CC2}	Internal IC consumption, 1 nF output load on pin 9	10		2.7		mA
I_{CC3}	Internal IC consumption, latch−off phase	10			0.6	mA
I_{TSD}	Current consumption in TSD mode	−		400		μA

INTERNAL START−UP CURRENT SOURCE − High−voltage pin biased to 60 Vdc.

Symbol	Rating	Pin	Min	Typ	Max	Unit
IC2	High−voltage current source, V_{CC} = 10 V	14	3	6	9	mA
IC1	High−voltage current source, V_{CC} = 0, T_J = 25°C	14	150	650	1200	μA
V_{Th}	V_{CC} transition level for IC1 to IC2 toggling point	14		0.9		V
I_{leak}	Leakage current for the high voltage source, Vpin 14 = 500 Vdc, V_{CC} = 12 V, T_J > 0°C	14	1	15	30	μA

DRIVE OUTPUT

Symbol	Rating	Pin	Min	Typ	Max	Unit
T_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of a 12 V output signal	9	−	40	−	ns

1. See characterization table for linearity over negative bias voltage.
2. Guaranteed by design.
3. The OTP parameters are selected to cope with a TTC03−474 which offers a resistance of 8.8 kΩ when heated to a temperature of 110°C.
4. The brown−out circuitry is disabled on versions A & C and operates on versions B & D.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

DRIVE OUTPUT

Symbol	Rating	Pin	Min	Typ	Max	Unit
T_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of a 12 V output signal	9	–	25	–	ns
Isource	Source current capability at V_{DRV} = 10.5 V	9	–	500	–	mA
Isink	Sink current capability at V_{DRV} = 0 V	9	–	800	–	mA
V_{DRVlow}	DRV pin level at V_{CC} close to $V_{CC(min)}$ with a 33 kΩ resistor to GND	9	7.6	–	–	V
$V_{DRVhigh}$	DRV pin level at V_{CC} = 28 V	9	10	15	17	V

CURRENT COMPARATOR

Symbol	Rating	Pin	Min	Typ	Max	Unit
I_{IB}	Input Bias Current @ 0.8 V input level on pin 7	7		0.02		μA
V_{Limit}	Maximum internal current setpoint − pin1 grounded	7	0.76	0.8	0.84	V
T_{DEL}	Propagation delay from current detection to gate off−state	7		100	150	ns
T_{LEB}	Leading Edge Blanking Duration	7		140		ns
TSS	Internal soft−start duration activated upon startup, auto−recovery and BO release for versions B & D, pin 1 grounded.	–		5		ms
IOPPo	Setpoint decrease for pin 1 biased to −300 mV (Note 1)	1		37.5		%
IOOPv	Voltage setpoint for pin 1 biased to −300 mV (Note 1)	1	0.46	0.5	0.54	V
IOPPs	Setpoint decrease for pin 1grounded	1		0		%

INTERNAL OSCILLATOR

Symbol	Rating	Pin	Min	Typ	Max	Unit
f_{OSC}	Oscillation frequency (65 kHz version, A & B)	–	60	65	70	kHz
f_{OSC}	Oscillation frequency (100 kHz version, C & D)	–	92	100	108	kHz
D_{max}	Maximum duty−cycle	–	76	80	84	%
f_{jitter}	Frequency jittering in percentage of f_{OSC}	–		±5		%
f_{swing}	Swing frequency with a 22 nF capacitor to pin 4	4		300		Hz
ICjit	Jittering modulator charging current	4		18		μA
VCjitP	Jittering capacitor peak voltage	4		2.2		V
VCjitV	Jittering capacitor valley voltage	4		0.8		V

FEEDBACK SECTION

Symbol	Rating	Pin	Min	Typ	Max	Unit
R_{up}	Internal pull−up resistor	6		20		kΩ
R_{FB}	Equivalent resistor on FB pin			16		kΩ
I_{ratio}	Pin 6 to current setpoint division ratio	–		4.2		kΩ

FREQUENCY FOLDBACK

Symbol	Rating	Pin	Min	Typ	Max	Unit
I_{fold}	Internal foldback reference current	5	8.5	10	11.5	μA
V_{fold}	Frequency folback level with a 100 kΩ resistor to ground	5		1		V
I_{skip}	Skip current in percentage of the maximum excursion, for V_{fold} = 1 V			30		%
F_{trans}	Transition frequency below which skip−cycle occurs for T_J = 25°C	–	21	25	29	kHz
V_{skip}	Skip−cycle level voltage on the feedback pin	6		320		mV

1. See characterization table for linearity over negative bias voltage.
2. Guaranteed by design.
3. The OTP parameters are selected to cope with a TTC03−474 which offers a resistance of 8.8 kΩ when heated to a temperature of 110°C.
4. The brown−out circuitry is disabled on versions A & C and operates on versions B & D.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

INTERNAL RAMP COMPENSATION

Symbol	Rating	Pin	Min	Typ	Max	Unit
V_{ramp}	Internal ramp level @ 25°C (Note 2)	7		3.0		V
R_{ramp}	Internal ramp resistance to CS pin (Note 2)	7		20		kΩ

PROTECTIONS

Symbol	Rating	Pin	Min	Typ	Max	Unit
V_{latch}	Latching level input	2	2.85	3	3.25	V
T_{latch}−del	Delay before latch confirmation	–		20		μs
V_{tim}Fault	Timer level completion	3		4.3		V
I_{tim}	Timer capacitor charging current	3		12		μA
TimerL	Timer length, Ctimer = 0.22 μF typical	3		100		ms
V_{BO}	Brown−Out level − B & D versions	11	0.95	1	1.05	V
I_{BO}	Hysteresis current, Vpin 11 < V_{BO} − B & D versions, T_J = 25°C	11	9	10	11	μA
I_{BO}	Hysteresis current, Vpin 11 < V_{BO} − B & D versions, −25°C < T_J < 25°C	11	8.6	10	11	μA
I_{BO}bias	Brown−Out input bias current − B & D versions	11		0.02		μA
T_{BO}−del	Delay before brown−out confirmation	–		20		μs
I_{OTP}	Over temperature shutdown current (Note 3)	12	101	113	124	μA
V_{OTP}	Over temperature latching voltage (Note 3)	12	0.95	1	1.05	V
TSD	Temperature shutdown	–	140			°C
TSD_hys	Temperature shutdown hysteresis	–		40		°C

1. See characterization table for linearity over negative bias voltage.
2. Guaranteed by design.
3. The OTP parameters are selected to cope with a TTC03−474 which offers a resistance of 8.8 kΩ when heated to a temperature of 110°C.
4. The brown−out circuitry is disabled on versions A & C and operates on versions B & D.

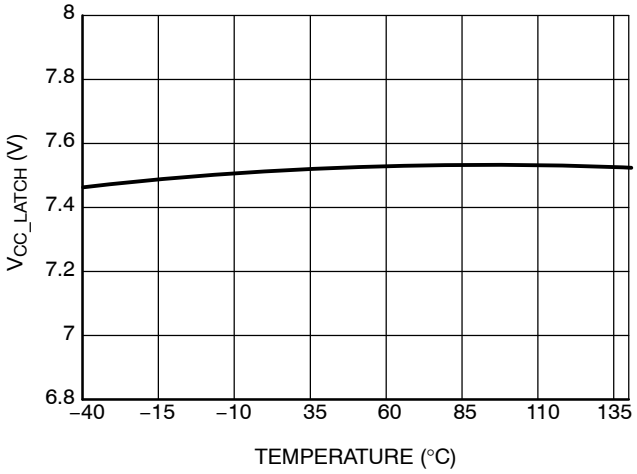


Figure 3. V_{CC_LATCH} vs. Temperature

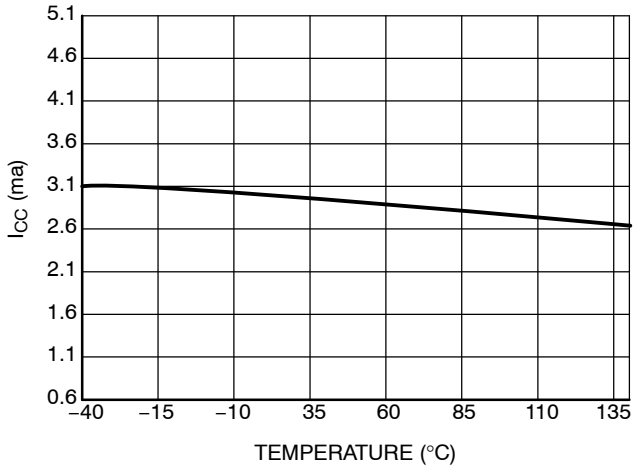


Figure 4. I_{CC2} vs. Temperature

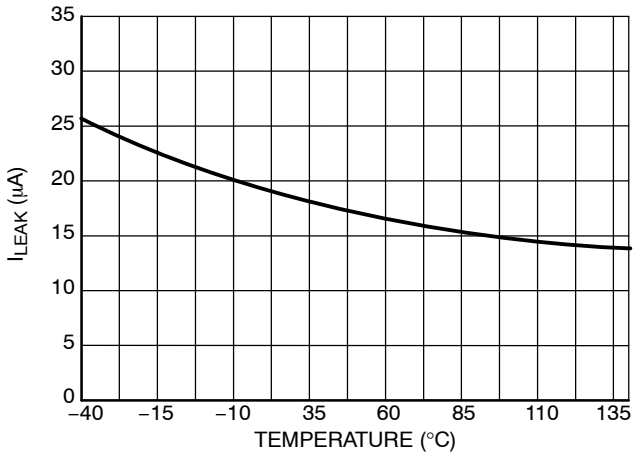


Figure 5. High−Voltage Leakage Curren vs. Temperature

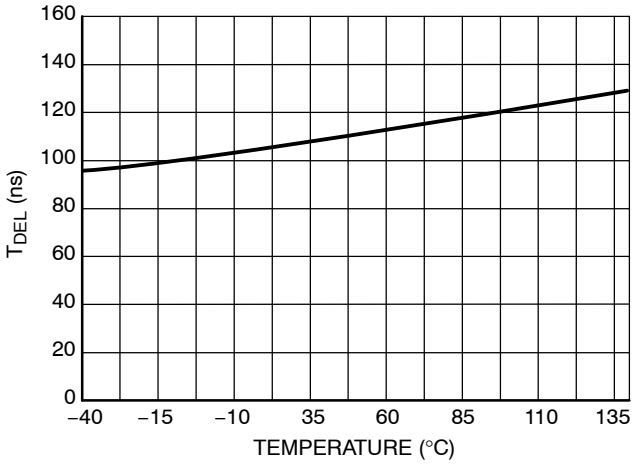


Figure 6. Propagation Delay vs. Temperature

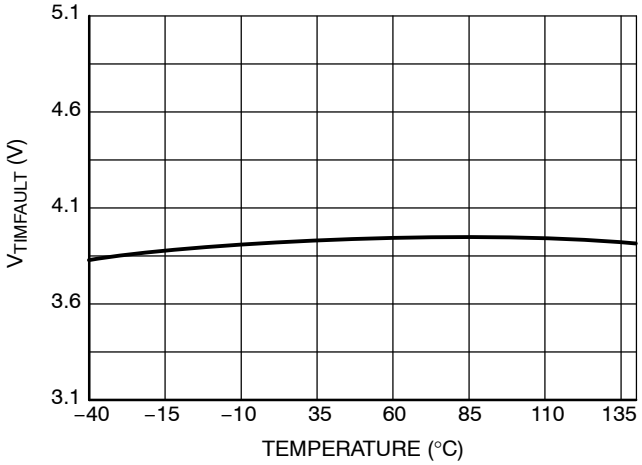


Figure 7. Fault Timer Level vs. Temperature

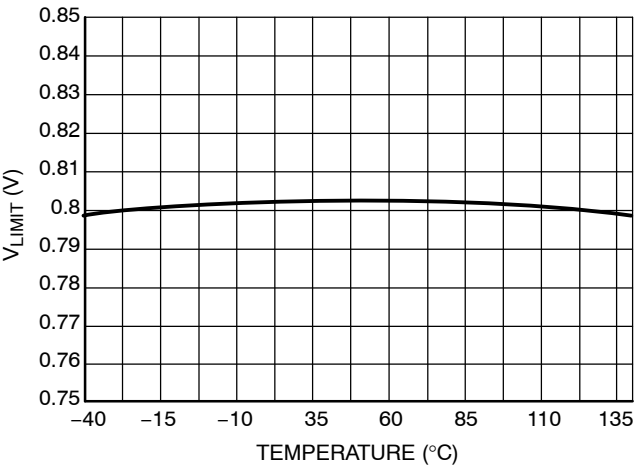


Figure 8. Current Sense Internal Setpoint vs. Temperature

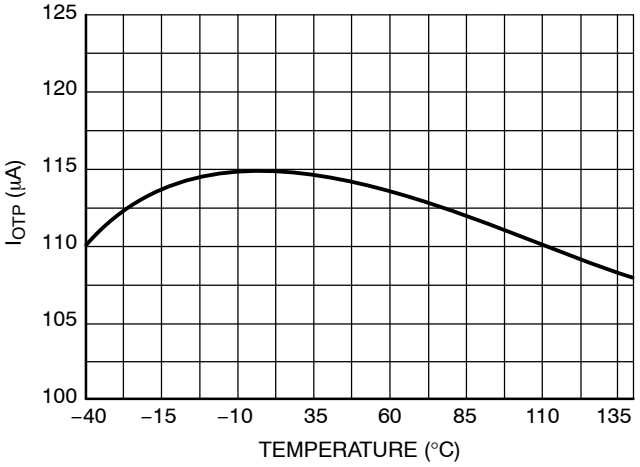


Figure 9. OTP Current vs. Temperature

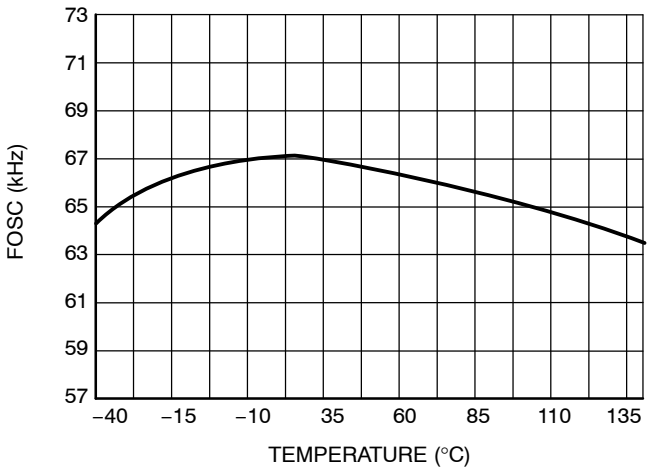


Figure 10. Oscillator Frequency vs. Temperature

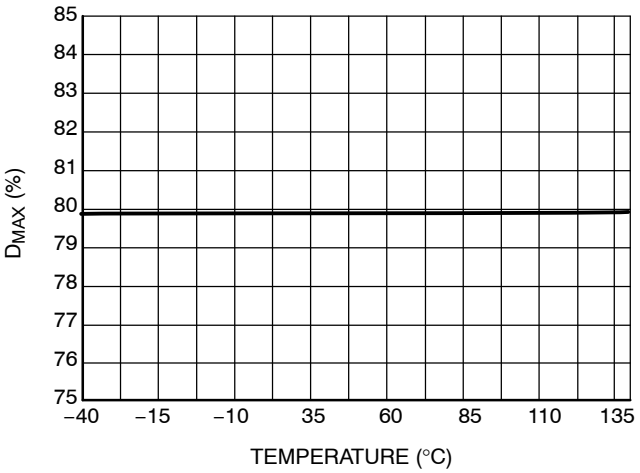


Figure 11. Maximum Duty−Cycle vs. Temperature

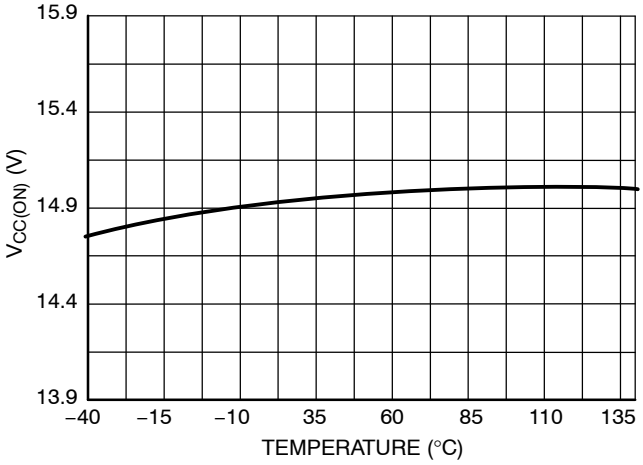


Figure 12. $V_{CC(ON)}$ Voltage vs Temperature

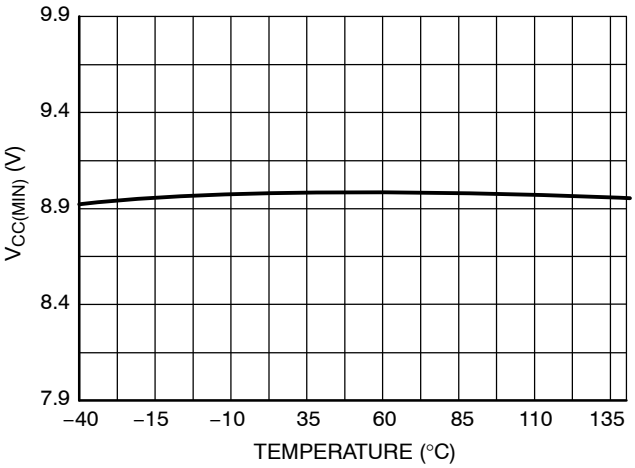


Figure 13. $V_{CC(MIN)}$ Voltage vs Temperature

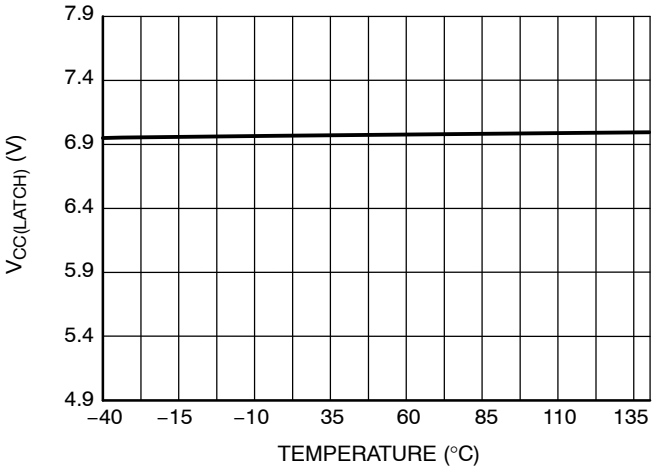


Figure 14. $V_{CC(LATCH)}$ vs Temperature

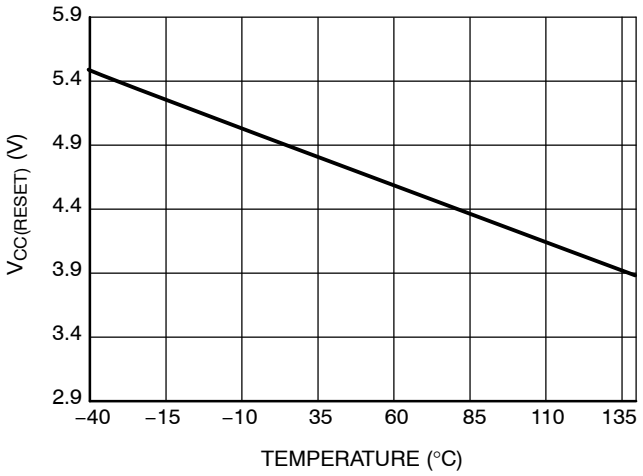


Figure 15. $V_{CC(RESET)}$ vs Temperature

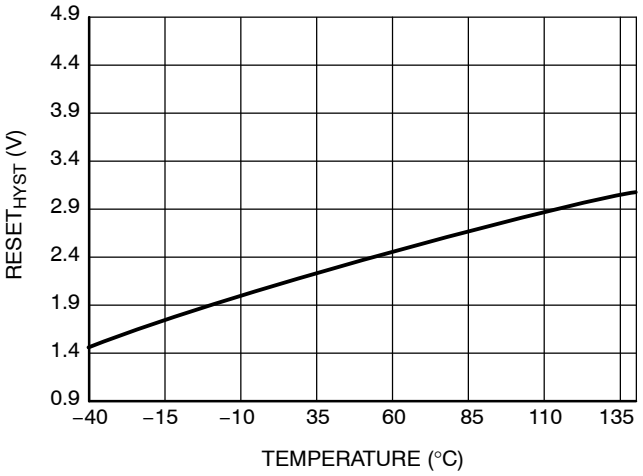


Figure 16. $V_{CC(LATCH)}$−VCC_{HYST} vs Temperature

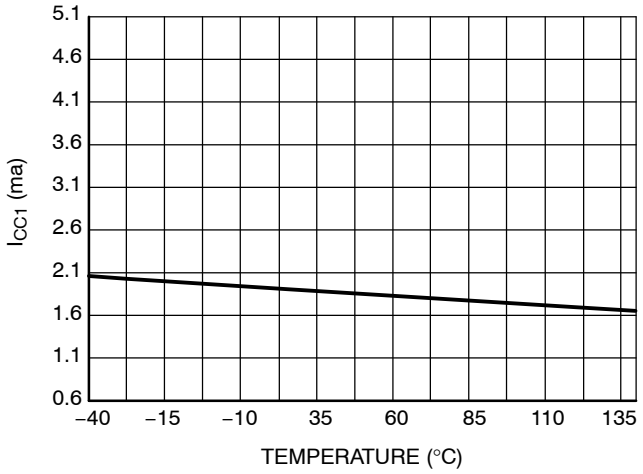


Figure 17. I_{CC1} vs Temperature

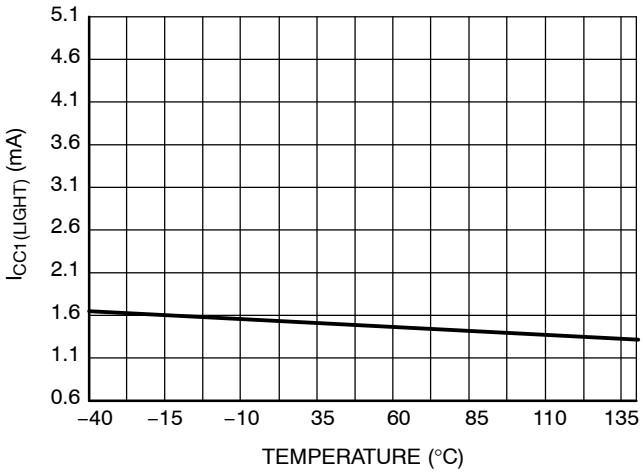


Figure 18. $I_{CC1(LIGHT)}$ vs Temperature

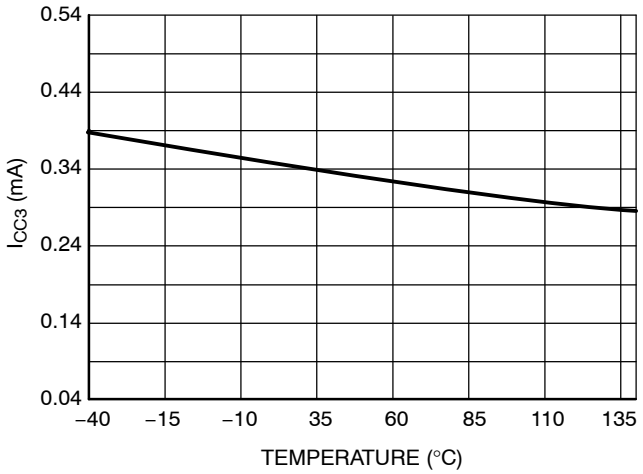


Figure 19. I_{CC3} vs Temperature

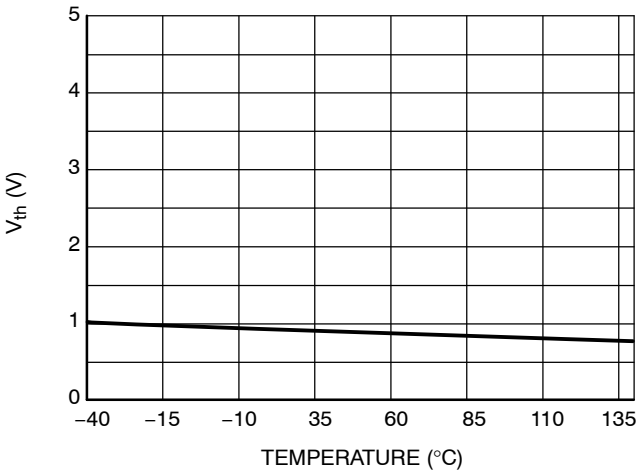


Figure 20. Threshold Voltage vs Temperature

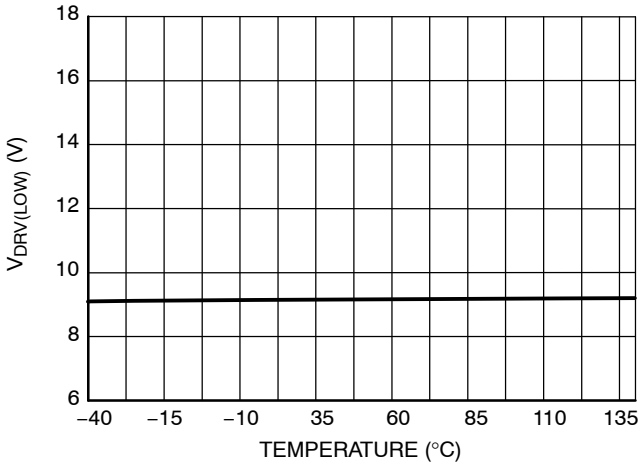


Figure 21. $V_{DRV(LOW)}$ vs Temperature

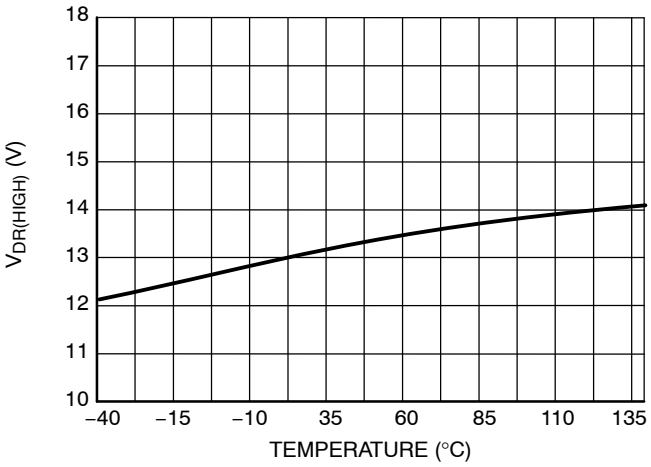


Figure 22. Drive Voltage $V_{DRV(HIGH)}$ vs Temperature

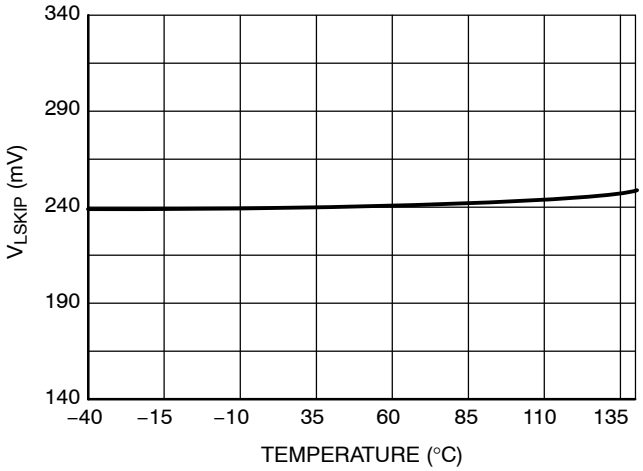


Figure 23. Skip Level vs. Temperature

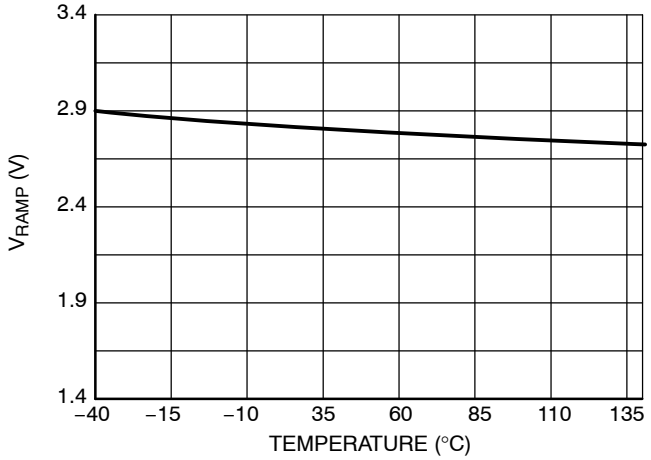


Figure 24. Ramp Level vs. Temperature

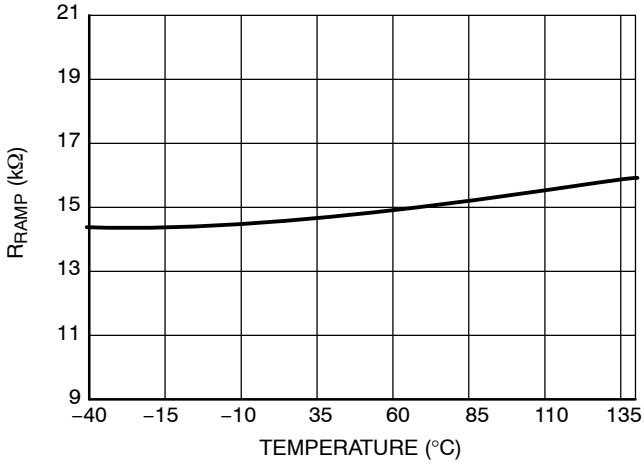


Figure 25. Ramp Resistor Value vs. Temperature

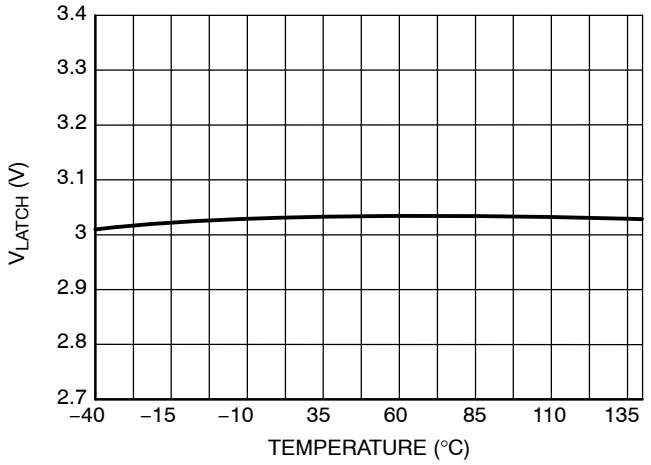


Figure 26. Latching Level vs. Temperature

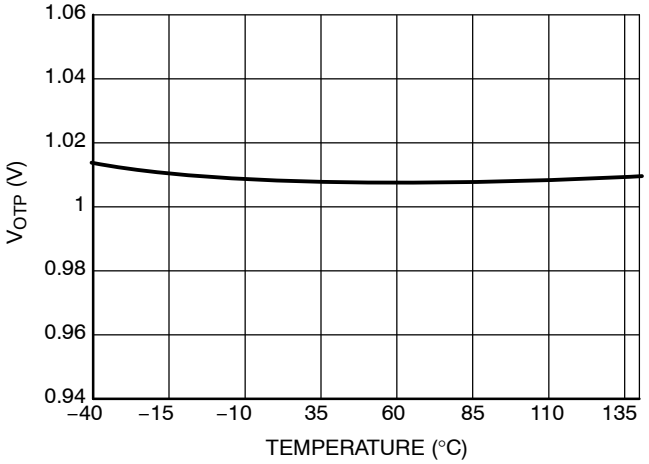


Figure 27. V_{OTP} Voltage vs. Temperature

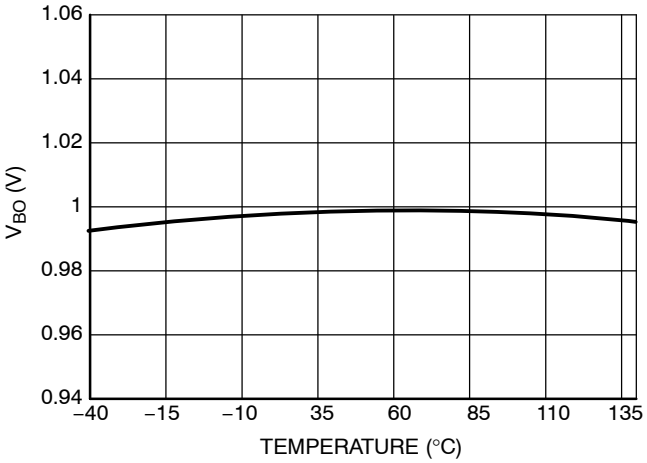


Figure 28. Brown−out Level vs. Temperature

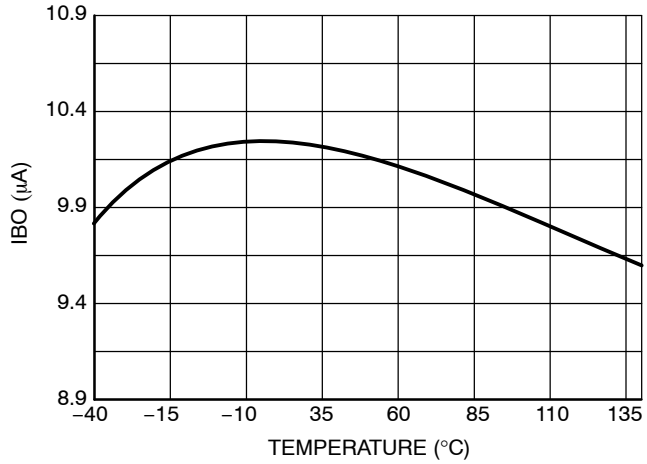


Figure 29. Brown−out Hysteresis Current vs. Temperature

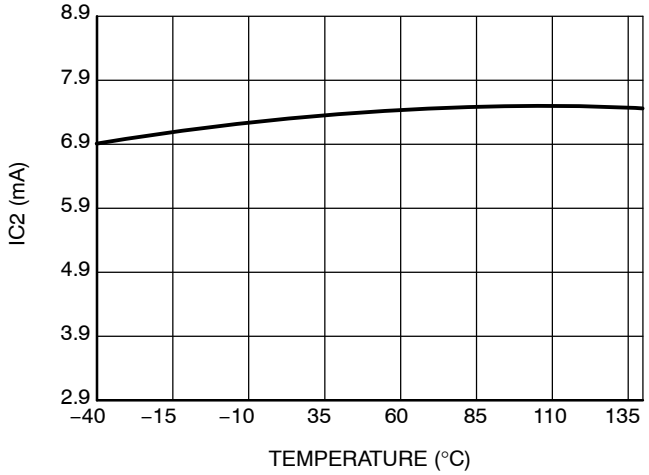


Figure 30. IC2 Startup Current vs. Temperature

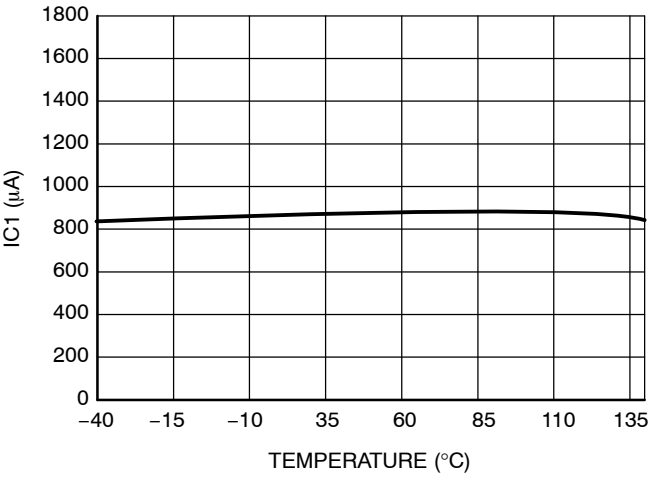


Figure 31. IC1 Startup Current vs. Temperature

Application Information

Introduction

SpeedKing II implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost ac−dc adapters, open−frame power supplies etc. Thanks to its High−Voltage technology, the DAP−018X incorporates all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as an adjustable EMI jittering and a fault timer...

- **Current−mode operation with internal ramp compensation:** implementing peak current mode control, the DAP−018X offers an internal ramp compensation signal that can easily by summed up to the sensed current. Subharmonic oscillations can thus be fought via the inclusion of a simple resistor in series with the current−sense information.
- **Internal OPP:** by routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin, the user has a simple and non−dissipative option to alter the maximum peak current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage down to –300 mV, then a peak current reduction down to 40% typical can be achieved. For an improved performance, the maximum voltage excursion on the sense resistor is limited to 0.8 V.
- **Internal high−voltage startup switch:** reaching a low no−load standby power represents a difficult exercise when the controller requires an external, lossy, resistor connected to the bulk capacitor. Thanks to an internal logic, the controller disables the high−voltage current source after startup which no longer hampers the consumption in no−load situations.
- **EMI jittering:** a dedicated pin offers the ability to vary the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To avoid modulation conflicts, the jittering will be disabled as soon as the controller enters frequency folback (light load conditions).
- **Frequency foldback capability:** a continuous flow of pulses in not compatible with no−load standby power requirements. The controller observes the feedback pin and when it reaches a level determined by pin 5, the peak current freezes. The oscillator then starts to reduce its switching frequency as the feedback level continues to decrease. It can decrease down to 26 kHz (typical). At this point, if the power continues to drop, the controller enters classical skip−cycle mode at a peak current set by pin 5 level. The point at which the foldback occurs can be adjusted to any level, we recommend to put it in the vicinity of 1 V or slightly above.
- **Bias reduction:** the controller detects that standby mode is entered by monitoring the feedback pin level. When this occurs, the circuit significantly reduces its bias current by shutting down un−necessary blocks. This improves the standby power further.
- **Brown−out:** versions B & D include a brown−out (BO) detector. When the voltage sensed on this pin is below the BO level, the controller does not operate. When the voltage reaches the threshold, the controller pulses and open the internal hysteresis current source. By connecting a divider network between the bulk voltage and the BO pin, the designer has the flexibility to adjust the turn−on and turn−off levels. For versions A & C, the brown−out circuitry is disabled and pin 11 is not internally connected.
- **Internal soft−start:** a soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is internally fixed to 5 ms. The soft−start is activated when a) a new startup sequence occurs – fresh startup or during an auto−recovery hiccup b) when the controller recovers from a brown−out condition (B & D versions).
- **OVP input:** the Speedking II includes a latch input that can be used to sense an overvoltage condition on the adapter. If this pin is brought higher than the internal reference voltage V_{latch}, then the circuit permanently latches off. The V_{CC} pin swings up and down, keeping the controller latched. The latch reset occurs when a) the user disconnects the adapter from the mains and lets the V_{CC} falls below the $V_{CCreset}$ value b) for versions B & D, if the internal BO circuitry senses a bulk / mains reset, then the controller is also reset. In this case, if the controller is within a hiccup cycle: the hiccup cycle is immediately reset and driving pulses only re−appear on the output when V_{CC} reaches $V_{CC(on)}$.
- **OTP input:** the controller incorporates an Over Temperature Protection circuitry (OTP) which allows the direct connection of a Negative Temperature Coefficient (NTC) sensor from pin 12 to GND. When the temperature increases, the NTC resistor falls down. When the NTC reaches a 8.8 kΩ value (T = 110°C), the voltage developed across its terminal is V_{OTP}. The internal comparator trips and latches−off the part. Reset occurs in similar conditions as described in the OVP section.
- **Short−circuit protection:** short−circuit and especially over−load protection are difficult to implement when a strong leakage inductance between auxiliary and power

windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8 V maximum peak current limit is activated, an error flag, IpFlag, is asserted and a time period starts, thanks to an adjustable timer. If the timer reaches completion while the error flag is still present, the controller stops the pulses and goes into a latch−off phase, operating in a low−frequency burst−mode. To limit the fault output power, a divide−by−two circuitry is installed on the V_{CC} pin and requires twice a start−up sequence before another attempt to re−start is. As soon as the fault disappears, the SMPS resumes operation. The latch−off phase can also be initiated, more classically, when V_{CC} drops below $V_{CC(min)}$ (7.9 V typical).

Start−up Sequence

When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level (typically 15 V), the current source turns off, reducing the amount of power being dissipated. At this time, the V_{CC} capacitor only supplies the controller, and the auxiliary supply should take over before V_{CC} collapses below $V_{CC(min)}$. Figure 32 shows the internal arrangement of this structure:

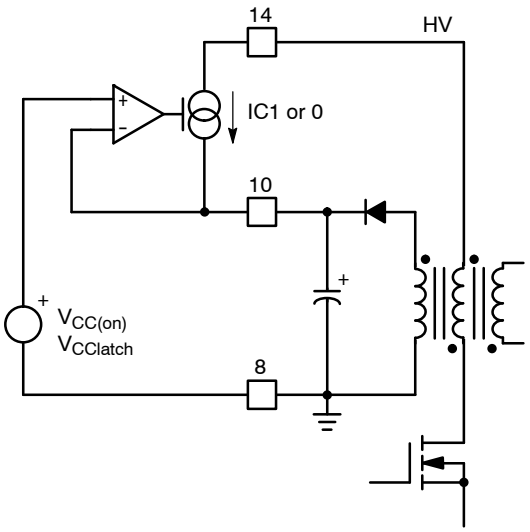


Figure 32. The Current Source Brings V_{CC} Above 15 V (typical) and then Turns Off

In some fault situations, a short−circuit can purposely occur between V_{CC} and ground. In high line conditions (V_{HV} = 370 Vdc) the current delivered by the startup device will seriously increase the junction temperature. For instance, since IC1 equals 2 mA (the min corresponds to the highest T_J), the device would dissipate 370 x 2m = 740 mW. To avoid this situation, the controller includes a novel circuitry made of two startup levels, IC1 and IC2. At power−up, as long as V_{CC} is below a certain level (1.8 V typ.), the source delivers IC1 (around 500 μA typical), then, when V_{CC} reaches 1.8 V, the source smoothly transitions to IC2 and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND, the power dissipation will drop to 370 x 500 μ = 185 mW. Figure 33 portrays this particular behaviour:

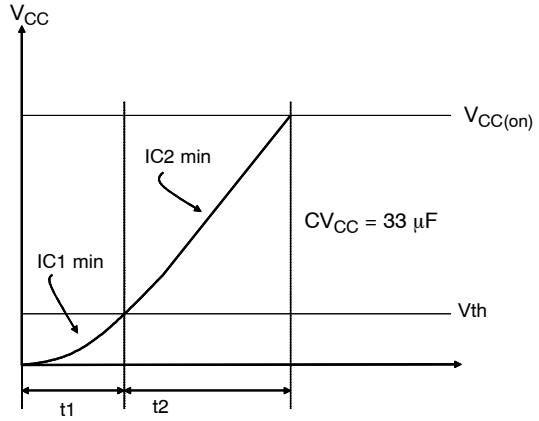


Figure 33. The Startup Source Now Features a Dual−level Startup Current

The first startup period is calculated by the formula C x V = I x t, which implies a 22 μ x 1.8 / 200 μ = 198 ms startup time for the first sequence. The second sequence is obtained by changing to 2 mA with a delta V of $V_{CC(on)} - V_{Th}$ = 15 – 1.8 = 13.2 V, which finally leads to a second startup time of 13.2 x 22 μ / 2m = 145 ms. The total startup time becomes 198 m + 140 m = 343 ms with a worst case condition on the startup source only. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

As soon as V_{CC} reaches $V_{CC(on)}$, drive pulses are delivered on pin 9 and the auxiliary winding increases the voltage on the V_{CC} pin. Because the output voltage is below the target (the SMPS is starting up), the controller smoothly ramps up the peak current to $I_{p,max}$ (0.8 V / R_{sense}) which is reached after a typical soft−start period. This soft−start period is internally fixed and lasts typically 5 ms. As soon as the peak current setpoint reaches its maximum (during the startup period but also anytime an overload occurs), an internal error flag is asserted, Ipflag, indicating that the system has reached its maximum current limit set point (I_p = $I_{p,max}$). As soon as the error flag gets asserted, the current source on pin 3 is activated and charges up the capacitor connected to this pin. If the error flag is still asserted when the timer capacitor has reached the threshold level V_{tim}Fault, (which is about 100 ms with a 0.22 μF typically), then the controller assumes that the power supply has really undergone a fault condition and immediately stops all pulses to enter a safe burst operation. Figure 34 depicts the V_{CC} evolution during a proper startup sequence, showing the state of the internal error flag:

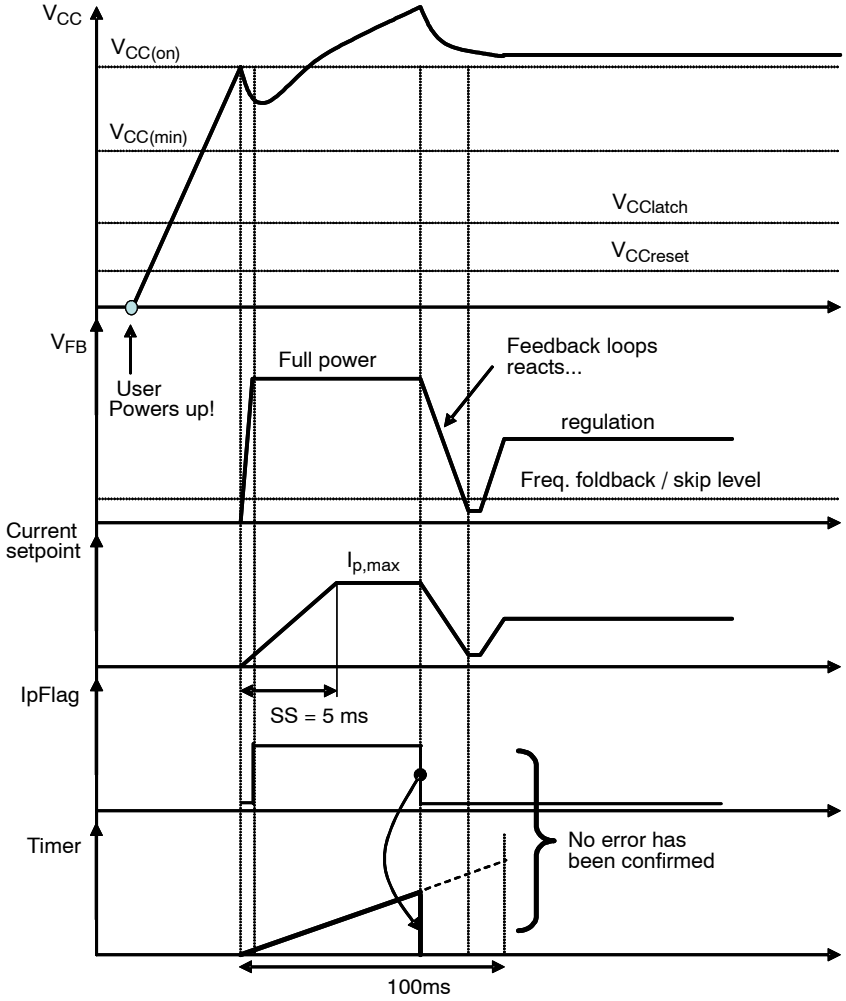


Figure 34. An Error Flag gets Asserted

An error flag gets asserted as soon as the current setpoint reaches its upper limit (0.8 V/R_{sense}). Here the timer lasts 100 ms, a 0.22 μF capacitor being connected to pin 3.

Short−circuit or Overload Mode

There can be various events that force a fault on the primary side controller. We can split them in different situation, each having a particular configuration:

1. the converter regulates but the auxiliary winding collapses: this is a typical situation linked to the usage of a constant−current / constant−voltage (CC−CV) type of secondary−side controller. If the output current increases, the voltage feedback loop gives up and the current loop takes over. It means that Vout goes low but the feedback loop is still closed because of the output current monitoring. Therefore, seen from the primary side, there is no fault. However, there are numerous charger applications where the output voltage shall not go below a certain limit, even if the current is controlled. To cope with this situation, the controller features a precise under−voltage lockout comparator biased to a $V_{CC(min)}$ level. When this level is crossed, whatever the other pin conditions, pulses are stopped and the controller enters the safe hiccup mode, trying to re−start. Figure 35 shows how the converter will behave in this situation. If the fault goes away, the SMPS resumes operation.

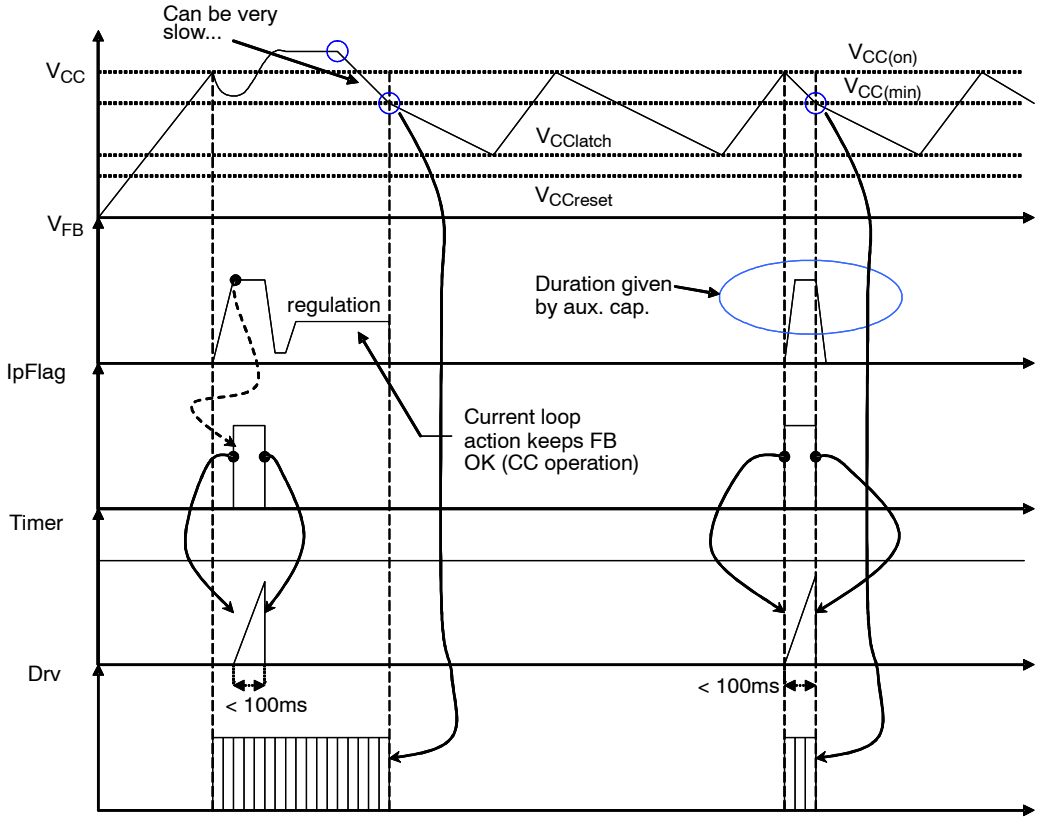


Figure 35. First Fault Mode Case

First fault mode case, the auxiliary winding collapses but feedback is still there (0.22 μF timer capacitor)

2. In the second case, the converter operates in regulation, but the output is severely overloaded. However, due to the bad coupling between the power and the auxiliary windings, the controller V_{CC} does not go low. The peak current is pushed to the maximum and the timer starts to count. Upon completion, all pulses are stopped and dual−startup hiccup mode is entered. If the fault goes away, the SMPS resumes operation.

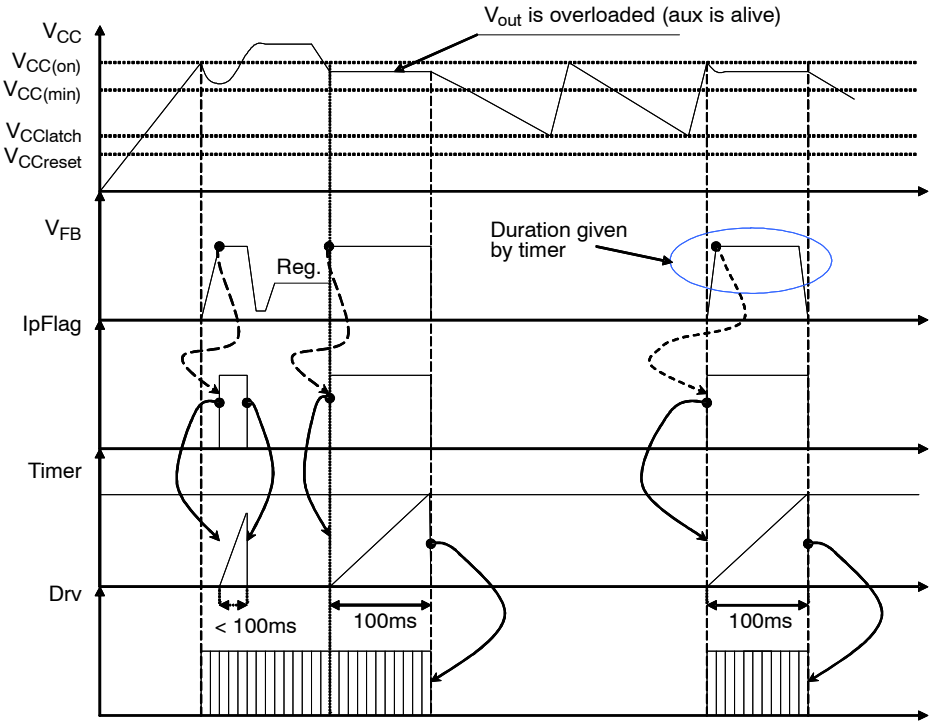


Figure 36. This Case is Similar to a Short−circuit where V_{aux} does NOT Collapse

3. A third case exists where the short−circuit makes the auxiliary level go below $V_{CC(min)}$. In that case, the timer length is truncated and all pulses are stopped. The double hiccup fault mode is entered and the SMPS tries to re−start. When the fault is removed, the SMPS resumes operation.

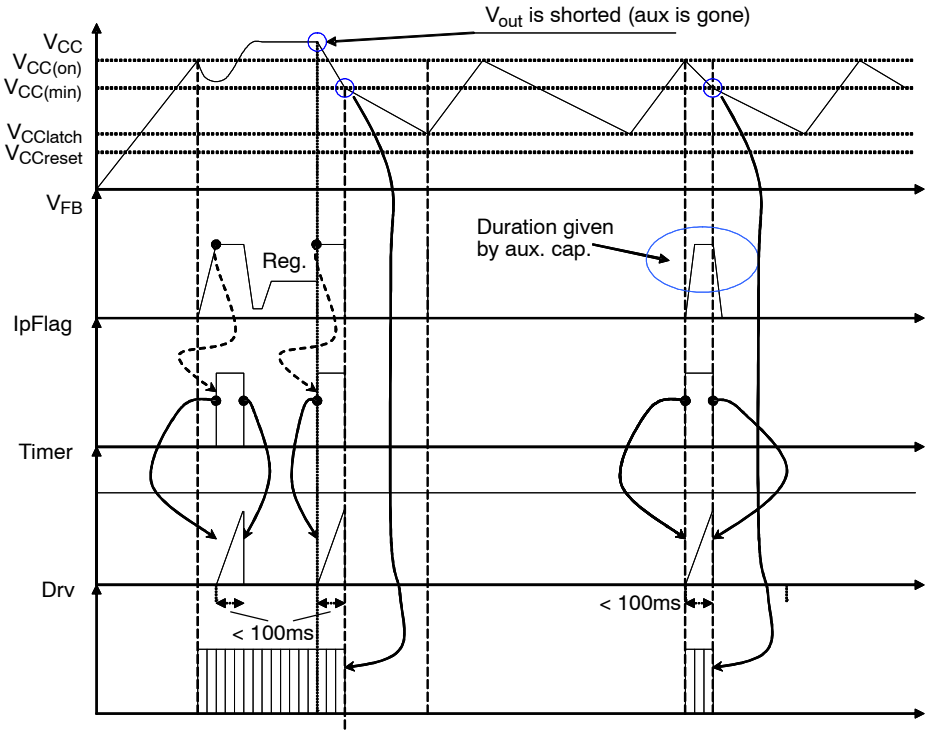


Figure 37. This Case is Similar to a Short−circuit where V_{aux} Does Collapse

The recurrence in hiccup mode can easily be adjusted by either reducing the timer or increasing the V_{CC} capacitor. Figure 38 details the various time portion a hiccup is made of:

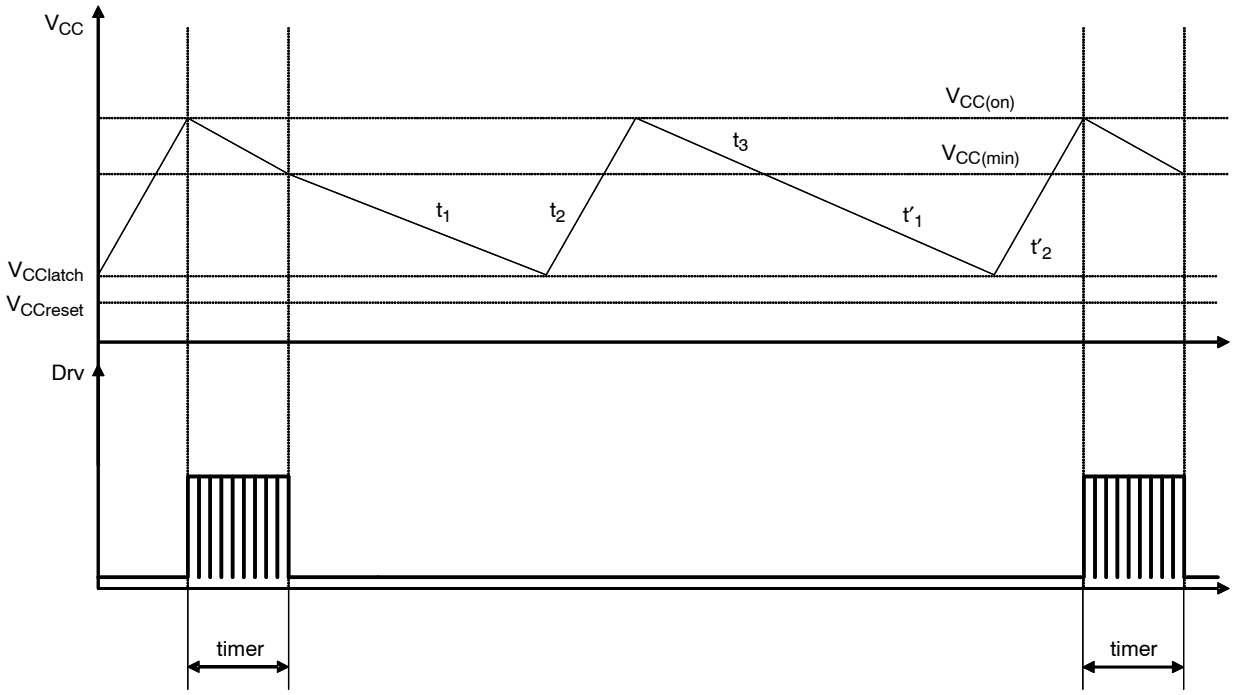


Figure 38. The Burst Period is Ensured by the V_{CC} Capacitor Charge / Discharge Cycle (here a 0.22 μF capacitor on timer)

If by design we have selected a 22 μF V_{CC} capacitor, it becomes easy to evaluate the burst period and its duty−cycle. This can be done by properly identifying all time events on Figure 38 and applying the classical formula:

$$t = \frac{C\Delta V}{I}$$

- t_1: I = ICC3 = 600 μA,
  $\Delta V = 9 - 6.5 = 2.5\ V \rightarrow t_1 = 91$ ms
- t_2: I = 3 mA, $\Delta V = 15 - 6.5 = 8.5\ V \rightarrow t_1 = 62$ ms
- t_3: I = 600 μA, $\Delta V = 15 - 6.5 = 8.5\ V \rightarrow t_1 = 311$ ms
- $t'_1 = t_1 = 91$ ms
- $t'_2 = t_2 = 62$ ms

The total period duration is thus the sum of all these events which leads to T_{fault} = 617 ms. If the timer lasts 100 ms, then our duty−cycle in auto−recovery burst equals 100/(617 + 100) ≈ 13%, which is good. Should the user like to further decrease or, to the contrary, increase this duty−cycle, changing the V_{CC} capacitor is an easy job.

Latch−off and Over Voltage Protection

Speedking II features a fast comparator that permanently monitors pin 2 level. Figure 39 details how it is internally arranged:

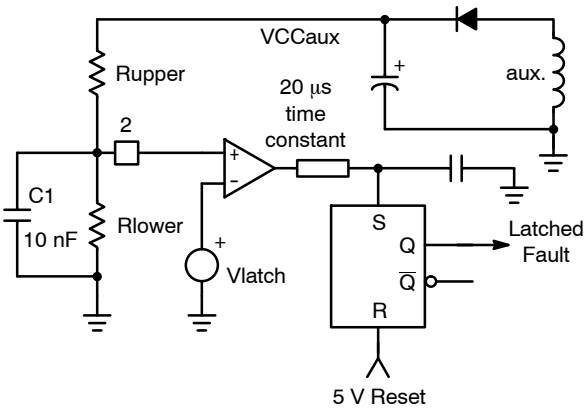


Figure 39. A Comparator Monitors Pin 2 and Latches−off the Part in Case the Threshold is Reached

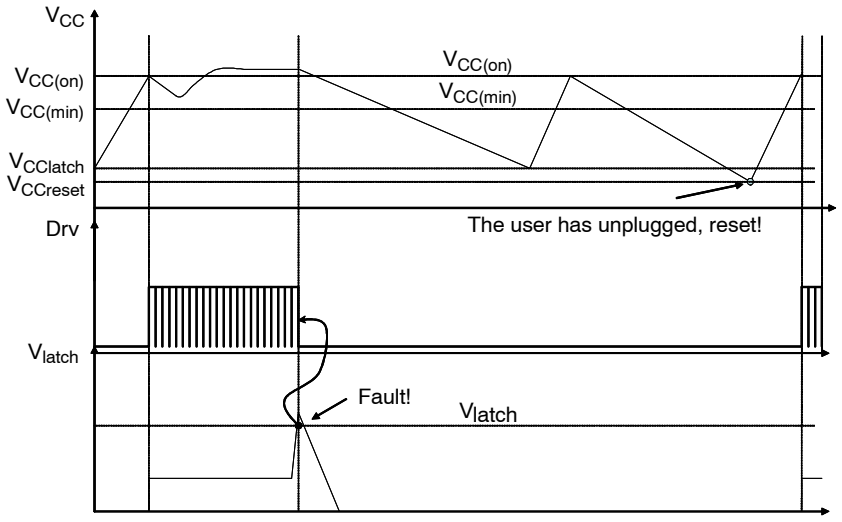


Figure 40. The Part is Reset when V_{CC} Reaches 5 V or when BO Senses the Bulk Capacitor Voltage is Back to Normal

If for any reason the latch pin level grows above V_{latch}, the part immediately stops pulsing and stays latched in this position until the user cycles down the power supply. The reset actually occurs if V_{CC} drops below 5 V, e.g. if the adapter user disconnects it from the mains. Figure 40 details the operating diagrams in case of a fault. Please note the presence of RC time constant on the comparator output, aimed to filtering any spurious oscillations linked to an eventual noise presence. The typical value of this time constant is 20 μs.

On both OVP and OTP events and in the case of a latched−OCP version, the latch reset occurs in the following conditions:

- a user reset via a mains interruption (unplug and replug adapter) which is long enough to let the V_{CC} capacitor discharge to the controller reset level of 5 V.
- for B & D versions, a reset can occur if the brown−out circuitry is asserted before the V_{CC} reaches 5 V.

Soft−start

The Speedking II features an internal soft−start circuit activated during the power on sequence (PON) but also in fault recovery (short−circuit protection or brown−out release). As soon as V_{CC} reaches $V_{CC(on)}$, the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 0.8 V/R_{sense}). The peak current is clamped at 0.8 V/R_{sense} through the entire soft−start period until the supply enters regulation. Figure 41 shows a typical startup shot.

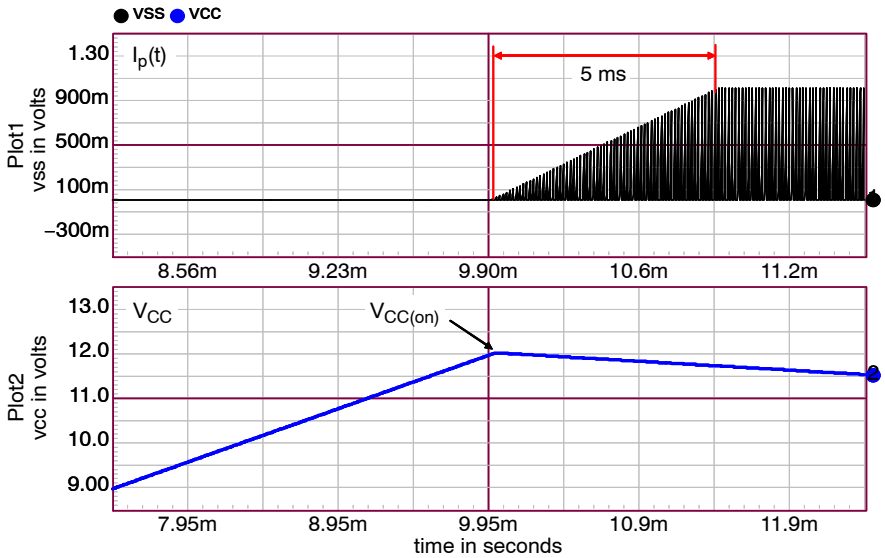


Figure 41. Soft−start is Activated During a Start−up Sequence, an Auto−recovery Burst−mode or when the Brown−out Pin is Released

The soft−start is activated in the following conditions:

- Startup sequence: when the user powers the adapter, the peak current smoothly ramps−up from a low value towards a maximum value defined by the sense resistor.
- In auto−recovery burst−mode (e.g. during a non−latched short−circuit), each new set of pulses starts with a soft−start sequence.
- When the brown−out pin senses a reset on the bulk voltage, the controller restarts via a soft−start sequence, just like a fresh power−on sequence.

* Please note that Speedking II does use implement the soft−burst technique as built in the original Speedking circuit.

Internal Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. Figure 42 depicts how internally the ramp is generated.

* Please note that the ramp signal will be disconnected from the CS pin, during the OFF time.

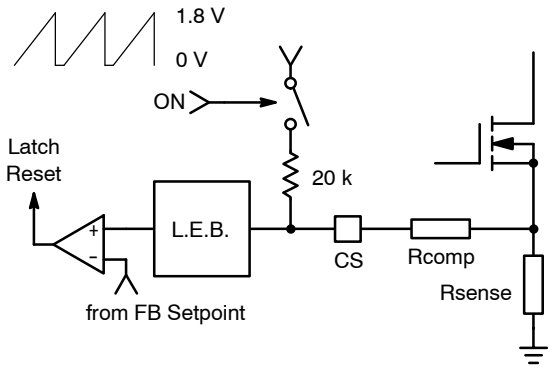


Figure 42. Inserting a Resistor

Inserting a resistor in series with the current sense information brings ramp compensation and stabilizes the converter in CCM operation.

In the Speedking II controller, the oscillator ramp features a 1.8 V swing. If our clock operates at a 65 kHz frequency, then the oscillator slope corresponds to a 120 mV/μs ramp. In our flyback design, let's assume that our primary inductance L_p is 350 μH, and the SMPS delivers 12 V with a N_p:N_s ratio of 1:0.1. The off−time primary current slope is thus given by:

$$\frac{\left(V_{out} + V_f\right) \cdot \frac{N_S}{N_P}}{L_P} = 371\ \text{mA/μs or 37 mV/μs}$$

when projected over a sense resistor R_{sense} of 0.1Ω, for instance. If we select 75% of the downslope as the required amount of ramp compensation, then we shall inject 27 mV/μs. Our internal compensation being of 120 mV/μs, the divider ratio (divratio) between R_{comp} and the 20 kΩ is 0.225. R_{comp} can therefore be obtained using the following value:

$$R_{comp} = \frac{R_{ramp} \cdot \text{divratio}}{(1 - \text{divratio})} = \frac{20\ \text{k} \times 0.225}{1 - 0.225} = 5.8\ \text{k}\Omega$$

Brown−out Protection

Versions B and D of the controller include a dedicated circuitry which permanently monitors the bulk capacitor level. Figure 43 depicts the comparator arrangement known as a brown−out protection:

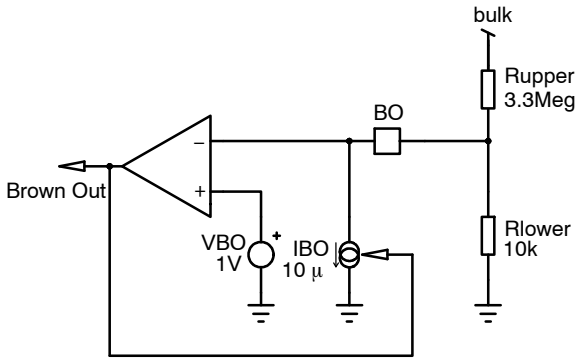


Figure 43. A Brown−out Circuit Protects the Power Supply against Low Input Voltages

When the input voltage is low, below $V_{BO(on)}$, the BO comparator output is low and the current source is activated, drawing 10 μA from the BO pin (pin 11) to ground. The controller is silent, and no driving pulses are delivered to the power MOSFET. When the input is sufficiently high, the BO comparator toggles high and shuts down the current source, providing the necessary hysteresis to the circuit. When toggling high, the BO signal also resets ALL the internal logic circuits including an eventual latch state triggered by an OVP for instance (or a latched OCP for this particular version). When the BO comparator has given the authorization to work, the controller resets its hiccup mode on the V_{CC} (if any) and waits for the next $V_{CC(on)}$ event to start pulsing again (via soft−start sequence). A 20 μs RC time−constant has been added in series with the brown−out comparator to further avoid false trigger of the controller.

Figure 44 shows typical signals in presence of a brown−out suddenly occuring and coming back again:

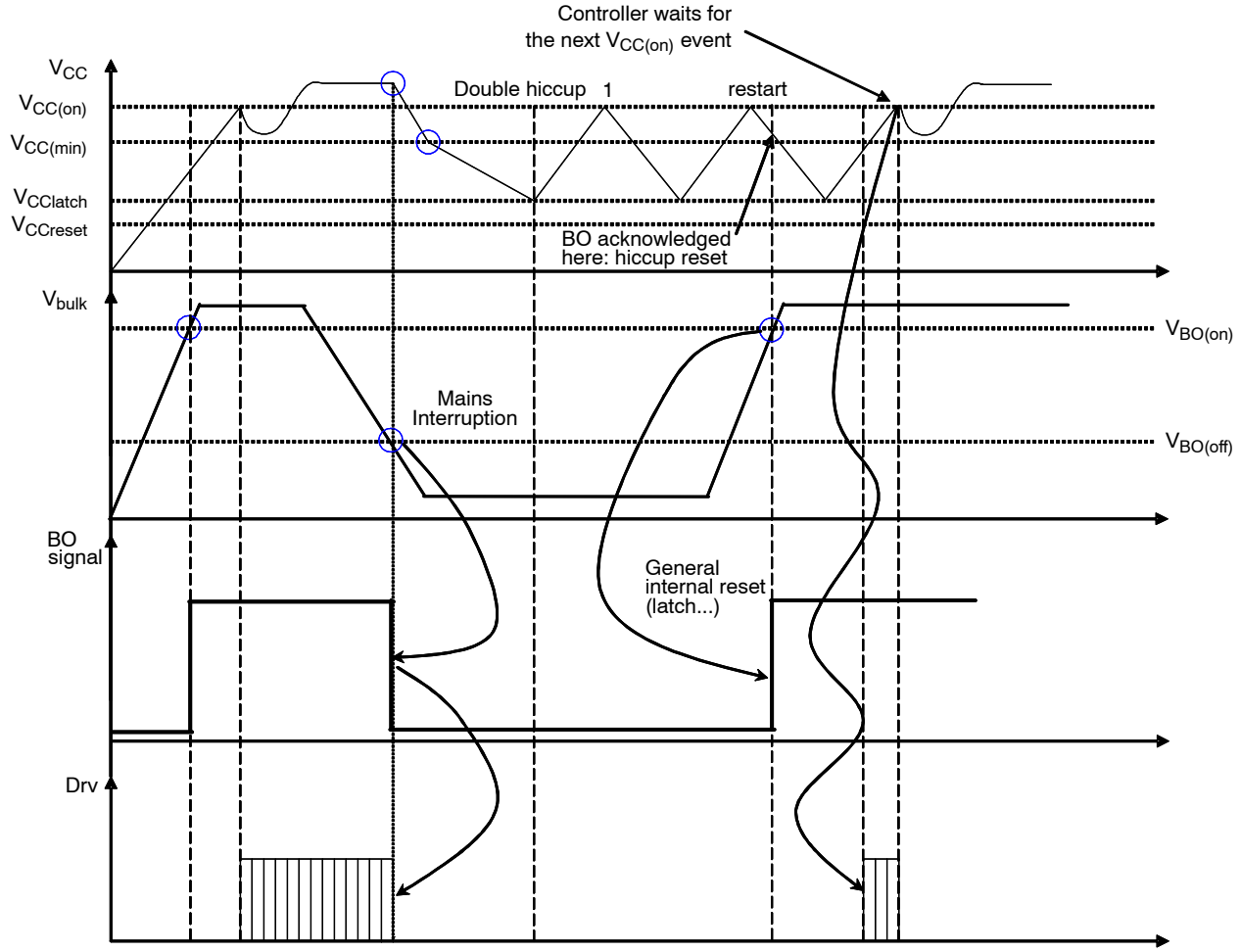


Figure 44. A Brown−out Event Immediately Stops the Driving Pulses

When the bulk comes back to its normal level, the controller waits for the next $V_{CC(on)}$ event to re−start pulsing. If the controller was in a double−hiccup mode, the logic circuit is reset to accelerate the restart to the next $V_{CC(on)}$ event.

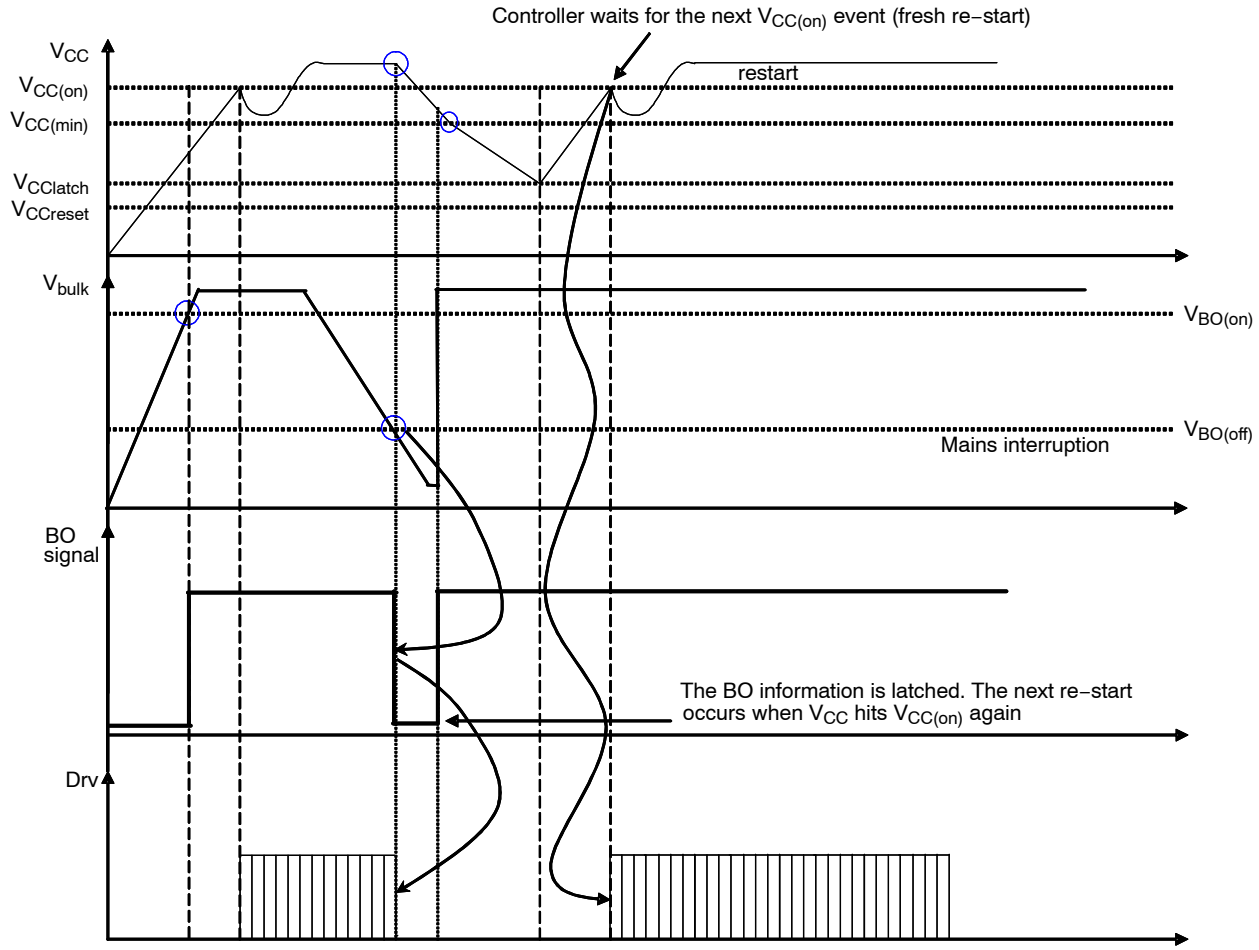


Figure 45. A Brown−out Event Immediately Stops the Driving Pulses

When the bulk comes back to its normal level, the controller waits for the next $V_{CC(on)}$ event to re−start pulsing. In this case, the BO re−appears while V_{CC} was still ok but the controller waits for V_{CC} to ramp down to $V_{CClatch}$ then performs a fresh re−start before pulsing again.

The bridge resistors can be evaluated using the following equations:

$$R_{upper} = \frac{V_{BO,on} - V_{BO,off}}{I_{BO}} \quad \text{(eq. 1)}$$

$$R_{lower} = \frac{V_{BO} R_{upper}}{V_{BO,off} - V_{BO}} \quad \text{(eq. 2)}$$

Where V_{BO} = 1 V typical and I_{BO} = 10 μA typical.

Suppose the adapter designer needs a turn−on voltage of 100 Vdc and a turn−off voltage of 50 Vdc, then the upper resistor would be 4.9 MΩ and the lower side resistor 100 kΩ. The total dissipation for a 330 Vdc bulk rail would amount to 22 mW.

* Please note that the current source arrangement brings un−precision to the turn−on voltage only, whereas the turn−off voltage is only dependent on the V_{BO} reference voltage.

Frequency Foldback and Skip Cycle

Unlike its predecessor, Speedking II implements a frequency reduction in low power mode. Also called frequency foldback, this technique has proven to offer a good performance, especially in the middle of the power range. On this controller, the foldback occurs when the peak current reaches a level set via the original skip pin (pin 5). Once the peak current reaches this value, via a decrease in the feedback voltage, the controller freezes it and the only way to further reduce the output power is to fold the frequency back. The frequency variation is ensured over a delta feedback voltage of around 500 mV. When the frequency hits the frequency limit (F_{trans}), the frequency reduction is stopped. At this point, if the load goes further down, the feedback voltage drops and when it reaches 300 mV, the controller enters traditional skip−cycle (no soft−burst).

At full power, the peak current varies according to the power demand, the switching frequency being fixed to 65 kHz. The feedback voltage is allowed to move between 300 mV and 3.4 V which is the upper feedback limit beyond which a fault is detected. When the load starts to decrease, the feedback voltage goes down to impose lower peak

currents. When the feedback pin reaches the V_{fold} level, the peak current is set to V_{fold} /4.2 and cannot decrease anymore. The feedback voltage continues to go down but it now changes the switching frequency down to 26 kHz (typical), naturally reducing the amount of transmitted power. When the feedback touches a typical 300 mV limit, skip−cycle takes place. The whole behavior is illustrated by Figure 46:

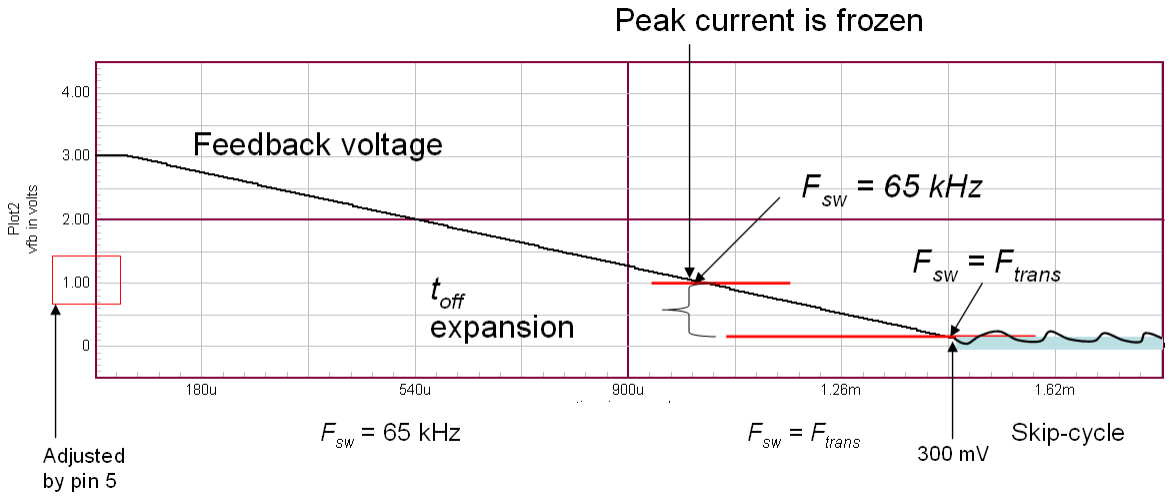


Figure 46. The Controller Changes its Operating Frequency in Light Load Conditions

Further details are given by Figure 47 which represents both switching frequency and peak current setpoints in relationship to the feedback voltage. Pin 5 provides a means to alter the foldback limit. To fine tune the efficiency but also to combine a low skip current level and a reduced acoustic noise in standby, the designer must wire a resistor to ground to set the foldback level (Figure 48). As we internally have a 10 μA current source, the relationship is straightforward:

$$R_{fold} = \frac{V_{fold}}{10\ \mu} \qquad \text{(eq. 3)}$$

For instance, suppose we want to set the folback point to 1 V, then the resistor value should be 100 kΩ. We recommend to put a 10 nF capacitor to ground on this pin. Both the resistor and the capacitor must be placed very close to the controller to avoid any noise pick−up.

Because the clock frequency must reach 26 kHz at a feedback voltage of 300 mV, pin 5 level cannot be set too low in order to provide enough dynamic range for the Voltage−Controlled Oscillator (VCO). To obtain a good linearity, we recommend a minimum voltage dynamics of 300 mV, which implies a level on pin 5 always above 600 mV. Also, setting the frequency foldback too low will alter the performance in standby power.

The graphs in Figure 47 (65 kHz version) depict the operation in light load conditions where the frequency is decreased down to 26 kHz (typical)

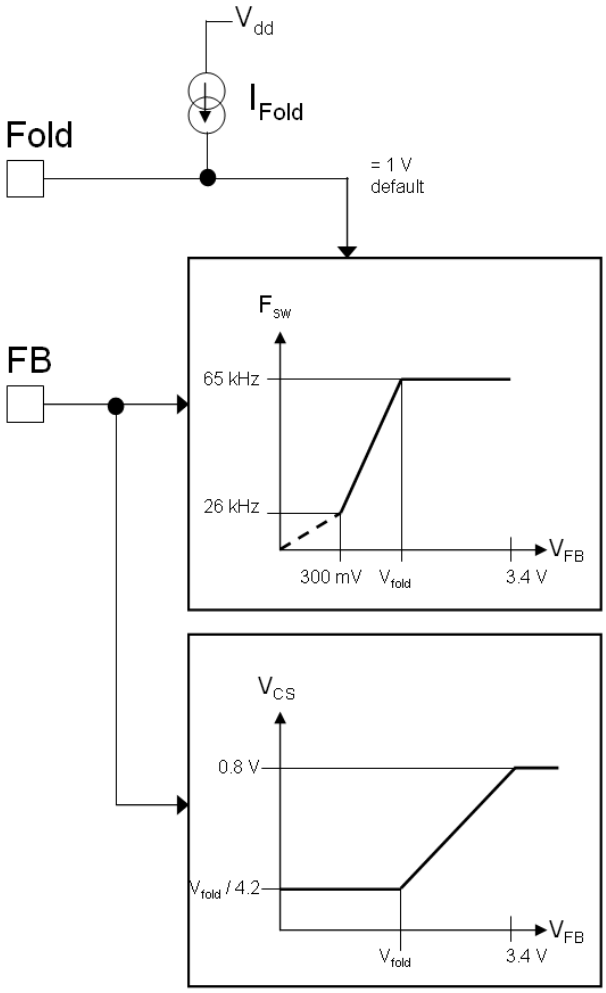


Figure 47. Operation in Light Load Conditions

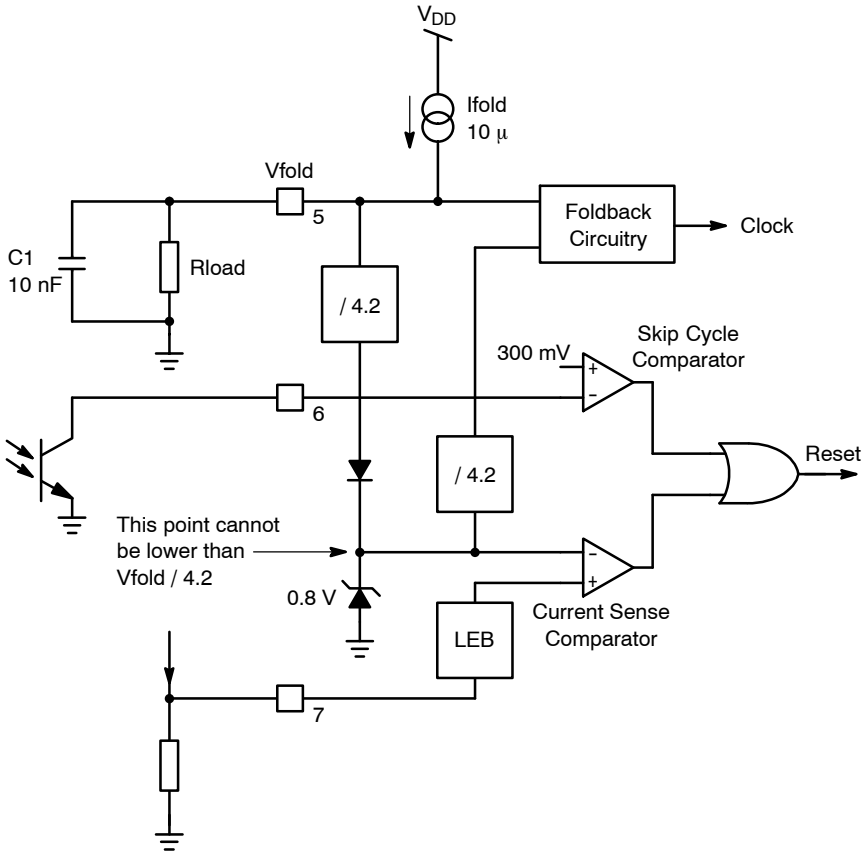


Figure 48. A Pulldown Resistor Adjusts the Foldback Level

Bias Reduction in Light Load

When the power supply enters deep standby mode (skip−cycle is active), a comparator instructs the controller that it entered in light load conditions. When this happens, the circuit reduces various internal bias currents to further bring its consumption down and improve the consumption in no−load conditions.

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. Speedking II offers a ±5% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with an adjustable period. Figure 49 displays the internal arrangement around pin 4. It is actually a I – 2I generator, producing a clean 50% duty−cycle sawtooth. If we take a 2 V swing on the jitter capacitor, then we calculate the needed value for a 4 ms period, or a 250 Hz modulation speed, again applying the V x C = I x t relationship. We need 2 ms to ramp−up and 2 ms to ramp down, therefore: C = 20 μ x 2 m / 2 = 20 nF. If we select a 22 nF, then our modulation frequency will be around 227 Hz... Figure 50 shows the relationship between the jitter ramp and the frequency deviation.

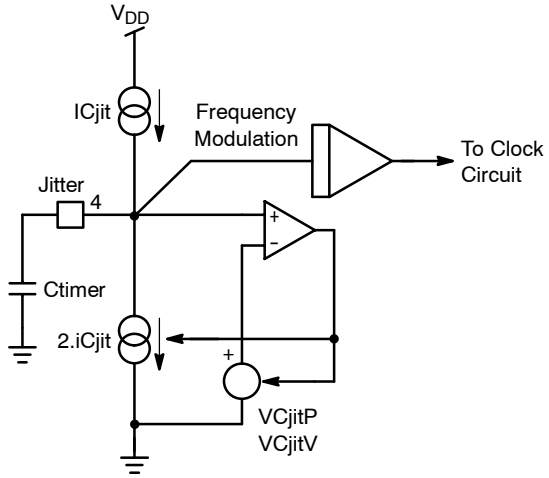


Figure 49. An Internal Ramp is Used to Introduce Frequency Jittering on the Oscillator Sawtooth

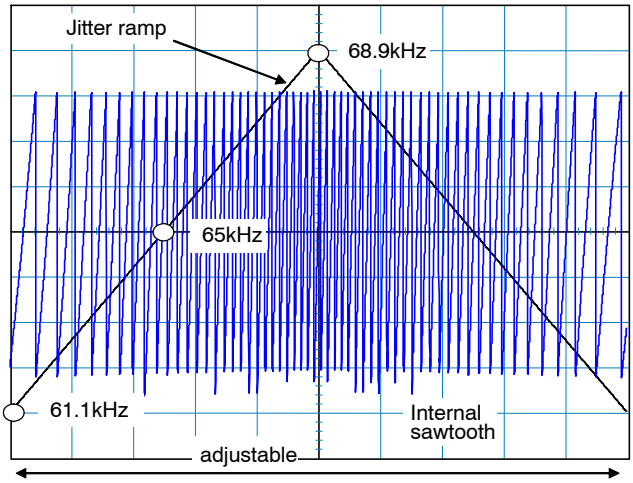


Figure 50. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is described by Figure 52. On this drawing, a voltage is derived from the auxiliary winding and produces a negative level during the on−time of the main power transistor. The negative voltage amplitude directly relates to the input level via the transformer turn ratio linking the primary winding to the auxiliary winding. Figure 51 depicts the typical signal obtained on the auxiliary winding:

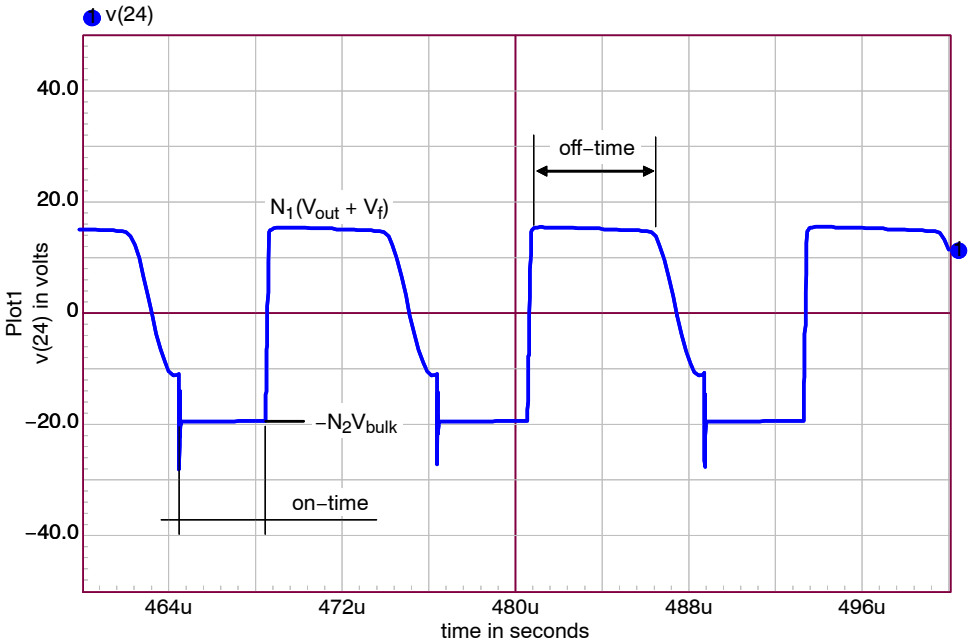


Figure 51. The Signal Obtained on the Auxiliary Winding Swings Negative During the On−time

During the off−time, the voltage plateaus to a positive level depending on the turn ratio between the output winding (N_s) and the power winding. This ratio is noted N_1. During the on−time, the transformer terminal swings to a negative voltage whose amplitude now depends on the turn ratio N_2, equal to the primary (N_p) to the auxiliary winding ratio (N_{aux}). If we place a resistive divider between the auxiliary winding and the OPP pin, as suggested by Figure 52, we have a means to influence the internal setpoint as the bulk voltage increases. The equations to design the network are fairly simple:

Suppose we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to 20% reduction or a setpoint voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 800 - 640 = -160\ mV \qquad \text{(eq. 4)}$$

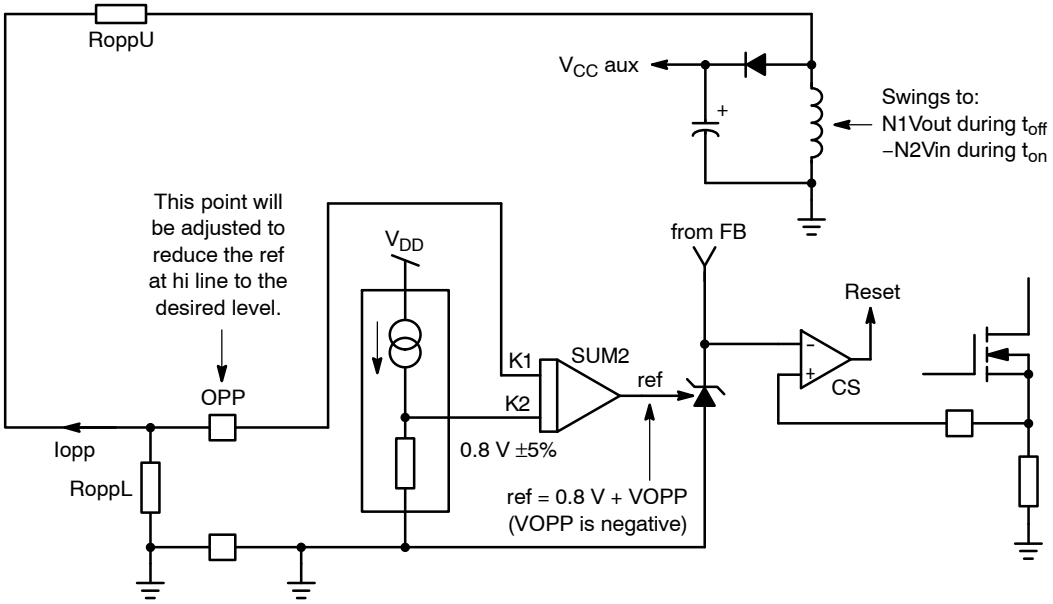


Figure 52. The OPP Circuitry Affects the Maximum Peak Current Setpoint by Summing a Negative Voltage to the Internal Voltage Reference

Let us assume that we have the following converter characteristics:

V_{out} = 19 V

V_{in} = 85 to 265 Vrms

$N_1 = N_p:N_s$ = 1:0.2

$N_2 = N_p:N_{aux}$ = 1:0.16

Given the turn ratio between the primary and the auxiliary windings, the on−time voltage at high line (265 Vac) on the auxiliary winding swings down to:

$$V_{aux} = -N_2 V_{in,max} = -0.16 \times 375 = -60\ V \quad \text{(eq. 5)}$$

To obtain a level as imposed by Equation 3, we need to install a divider featuring the following ratio:

$$Div = \frac{0.16}{60} = 0.00266 \quad \text{(eq. 6)}$$

If we arbitrarily fix the pulldown resistor R_{OPPL} to 1 kΩ, then the upper resistor can be obtained by:

$$R_{OPPU} = \frac{60 - 0.16}{0.16/1\ k} = 374\ k\Omega \quad \text{(eq. 7)}$$

If we now plot the peak current setpoint obtained by implementing the recommended resistor values, we obtain the following curve:

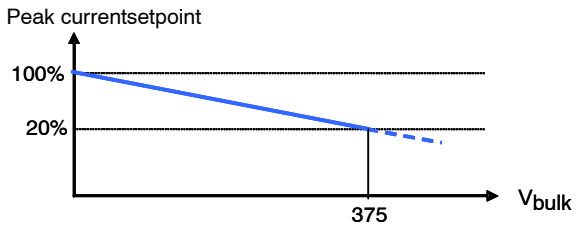


Figure 53. The Peak Current Regularly Reduces Down to 20% at 375 Vdc

The OPP pin is made of zener diodes arranged to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection wich can lead to an erratic circuit behaviour. To avoid this problem, the pin is internall clamped slightly below –300 mV which means that if more current is injected before reaching the ESR forward drop, then the maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal zener diode, then care must be taken to avoid injecting a current beyond –2 mA. Given the value of R_{OPPU}, there is no risk in the present example.

On Figure 53, we can see that the OPP starts to fold the setpoint immediately from a low mains operation. This is no different than a standard OPP circuitry built from a resistive string placed between the bulk rail and the current sense pin. However, in some applications, it is good to remove the OPP at low line and place a small threshold so that our OPP only changes the circuit power capability at high line only. Figure 54 offers a possible solution built on a zener diode connection.

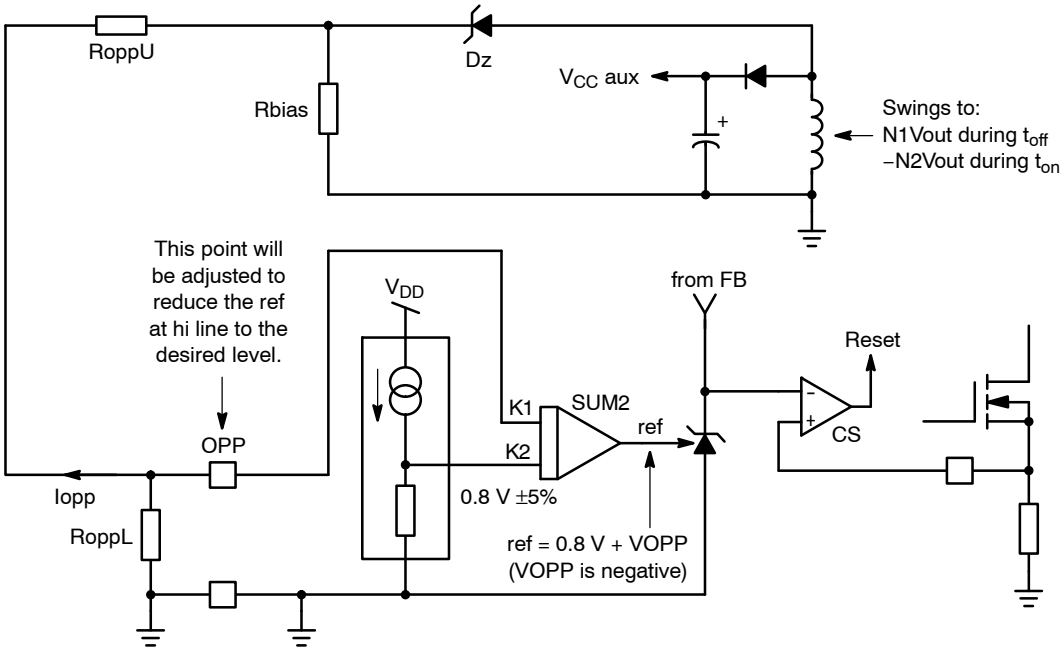


Figure 54. The Zener Diode can Introduce a Threshold which Disables OPP at Low Line for Maximum Power Capability

Suppose we need a threshold placed at 150 Vdc. In that case, give the turn ratio, we need to install a zener diode featuring the following breakdown voltage:

$$V_z = 150 \times 0.16 = 24\ V \qquad \text{(eq. 8)}$$

In high line conditions (V_{bulk} = 375 Vdc), the voltage on the zener diode voltage will now swing to:

$$V_{aux} = -N_2 V_{in,max} + 24 = -0.16 \times 375 + 24 = -36\ V \qquad \text{(eq. 9)}$$

Applying Equation 6 again, we have:

$$R_{OPPU} = \frac{36 - 0.16}{0.16/1\ k} = 224\ k\Omega \qquad \text{(eq. 10)}$$

The new compensation now looks like what Figure 55 shows:

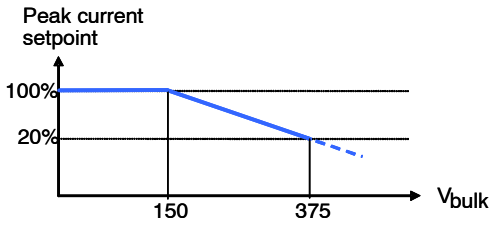
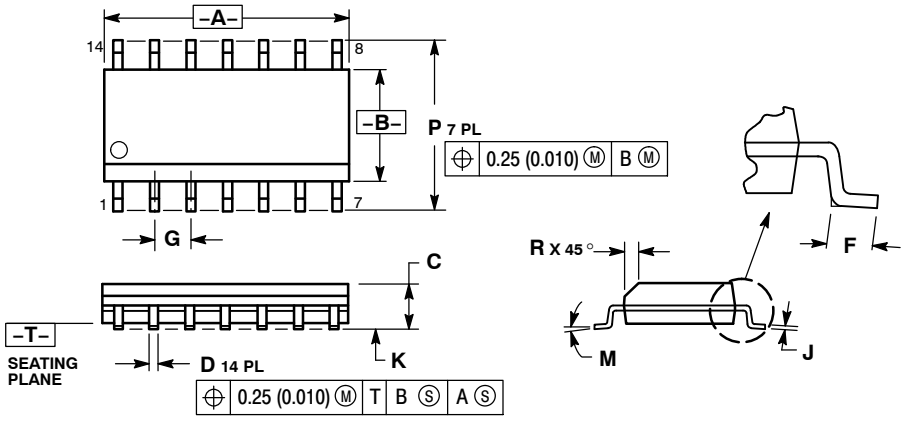


Figure 55. The Addition of the Zener Diode Introduces a Threshold at 150 Vdc

The bias resistor R_{bias}, makes sure that enough current circulates in the zener diode to make it work far enough from its knee. The tradeoff includes the power consumption brought by the addition of this new component. Further reduction can be obtained by inserting a standard diode in series with the zener to block the positive excursion.

PACKAGE DIMENSIONS

SOIC−14
D SUFFIX
CASE 751A−03
ISSUE H



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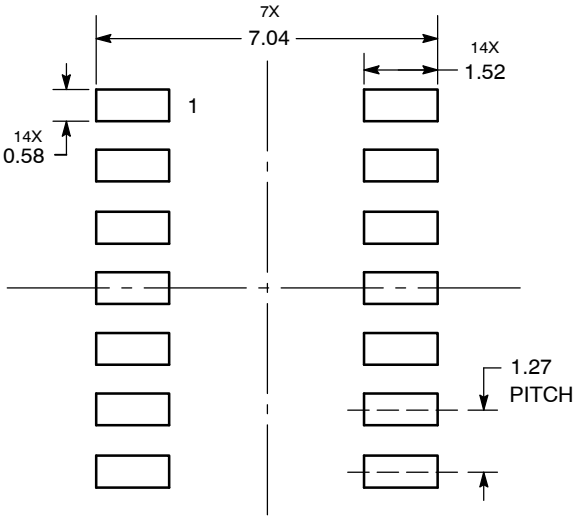
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



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