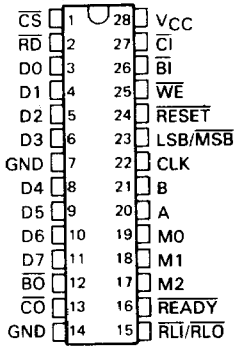
THCT2000M, THCT2000E DIRECTION DISCRIMINATORS

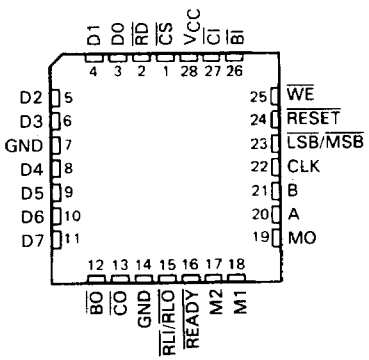
D2889, NOVEMBER 1985

- Inputs are TTL- and CMOS-Voltage Compatible
- Interfaces Mechanical Devices to Data Bus
- Identifies and Measures Forward or Backward Rotation or Direction
- Measures Pulse Duration and Frequency
- Cascadable 16-Bit Up/Down Counter
- 8-Bit Parallel 3-State Bus with Each Output Capable of Driving up to 15 LSTTL Loads
- Dependable Texas Instruments Quality and Reliability

THCT2000M . . . JD PACKAGE
THCT2000E . . . JD OR N PACKAGE
(TOP VIEW)



THCT2000M . . . FK PACKAGE
THCT2000E . . . FN PACKAGE
(TOP VIEW)



description

The THCT2000 direction discriminator can determine the direction and displacement of a mechanical device based on input signals from two transducers in quadrature. It can also measure a pulse duration using a known clock rate, or a frequency over a known time interval. It includes a 16-bit counter, which can be used separately. Several of these devices may be cascaded to provide accuracy greater than 16-bits.

The device may be used in many diverse applications, and is specifically designed for use in many types of microprocessor-based systems. Some of the possibilities include motor controls, robotics, tracker balls (mice), lathe or tooling machines, automobiles, and conveyer belts or other transport mechanisms.

The THCT2000M is characterized for operation over the full military temperature range of −55°C to 125°C. The THCT2000E is characterized for operation from −40°C to 85°C.

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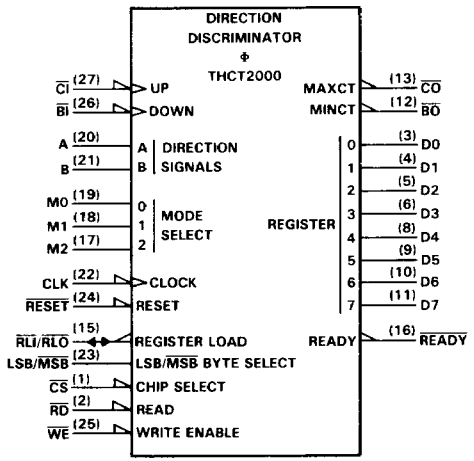
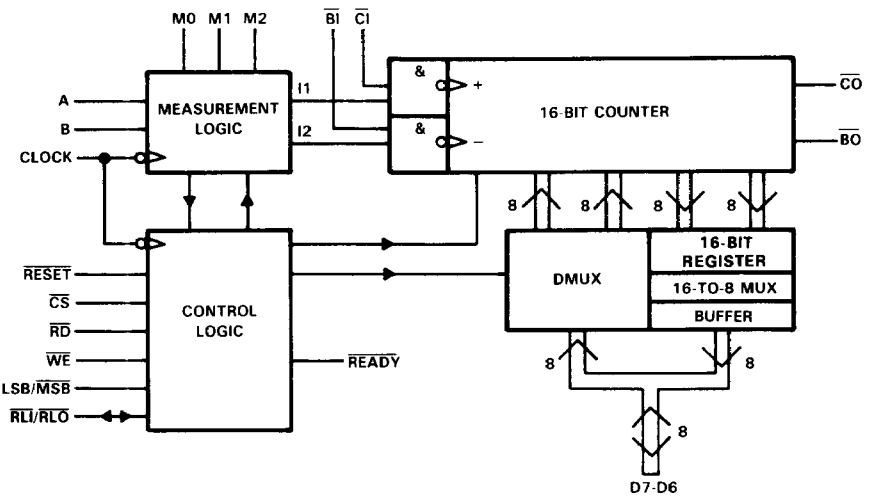
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

functional block diagram



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PIN NAME	PIN NUMBER	DESCRIPTION
A, B	20, 21	Signal measurement inputs.
$\overline{BI}$	26	Cascade input for counting down. In mode 0, $\overline{BI}$ is used as the clock input for counting down. Triggering occurs on the high-to-low transition.
$\overline{BO}$	12	Counter output underflow signal. Active (low) for a duration equal to the low level of the input clock.
$\overline{CI}$	27	Cascade input for counting up. In mode 0, $\overline{CI}$ is used as the clock input for counting up. Triggering occurs on the high-to-low transition.
CLK	22	Clock input. Used for internal synchronization and control timing.
$\overline{CO}$	13	Counter output overflow signal. Active (low) for a duration equal to the low level of the input clock.
$\overline{CS}$	1	Chip select input. This active-low input is used to enable read and write functions. For additional details, see read and write timing diagrams.
D0-D7	3, 4, 5, 6, 8, 9, 10, 11	Counter load inputs/register output data lines.
GND	7, 14	Pins 7 and 14 are both internally connected to the ground rail of the integrated circuit but both should be connected to the system ground for proper operation.
LSB/$\overline{MSB}$	23	Byte select input. During read operations, a high level selects the least significant byte, while a low level selects the most significant byte. For write operations, this input directs the data on the bus into the least significant or most significant byte position of the counter. See write timing diagrams for additional details.
M0, M1, M2	19, 18, 17	Mode select inputs.
$\overline{RD}$	2	Read input. When active (low) in conjunction with $\overline{CS}$ low, the data stored in the output register will be present on the data bus as selected by the LSB/$\overline{MSB}$ input. See read timing diagrams for additional details.
$\overline{READY}$	16	Ready output. When active (low), this output indicates to the processor that it may complete the read or write operation. $\overline{READY}$ is synchronous with the negative-going edge of CLK. This output requires a pullup resistor (1 kΩ nominal).
$\overline{RESET}$	24	Counter and control logic reset. When active (low), the counter is asynchronously reset to zero while the control logic is asynchronously initialized to the proper state as determined by the mode control inputs. The output register is not affected by $\overline{RESET}$.
$\overline{RLI}$/$\overline{RLO}$	15	Register load input/register load output (open drain). This pin can be used as an input to directly load the output register, or it can be used as an output to detect whenever the output register has been loaded. When used as an output, a pullup resistor (1 kΩ nominal) is required. See read timing diagrams for additional details.
V_{CC}	28	Power supply voltage.
$\overline{WE}$	25	Write enable input. When active (low) in conjunction with $\overline{CS}$ low, the data present on D0-D7 will be asynchronously loaded into the counter as selected by LSB/$\overline{MSB}$. See write timing diagrams for additional details.