

VMTA

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ENGINEERING SOLUTIONS ON A CHIP FROM INTERSIL

Product offerings described in this data book reflect Intersil's commitment to industry leadership as a producer of advanced low-power analog and digital semiconductor components and data acquisition systems.

These components are fabricated using a wide variety of process technologies and are intended to provide state-of-the-art performance and maximum cost effectiveness.

Product areas in which Intersil demonstrates its innovative approach to providing engineering solutions on a chip include:

- **FIELD EFFECT AND DUAL MATCHED BIPOLAR TRANSISTORS**

A complete line of high-performance junction FETs, dual JFETs, MOSFETs and matched dual bipolar devices.

- **DIGITAL**

Very low-power CMOS ROMs and EPROMs, as well as high-speed HMOS ROMs; CMOS microprocessors, peripherals and UARTs.

- **ANALOG SWITCHES AND MULTIPLEXERS**

The industry's broadest offering of highest-performance switches, including a video-RF switch with excellent isolation at 100 MHz, and multiplexers featuring the least error as well as unprecedented input overload protection.

- **ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS**

3½- and 4½-digit display output (DVM) analog-to-digital converters; 12-, 14- and 16-bit microprocessor-compatible analog-to-digital converters; and high-speed precision digital-to-analog converters up to 14 bits.

- **LINEAR**

A new set of low-power devices with unequalled performance—1- μ V offset voltage op amps, 4- μ A quiescent current regulators and supply monitors, 95-per-cent-efficient voltage converters and 1ppm/°C voltage references; a complete family of CMOS op amps; and a wide variety of special analog function circuits.

- **TIMERS, COUNTERS AND DISPLAY DRIVERS**

A wide range of low-power counters, timers and multidigit LED, LCD and vacuum fluorescent display decoder/drivers, including those with full alphanumeric capability.

General Information

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EXPLANATION OF TERMS, INDICES AND SPECIAL SUBSECTIONS

A

PRODUCTION DATA SHEET

This is a full, final data sheet, and describes a mature product in full production. Although Intersil reserves the right to make changes in specifications contained in these data sheets at any time without notice, such changes are not common and are usually minor, generally relating to yield and processing improvements. These data sheets are not marked; others are marked preliminary.

PRELIMINARY DATA SHEET

A preliminary data sheet is issued in advance of the availability of production samples and generally indicates that at the time of printing, the device had not been fully characterized. In the case of a second-source part, the specifications are already determined, and a "preliminary" designation indicates the anticipated availability of the device.

ALPHANUMERIC INDEX

This part number index is arranged first by alpha sequence, (ie: ADCxxxx, DGxxx, Gxxx, ICLxxx, ICMxxxx, etc.) then by numeric sequence (ie: LM100, LM101A, LM102, LM105, etc.) and ignoring package/temperature/pin number suffixes. The basic numbering sequence, is sorted by reading the part number characters from left to right. Reading the left character first (which is usually an alpha character), then the next character to the right and so forth.

BASE NUMBER INDEX

If only the basic part number is known, use the Base Number Index as a locator aid. The Base Number Index is organized in numeric sequence (with alpha prefixes appearing in bold type and numeric characters set in medium type). Devices are arranged in this index according to the numeric value of the first digit on the left, then the value of the second digit, then the third, and so on. For example, device number ICM7218 precedes ICL741, no package/temperature/pin number suffixes are included, but these may be obtained from the specific product data sheet.

FUNCTION INDEX

This is an index of Intersil device types categorized by product grouping and function. The first major subsection, DISCRETES, is further subdivided into categories for JFETs and Special Function devices.

All remaining major subsections (ANALOG SWITCHES/MULTIPLEXERS, DATA ACQUISITION, LINEAR, TIMERS/COUNTERS, TIMEKEEPING/DTMF, MEMORIES and MICROPROCESSORS/PERIPHERALS)

are organized alphabetically by function. The Functional Index appears in its entirety in section A, and an appropriate subindex appears at the beginning of each major product section.

CROSS-REFERENCE GUIDES

Two cross-reference guides are provided: one for Discrete Devices and one for Integrated Circuits.

The Discrete Cross-Reference Guide indicates whether Intersil can provide the industry-standard type, or an Intersil preferred part instead.

The IC Alternate Source Cross-Reference Guide lists competitive manufacturer device types for which Intersil makes pin-for-pin replacements. In the left-hand column, the competitive device part number is organized alphabetically by manufacturer. The Intersil pin-for-pin replacement appears in the right hand column.

SELECTOR GUIDES

Selector guide tables appear at the front of each major product category subsection and provides a quick reference of key parameters for devices contained in that section.

DEVICE FUNCTION/PACKAGE CODES

Package dimensions and diagrams explaining device prefix and suffix codes appear in Appendix B.

DIE SELECTION CRITERIA

Many of Intersil's semiconductor products are available in die form. This subsection of Appendix B contains general information on criteria for transistor and integrated circuit die selection, including physical parameters, packaging for shipment, assembly, testing and purchase options.

HIGH-RELIABILITY PROCESSING

This subsection of Appendix B defines Intersil's commitment to 100 percent compliance with MIL-STD-883, MIL-STD-750, MIL-M-38510 and MIL-S-19500 specifications. It also outlines Intersil's programs for quality conformance, quality testing and limited use qualification and includes a glossary of military/aerospace Hi-Rel terms.

Intersil reserves the right to make changes in circuitry or specifications contained herein at any time without notice.

Intersil assumes no responsibility for the use of any circuits described herein and makes no representations that they are free patent infringement.

LIFE SUPPORT POLICY. INTERSIL'S PRODUCTS ARE NOT AUTHORIZED, NOR WARRANTED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES AND/OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF INTERSIL, INC.

For the purposes of this policy, critical components in life support systems and/or devices are defined as:

1. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
2. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

Intersil cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Intersil product. No circuit patent licenses are implied. Intersil reserves the right to change the circuitry and specifications without notice at any time.

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†The ICL7136 is recommended for all applications which currently employ the ICL7126.

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**Obsolete product, refer to page A-9.

OBSOLETE PRODUCTS

The products listed below have been designed into circuits in the past, but are no longer likely to be the most economic choice for new designs.

These products are still available for use in existing designs. Data sheets for these products are available upon request.

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AM25L02/3/4	SU/NE536
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G116-19	LM107/307
G125-32	μ A741
ICL7600/01	AD741K
ICL8052/7101	μ A748
ICL8052/71C03	LH2101/2301
ICL8068/71C03	IH5101
ICL8052/53	LM4250
IH401	μ A733
IMF5911/12	LM102/302
LD110/111	LM110/310
LD114	LH2110/2310
MM450/550	LH2111/2311
MM451/551	LM111/311
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 MP7521JN AD7521JN
 MP7521KD AD7521KD
 MP7521KN AD7521KN
 MP7521LD AD7521LD
 MP7521LN AD7521LN
 MP7521SD AD7521SD
 MP7521TD AD7521TD
 MP7521UD AD7521UD
 MP7523JN AD7523JN
 MP7523KN AD7523KN
 MP7523LN AD7523LN
 MP7530JD AD7530JD
 MP7530JN AD7530JN
 MP7530KD AD7530KD
 MP7530KN AD7530KN
 MP7530LD AD7530LD
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 MP7531KN AD7531KN
 MP7531LD AD7531LD
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 MP7533AD AD7533AD
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 MP7533CD AD7533CD
 MP7533JN AD7533JN
 MP7533KN AD7533KN
 MP7533LN AD7533LN
 MP7533SD AD7533SD
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 MP7533UD AD7533UD
 MP7621AD AD7541AD
 MP7621BD AD7541BD
 MP7621JN AD7541JN
 MP7621KN AD7541KN
 MP7621SD AD7541SD
 MP7621TD AD7541TD

Mitsubishi Intersil
 M58435P ICM1115B

Motorola Intersil
 LM101 LM101
 LM105 LM105
 LM107 LM107
 LM110 LM110
 LM111 LM111
 LM301 LM301
 LM305 LM305
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 MCM68332 IM7332
 MCM68364 IM7364
 MC1723 μA723
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 MC1748 μA748
 MHW590 AD590

National Semiconductor Intersil
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 AD7520JN (DAC1022LCN) AD7520KD
 AD7520KN (DAC1021LCD) AD7520KD
 AD7520KN (DAC1021LCN) AD7520KN
 AD7520LD (DAC1020LCD) AD7520LD
 AD7520LN (DAC1020LCN) AD7520LN
 AD7520SK (DAC1022LD) AD7520SD
 AD7520TD (DAC1021LD) AD7520TD
 AD7520UD (DAC1020LD) AD7520UD
 AD7521JD (DAC1222LCD) AD7521JD
 AD7521JN (DAC1222LCN) AD7521KD
 AD7521KD (DAC1221LCD) AD7521KN
 AD7521KN (DAC1221LCN) AD7521KN
 AD7521LD (DAC1220LCD) AD7521LD
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 AD7521SD (DAC1222LD) AD7521SD
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 AD7530KN (DAC1021LCN) AD7530KN
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 AD7533AD (DAC1022LCD) AD7533AD
 AD7533BD (DAC1021LCD) AD7533BD
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 AD7533KN (DAC1021LCN) AD7533KN
 AD7533LN (DAC1020LCN) AD7533LN
 AD7533SD (DAC1022LD) AD7533SD
 AD7533TD (DAC1021LCN) AD7533TD
 AD7533UD (DAC1020LD) AD7533UD
 AH0139CD DG139BK
 AH0139D DG139BK
 AH0139D/883 DG139AK/883B
 AH0142CD DG142BK
 AH0142D DG142BK
 AH0142D/883 DG142AK/883B
 AH0143CD DG143BK
 AH0143D DG143AK
 AH0143D/883 DG143AK/883B
 AH0144CD DG144BK
 AH0144D DG144AK
 AH0144D/883 DG144AK/883B
 AD0145CD DG145BK
 AH0145D DG145AK
 AH0145D/883 DG145AK/883B
 AH0146CD DG146BK
 AH0146D DG146AK
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 AH0161CD DG161BK
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 AH0162D/883B DG162AK/883B
 AH0163CD DG163BK
 AH0163D DG163AK
 AH0163D/883 DG163AK/883B
 AH0164CD DG164BK
 AH0164D DG164AK
 AH0164D/883B DG164AK/883B
 AH5009CN IH5009CPD
 AH5010CN IH5010CPD
 AH5011CN IH5011CPE
 AH5012CN IH5012CPE
 AH5013CN IH5013CPD
 AH5014CN IH5014CPD
 AH5015CN IH5015CPE
 AH5016CN IH5016CPE
 AM9709CN IH5009CPD
 AM9709CN IH5009CPD
 AM9710CN IH5010CPD
 AM9710CN IH5010CPD
 AM9711CN IH5011CPE
 AM9711CN IH5011CPE
 AM9712CN IH5012CPE
 AM9712CN IH5012CPE
 DM7555 ICM7555
 DM7556 ICM7556
 LF11201D DG201AK
 LF11201D/883 DG201AK/883B
 LF11508D IH6108MJ
 LF11508D/883 IH6108MJ/883B
 LF11509D IH6208MJ
 LF11509D/883 IH6208MJ/883B
 LF13201 DG201
 LH0042 LH0042
 LH2108 LH2108
 LH2110 LH2110
 LH2111 LH2111
 LH2301 LH2301
 LH2308 LH2308
 LH2310 LH2310
 LH2311 LH2311
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 LM101 LM101
 LM102 LM102
 LM105 LM105
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 LM110 LM110
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 LM300 LM300
 LM301 LM301
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 AD7533AD (DAC1022LCD) AD7533AD
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 DG139BK DG139BK
 DG139AK/883B DG139AK/883B
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 DG143BK DG143BK
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 IH5009CPD IH5009CPD
 IH5010CPD IH5010CPD
 IH5011CPE IH5011CPE
 IH5012CPE IH5012CPE
 IH5013CPD IH5013CPD
 IH5014CPD IH5014CPD
 IH5015CPE IH5015CPE
 IH5016CPE IH5016CPE
 IH5009CPD IH5009CPD
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 IH5010CPD IH5010CPD
 IH5011CPE IH5011CPE
 IH5011CPE IH5011CPE
 IH5012CPE IH5012CPE
 IH5012CPE IH5012CPE
 ICM7555 ICM7555
 ICM7556 ICM7556
 DG201AK DG201AK
 DG201AK/883B DG201AK/883B
 IH6108MJ IH6108MJ
 IH6108MJ/883B IH6108MJ/883B
 IH6208MJ IH6208MJ
 IH6208MJ/883B IH6208MJ/883B
 DG201 DG201
 LH0042 LH0042
 LH2108 LH2108
 LH2110 LH2110
 LH2111 LH2111
 LH2301 LH2301
 LH2308 LH2308
 LH2310 LH2310
 LH2311 LH2311
 LM100 LM100
 LM101 LM101
 LM102 LM102
 LM105 LM105
 LM107 LM107
 LM108 LM108
 LM110 LM110
 LM111 LM111
 LM300 LM300
 LM301 LM301
 LM302 LM302
 LM305 LM305
 LM307 LM307
 LM308 LM308
 LM310 LM310
 LM311 LM311
 LM4250 LM4250
 μA723 μA723
 μA733 μA733
 μA740 μA740
 μA741 μA741
 μA741 μA741
 μA741 μA741
 μA748 μA748
 μA748 μA748
 IM7332 IM7332
 IM7364 IM7364
 ICM7224 ICM7224

NEC
 μPD816C ICM7038B
 μPD820C ICM1115B
 μPD833G ICM7223
 μPD1963C ICM7050
 μPD2332 IM7332
 μPD2364 IM7364

NPC Intersil
 SM5510 ICM1115B

OKI Intersil
 MSM503 AD503

Panasonic/Matsushita Intersil
 MN6091 ICM7038B
 MN6093 ICM7051A

Phillips/Fasalec Intersil
 MB7B ICM7245U
 MB101 ICM7245B
 MB103 ICM7245E
 MB105 ICM7245U
 MB107 ICM7245D
 MB108 ICM7245E
 MB143 ICM7245A
 MB144 ICM7245F
 MB510 ICM1115B

Plessey Intersil
 SC748 μA748

PMI Intersil
 PM308 LM308
 SSS741 μA741

Raytheon Intersil
 LH2101 LH2101
 LH2301 LH2301
 LH2311 LH2311
 LM101 LM101
 LM105 LM105
 LM107 LM107
 LM108 LM108
 LM301 LM301
 LM305 LM305
 LM307 LM307
 LM308 LM308
 LM308 LM308
 LM311 LM311
 RC723 μA723
 RC733 μA733
 RC741 μA741
 RC748 μA748
 RM723 μA723
 RM741 μA741
 RM748 μA748

RCA Intersil
 CA101 LM101
 CA107 LM107
 CA111 LM111
 CA301 LM301
 CA307 LM307
 CA308 LM308
 CA311 LM311
 CA741 μA741
 CA748 μA748
 CD22015E ICM7051A
 CPD6402 IM6402

Samsung Intersil
 K5524DU01E ICM7245U
 K5524B01J ICM7245A
 K5524B01H ICM7245B
 K5524B10H ICM7245D
 K5524B12H ICM7245E
 K5524B20H ICM7245F

Sanyo Intersil
 LC7523 AD7523

Signetics Intersil
 μA723 μA723
 μA733 μA733
 μA740 μA740
 μA741 μA741
 μA741 μA741
 μA748 μA748
 μA748 μA748
 LH2101 LH2101
 LH2108 LH2108
 LH2301 LH2301
 LH2308 LH2308

DISCRETE CROSS REFERENCE



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
10DS	2N5458	2N2606	2N2607	2N3331	2N5270	2N3814	IT132
10DU	2N3884	2N2607	2N2607	2N3332	2N5268	2N3815	IT132
102M	2N5586	2N2608	2N2608	2N3333	IT132	2N3816	IT130
102S	2N5457	2N2609	2N2609	2N3334	IT132	2N3818A	IT130A
103M	2N5457	2N2609JAN	2N2609JAN	2N3335	IT132	2N3817	IT130
103S	2N5458	2N2609	IT120	2N3336	IT132	2N3817A	IT130A
104M	2N5458	2N2640	IT122	2N3347	IT137	2N3818	2N5484
105M	2N5458	2N2641	IT122	2N3348	IT138	2N3820	2N2605
105U	2N4340	2N2642	IT120	2N3349	IT138	2N3821	2N5281
106M	2N5465	2N2643	IT122	2N3350	IT137	2N3822	2N3822
107M	2N5485	2N2644	IT122	2N3351	IT138	2N3823	2N3823
110U	2N3665	2N2652	IT120	2N3352	IT139	2N3824	2N3824
120U	2N3666	2N2652A	IT120	2N3365	2N4340	2N3827	IT131
125U	2N4339	2N2720	IT120	2N3366	2N4338	2N3828	IT120
1277A	2N3822	2N2721	IT122	2N3367	2N4338	2N3829	2N2609
1278A	2N3821	2N2722	IT120	2N3368	2N4341	2N3909A	2N2609
1279A	2N3821	2N2722	IT139	2N3369	2N4339	2N3821	2N3821
1280A	2N4224	2N2803	IT139	2N3370	2N4338	2N3822	2N3822
1281A	2N3822	2N2804	IT138	2N3376	2N2608	2N3849	IT132
1282A	2N4341	2N2805	IT138	2N3378	2N2608	2N3950	IT132
1283A	2N4340	2N2806	IT139	2N3380	2N2609	2N3954	2N3954
1284A	2N4222	2N2807	IT139	2N3382	2N3994	2N3954A	2N3954A
1285A	2N3821	2N2841	2N2607	2N3384	2N3998	2N3955	2N3955
1286A	2N4220	2N2842	2N2607	2N3388	2N5114	2N3955A	2N3955A
130U	2N3667	2N2843	2N2607	2N3409	IT122	2N3956	2N3956
1325A	2N4222	2N2844	2N2607	2N3410	IT122	2N3957	2N3957
135U	2N4339	2N2903	IT122	2N3411	IT122	2N3966	2N4416
14T	2N4224	2N2903A	IT120	2N3423	IT122	2N3967	2N4221
155U	2N4416	2N2910	IT122	2N3424	IT122	2N3967A	2N4221
1714A	2N4340	2N2913	IT122	2N3425	IT122	2N3968	2N3685
182S	2N4391	2N2914	IT120	2N3436	2N4341	2N3968A	2N3685
183S	2N3823	2N2915	IT120	2N3437	2N4340	2N3969	2N3686
187S	2N4338	2N2915A	IT120	2N3438	2N4338	2N3969A	2N3686
196S	2N4340	2N2916	IT120	2N3452	2N4200	2N3970	2N3970
196S	2N4341	2N2916A	IT120	2N3453	2N4338	2N3971	2N3971
2000M	2N3823	2N2917	IT122	2N3454	2N4338	2N3972	2N3972
2001M	2N3823	2N2918	IT122	2N3455	2N4340	2N3973	2N3953
200S	2N4338	2N2919	IT120	2N3456	2N4338	2N3974	2N3954
200U	2N3824	2N2919A	IT120	2N3457	2N4338	2N3994	2N3994
201S	2N4391	2N2920	2N2920	2N3458	2N4341	2N3994A	2N3994
202S	2N4392	2N2920A	2N2920	2N3459	2N4339	2N4008	IT132
203S	2N3821	2N2936	IT120	2N3460	2N4336	2N4010	IT132
204S	2N3821	2N2937	IT120	2N3513	IT122	2N4011	IT132
2078A	2N3955	2N2972	IT122	2N3514	IT122	2N4015	IT139
2079A	2N3955	2N2973	IT122	2N3515	IT122	2N4016	IT137
2080A	2N3955A	2N2974	IT120	2N3516	IT122	2N4017	IT139
2081A	2N3955A	2N2975	IT120	2N3517	IT122	2N4018	IT139
2093M	2N3687	2N2976	IT120	2N3521	IT122	2N4019	IT138
2094M	2N3686	2N2977	IT120	2N3522	IT122	2N4020	IT139
2095M	2N3686	2N2978	IT120	2N3574	2N2607	2N4021	IT139
2098A	2N3954	2N2979	IT120	2N3575	2N2607	2N4022	IT139
2099A	2N3955A	2N2980	IT121	2N3578	2N2609	2N4023	IT137
210U	2N4416	2N2981	IT122	2N3587	IT122	2N4024	IT137
2130U	2N5452	2N2982	IT122	2N3608	3N172	2N4025	IT137
2132U	2N3955	2N3043	IT121	2N3660	IT120	2N4026	3N163
2134U	2N3955	2N3044	IT122	2N3684	2N3684	2N4038	2N4351
2135U	2N3957	2N3045	IT122	2N3684A	2N3684	2N4039	2N4351
2136U	2N3958	2N3046	IT121	2N3685	2N3685	2N4065	3N183
2138U	2N3958	2N3047	IT122	2N3685A	2N3685	2N4066	3N186
2139U	2N3958	2N3048	IT122	2N3686	2N3686	2N4067	3N186
2147U	2N3958						
2148U	2N3956	2N3049	IT139	2N3686A	2N3686	2N4082	2N3954
2149U	2N3956	2N3050	IT139	2N3687	2N3687	2N4083	2N3955
231S	2N3954	2N3051	IT139	2N3687A	2N3687	2N4084	2N3954
232S	2N3955	2N3052	IT139	2N3722	IT131	2N4085	2N3955
232S	2N3956	2N3059	IT139	2N3727	IT130	2N4091	2N4091
234S	2N3957	2N3066	2N4340	2N3728	IT122	2N4091A	2N4091
235S	2N3958	2N3067	2N4339	2N3753	IT121	2N4091JAN	2N4091JAN
2411U	2N4989	2N3068	2N4338	2N3754	IT132	2N4091JANTX	2N4091JANTX
250U	2N4091	2N3069	2N4341	2N3801	IT132	2N4091JANTXV	2N4091JANTXV
251U	2N4392	2N3070	2N4339	2N3802	IT132	2N4092	2N4092
2N2090	IT120	2N3071	2N4338	2N3803	IT132	2N4092A	2N4092
2N2090A	IT121	2N3084	2N4339	2N3804	IT135	2N4092JAN	2N4092JAN
2N2090B	IT121	2N3085	2N4339	2N3804A	IT130A	2N4092JANTX	2N4092JANTX
2N2223	IT122	2N3085	2N4339	2N3805	IT130	2N4092JANTXV	2N4092JANTXV
2N2223A	IT121	2N3087	2N4338	2N3805A	IT130A	2N4093	2N4093
2N2386	2N2808	2N3089	2N4339	2N3806	IT122	2N4093A	2N4093
2N2386A	2N2808	2N3089A	2N4339	2N3807	IT122	2N4093JAN	2N4093JAN
2N2453	IT122	2N3089	2N4339	2N3808	IT122	2N4093JANTX	2N4093JANTX
2N2453A	IT121	2N3093A	2N4339	2N3809	IT122	2N4093JANTXV	2N4093JANTXV
2N2480	IT122	2N3113	2N2607	2N3910	2N3810	2N4100	2N4100
2N2480A	IT121	2N3277	2N2606	2N3810A	2N3810A	2N4117	2N4117
2N2497	2N2608	2N3278	2N2607	2N3811	2N3811	2N4117A	2N4117A
2N2498	2N2609	2N3325	2N5265	2N3811A	2N3811A	2N4118	2N4118
2N2499	2N2609	2N3326	2N3297	2N3812	IT132	2N4118A	2N4118A
2N2500	2N2609	2N3330	2N5266	2N3813	IT132	2N4119	2N4119

DISCRETE CROSS REFERENCE (cont.)



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
3N180 3N181 3N182 3N183 3N188	3N172 3N181 3N181 3N181 3N188	8CV99 BF244 BF244A BF244B BF244C	IT182 2N5486 2N5484 2N5485 2N5486	BFX78 BFX82 BFX83 BFX89 BFY20	2N5337 2N5019 2N5019 IT120A IT122	CM552 CM593 CM697 CM600 CM656	2N5432 2N5433 2N5433 2N5433 2N5433
3N189 3N190 3N191 3N207 3N208	3N189 3N180 3N191 3N190 3N188	BF245 BF245A BF245B BF245C BF246	2N5486 2N4416 2N4416 2N4416 2N5485	BFY91 BFY92 BFY83 BFY84 BFY85	IT122 IT122 IT122 IT122 IT122	CM890 CMX740 CP640 CP643 CP650	2N4868A 2N5432 2N4391 2N5434 2N5432
3SK22 3SK23 3SK28 421 4390TP	2N5486 2N5397 2N5397 2N4392 2N5462	BF246A BF246B BF246C BF247 BF247A	2N5539 2N5638 2N5638 2N4091 2N4091	BFY86 BFY91 BFY92 BN208 BSV22	IT122 IT122 IT122 IT122 2N4416	CP651 CP652 CP653 D1101 D1102	2N5433 2N5433 2N5433 2N3921 2N3921
8033TP 588U 591 591 703U	2N5480 2N4416 2N5467 2N4416 2N4220	BF247B BF247C BF255 BF255A BF255B	2N4091 2N4091 2N5484 2N5484 2N4416	BSV78 BSV78 BSV8C BSX82 C21	2N4955A 2N4857A 2N4858A 2N3822 2N3821	D1103 D1177 D1178 D1179 D1180	2N4338 2N3921 2N3821 2N4338 2N3922
704U 705U 707U 714U 734EU	2N4220 2N4224 2N4860 2N3822 2N4416	BF256C BF320 BF320A BF320B BF320C	2N4416 2N5451 2N5450 2N5461 2N5482	C230B C38 C413N C510 C511	2N5196 2N4338 2N5434 2N4338 2N4221	D1181 D1182 D1183 D1184 D1185	2N4338 2N4338 2N4341 2N4340 2N4339
734U 751U 752U 753U 754U	2N5516 2N4340 2N4340 2N4341 2N4340	BF346 BF347 BF348 BF800 BF801	ITE4392 U01 U10 2N4857 2N4857	C812 C813 C814 C815 C620	2N4221 2N4221 2N4220 2N4221 2N4220	D1201 D1202 D1203 D1301 D1352	2N4224 2N4220 2N4220 2N4220 2N4220
755U 756U A190 A191 A192	2N4341 2N4340 ITE4416 ITE4416 2N4416	BF802 BF804 BF805 BF806 BF806	2N4339 2N4338 2N4859 2N4859 2N4856	C821 C822 C823 C824 C825	2N4220 2N4220 2N4220 2N4220 2N4220	D1303 D1420 D1421 D1422 D2T2218	2N4220 2N4858 2N3822 2N4855 IT129
A193 A194 A195 A196 A197	2N5484 2N5484 2N5484 ITE4416 ITE4391	BF810 BF811 BF815 BF816 BF817	2N4858 2N4858 2N4858 2N4856 2N4356	C850 C851 C852 C853 C8690	2N4220 2N4220 2N4220 2N4220 2N4341	D2T2218A D2T2218 D2T2219A D2T2904 D2T2904A	IT129 IT129 IT129 IT139 IT139
A198 A199 AST3891 AST3892 AST3893	ITE4392 ITE4393 2N5484 2N5484 2N4415	BF818 BF010 BF011 BF012 BF013	2N4858 U401 U401 U402 U403	C6691 C6692 C673 C674 C680	2N4341 2N4338 2N4341 2N4341 2N4338	D2T2905 D2T2905A D2T918 DA102 DA02	IT139 IT139 IT129 2N5196 2N5196
AST3924 AST5490 AST5491 AST5492 AD3954	2N4341 2N5480 2N5451 2N5492 2N3954	BF014 BF015 BF016 BF023 BF026	U404 U405 U406 IT5912 U403	C680A C681 C681A C692 C692A	2N4338 2N4338 2N4338 2N4339 2N4339	DN3066A DN3067A DN3068A DN3069A DN3070A	2N3921 2N4338 2N4336 2N3922 2N3621
AD3954A AD3955 AD3956 AD3956 AD3956 AD3955	2N3954A 2N3955 2N3956 2N3956 2N3955	BF044 BF045 BF046 BF049B BF049C	IT5912 IT5912 2N3955 2N3956 2N3958	C693 C683A C684 C684A C685	2N4339 2N4338 2N4220 2N4220 2N4220	DN3071A DN3365A DN3365B DN3365C DN3365D	2N4338 2N4320 2N4091 2N3956 2N4091
AD5906 AD5907 AD5908 AD5909 AD610	2N5906 2N5907 2N5906 2N5909 2N4878	BF521 BF521A BF567 BF567P BF568	2N5199 2N5199 2N3921 2N5459 2N3923	C685A C60 C61 C64 C65	2N4220 2N4338 2N4338 2N4338 2N4338	DN3367A DN3367B DN3366A DN3368A DN3369A	2N3687 2N4091 2N4341 2N4221 2N4339
AD611 AD612 AD613 AD614 AD615	2N4878 2N4878 2N4878 IT124 IT124	BF568P BF570 BF571 BF572 BF573	2N4416 2N3921 2N3922 2N3923 2N3921	C91 C92 C93 C94 C94E	2N4858 2N4363 2N4363 2N5457 2N5457	DN3369B DN3370A DN3370B DN3436A DN3436B	2N4220 2N4338 2N4338 2N4341 2N4222
AD616 AD618 AD620 AD621 AD622	IT120A IT140 IT132 IT130A IT130A	BF574 BF575 BF576 BF577 BF578	2N4856 2N4857 2N4858 2N4859 2N4950	C95 C95E C96E C97E C98E	2N5457 2N5459 2N5484 2N3822 2N3822	DN3437A DN3437B DN3438A DN3439B DN3458A	2N4340 2N4220 2N4339 2N4339 2N4341
AD630 AD631 AD632 AD633 AD633A	2N5520 2N5521 2N5522 2N5523 2N5524	BF579 BF580 BF710 BF711 BFW10	2N4861 2N4415A 2N5337 2N5019 2N3923	CC4445 CC4446 CC997 CF2396 CF24	2N5432 2N5434 2N4856 2N5458 2N3924	DN3458B DN3459A DN3459B DN3460A DN3460B	2N4222 2N4339 2N4220 2N4338 2N4320
AD635 AD637 AD636 AD636	2N3954 2N3955 2N3955 2N3956 2N3957	BFW11 BFW12 BFW13 BFW36 BFW39A	2N3922 2N4416 2N4867 IT128 IT120	CFM13026 CM600 CM601 CM602 CM603	2N4858 2N4092 2N4091 2N4091 2N4091	DNX1 DNX2 DNX3 DNX4 DNX5	2N4338 2N4338 2N4338 2N4989 2N4868
AD640 AD641 AD642 BC264 BC264A	2N5520 2N5521 2N5523 2N5496 2N5457	BFW54 BFW55 BFW56 BFW56 BFX11	2N3922 2N3922 2N4950 2N4224 IT132	CM640 CM641 CM642 CM643 CM644	2N4093 2N4093 2N4092 2N4092 2N4092	DNX6 DNX7 DNX8 DNX9 DU4339	2N4338 2N4416 2N4416 2N4338 2N5397
BC264B BC264C BC264D BCY87 BCY88	2N5456 2N5456 2N4416 IT121 IT122	BFX15 BFX36 BFX70 BFX71 BFX72	IT122 IT131 IT122 IT122 IT122	CM645 CM646 CM647 CM650 CM651	2N4092 2N4091 2N5432 2N5433	DU4340 E100 E101 E102 E103	2N5398 2N5456 2N4338 2N5457 2N5459

DISCRETE CROSS REFERENCE (cont.)



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
E105	J105	FF400	2N5457	IT127	IT127	ITE2977	IT120
E106	J106	FM1100	2N3954A	IT128	IT128	ITE2978	IT120
E107	J107	FM1100A	2N5906	IT129	IT129	ITE2979	IT120
E108	J105	FM1101A	2N5906	IT130	IT130	ITE3066	2N3685
E109	J106	FM1102	2N3954	IT130A	IT130A	ITE3067	2N3686
E110	J107	FM1102A	2N5906	IT131	IT131	ITE3068	2N3687
E111	J111	FM1103	2N3955	IT132	IT132	ITE3347	IT137
E111A	J111	FM1103A	2N5908	IT138	IT138	ITE3348	IT138
E112	J112	FM1104	2N3957	IT137	IT137	ITE3349	IT139
E112A	J112	FM1104A	2N5908	IT138	IT138	ITE3350	IT137
E113	J113	FM1105	2N3954A	IT139	IT139	ITE3351	IT138
E113A	J113	FM1105A	IT500	IT140	IT140	ITE368D	IT120
E114	J204	FM1106	2N3954A	IT1700	IT1700	ITE36DD	IT132
E174	J174	FM1106A	IT500	IT1701	3N172	ITE36DE	IT132
E175	J175	FM1107	2N3954	IT1702	3N163	ITE36DA	IT130
E176	J176	FM1107A	IT500	IT1750	IT1750	ITE3806	IT132
E177	J177	FM1108	2N3955	IT2700	3N165	ITE3807	IT132
E201	J201	FM1108A	IT500	IT2701	3N165	ITE3808	IT132
E202	J202	FM1109	2N3957	IT500	2N392	ITE3809	IT132
E203	J203	FM1109A	IT500	IT500	IT500	ITE3810	IT130
E204	J204	FM1110	2N3955	IT500P	IT500	ITE3811	IT130
E210	2N5397	FM1110A	IT501	IT501	IT501	ITE3817	IT130
E212	2N5397	FM1111	2N3957	IT501P	IT501	ITE3808	IT120
E230	2N4967	FM1111A	2N5909	IT502	IT502	ITE4017	IT139
E231	2N4967	FM1112	2N5196	IT502P	IT502	ITE4018	IT139
E232	2N4966	FM1200	2N6954	IT503	IT503	ITE4019	IT139
E233	2N4969	FM1201	2N3954	IT503P	IT503	ITE4020	IT139
E270	J270	FM1202	2N3954	IT504	IT504	ITE4021	IT139
E271	J271	FM1203	2N3955A	IT505	IT505	ITE4022	IT139
E300	2N5397	FM1204	2N3955	IT550	IT550	ITE4023	IT137
E304	2N5486	FM1205	2N3954	IT5911	IT5911	ITE4024	IT137
E305	2N5484	FM1206	2N3954	IT5912	IT5912	ITE4025	IT137
E308	J308	FM1207	2N3954	ITC2972	IT122	ITE4091	ITE4091
E309	J309	FM1208	2N3955A	ITC2973	IT122	ITE4092	ITE4092
E310	J310	FM1209	2N3955	ITC2974	IT120	ITE4093	ITE4093
E311	J310	FM1210	2N3955A	ITC2975	IT120	ITE4117	2N4117
E312	2N5397	FM1211	IT5911	ITC2976	IT120	ITE4118	2N4118
E400	2N3955	FM3954	2N3954	ITC2977	IT120	ITE4119	2N4119
E401	2N3955	FM3954A	2N3954A	ITC2978	IT120	ITE4338	2N4338
E402	2N3957	FM3955	2N3955	ITC2979	IT120	ITE4339	2N4339
E410	2N3955	FM3955A	2N3955A	ITC3347	IT137	ITE4340	2N4340
E411	IT5911	FM3956	2N3956	ITC3348	IT138	ITE4341	2N4341
E413	IT5911	FM3957	2N3957	ITC3349	IT139	ITE4391	ITE4391
E414	2N5454	FM3958	IT5911	ITC3350	IT137	ITE4392	ITE4392
E414	2N3956	FP4339	2N4339	ITC3351	IT138	ITE4393	ITE4393
E415	2N3957	FP4340	2N4340	ITC3352	IT138	ITE4416	ITE4416
E420	IT5911	FT0654A	2N5486	ITC3806	IT132	ITE4857	2N4857
E421	IT5912	FT0654B	2N5486	ITC3807	IT132	ITE4858	2N4858
E430	J309(X2)	FT0654C	2N4221	ITC3808	IT132	ITE4859	2N4859
E431	J310(X2)	FT0654D	2N4221	ITC3809	IT130	ITE4860	2N4860
ESM25	U401	FT3820	2N5019	ITC3807	IT132	J101	2N4336
ESM25A	U401	FT3820	2N5460	ITC3808	IT132	J102	2N5457
ESM4091	2N4091	FT3909	2N5019	ITC3909	IT132	J103	2N5459
ESM4092	2N4092	FT703	3N161	ITC3810	IT130	J105	J105
ESM4093	2N4093	FT704	3N163	ITC3811	IT130	J105-1B	J105
ESM4302	2N5457	GET5457	2N5457	ITC4017	IT139	J106	J106
ESM4303	2N5458	GET5458	2N5458	ITC4018	IT139	J106-1B	J106
ESM4304	2N5458	GET5459	2N5459	ITC4019	IT139	J107	J107
ESM4446	2N5432	HA7807	IT132	ITC4020	IT130	J107-1B	J107
ESM4446	2N5434	HA7809	IT132	ITC4021	IT138	J108	J106
ESM4447	2N5432	HOIG1030	3N163	ITC4022	IT139	J108-1B	J106
ESM4448	2N5434	HEP801	2N3822	ITC4023	IT137	J109	J106
FE0554A	2N4396	HEP802	2N5484	ITC4024	IT137	J109-1B	J106
FE0554B	2N5485	HEP803	2N5019	ITC4025	IT137	J110	J107
FE100	2N3821	HEPFO021	2N5484	ITE2453	IT120	J110-1B	J107
FE100A	2N3821	HEPFF1035	J176	ITE2635	IT120	J111	J111
FE102	2N4113	HEP2004	2N5484	ITE2636	IT122	J111-1B	J111
FE104	2N4113	HEP2005	2N5459	ITE2641	IT122	J111A	J111
FE104	2N4119	ID100	ID100	ITE2642	IT120	J111A-1B	J111
FE104A	2N4119	ID101	ID101	ITE2643	IT122	J112	J112
FE1800	2N4092	IMF3954	2N3954	ITE2644	IT122	J112-1B	J112
FE200	2N3821	IMF3954A	2N3954A	ITE2720	IT120	J112A	J112
FE202	2N3821	IMF3955	2N3955	ITE2721	IT122	J112A-1B	J112
FE204	2N3821	IMF3955A	2N3955A	ITE2722	IT120	J113	J113
FE300	2N3822	IMF3956	2N3956	ITE2903	IT122	J113-1B	J113
FE302	2N3821	IMF3957	2N3957	ITE2913	IT122	J113A	J113
FE304	2N3821	IMF3958	2N3958	ITE2914	IT122	J113A-1B	J113
FE3819	2N5484	IMF5911	IMF5911	ITE2915	IT120	J114	2N5555
FE4302	2N5457	IMF5912	IMF5912	ITE2916	IT120	J1401	IT501
FE4303	2N5459	IMF6465	IMF6465	ITE2917	IT122	J1402	IT502
FE4304	2N5459	IT100	IT100	ITE2918	IT122	J1403	IT503
FE5245	2N4416	IT101	IT101	ITE2919	IT120	J1404	IT503
FE5246	2N4494	IT106	ITE4418	ITE2920	IT120	J1405	IT504
FE5247	2N5486	IT109	ITE4418	ITE2936	IT120	J1406	IT505
FE5457	2N5457	IT120	IT120	ITE2937	IT120	J174	J174
FE5458	2N5458	IT120A	IT120A	ITE2972	IT122	J174-1B	J174
FE5459	2N5459	IT121	IT121	ITE2973	IT122	J175	J175
FE5464	2N5484	IT122	IT122	ITE2974	IT122	J175-1B	J175
FE5465	2N5485	IT124	IT124	ITE2975	IT120	J176	J176
FE5466	2N5486	IT126	IT126	ITE2976	IT120	J176-1B	J176

DISCRETE CROSS REFERENCE (cont.)



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
J177	J177	K309-18	J309	LS5105	2N5486	MD7002B	IT122
J177-18	J177	K310-18	J310	LS5245	ITE4416	MD7003	IT132
J201	J201	KE3684	2N3684	LS5245	2N5484	MD7003A	IT132
J201-18	J201	KE3685	2N3685	LS5247	2N5486	MD7003B	IT132
J202	J202	KE3686	2N3686	LS5248	2N5486	MD7004	IT128
J202-18	J202	KE3687	2N3687	LS5358	J204	MD7007	IT128
J203	J203	KE3623	2N3623	LS5359	J204	MD7007A	IT128
J203-18	J203	KE3970	ITE4391	LS5360	J202	MD7007B	IT128
J204	J204	KE3871	ITE4392	LS5361	J202	MD708	IT128
J204-18	J204	KE3972	ITE4393	LS5362	J203	MD708A	IT128
J210	2N5387	KE4091	ITE4091	LS5393	J203	MD7088	IT128
J211	2N5397	KE4092	ITE4092	LS5394	J203	MD6001	IT120
J212	2N5397	KE4093	ITE4093	LS5391	2N4867A	MD8002	IT122
J230	2N4867	KE4220	2N5457	LS5392	2N4868A	MD8003	IT122
J231	2N4868	KE4221	2N5458	LS5393	2N4868A	MD919	IT122
J292	2N4859	KE4222	2N5459	LS5394	2N4868A	MD918A	IT122
J270	J270	KE4223	J204	LS5395	2N4868A	MD8186	IT122
J270-18	J270	KE4391	ITE4391	LS5396	2N4868A	MD982	IT139
J271	J271	KE4392	ITE4392	LS5457	2N5457	MD984	IT139
J271-18	J271	KE4393	ITE4393	LS5458	2N5458	MEF103	2N5457
J300	2N5397	KE4416	ITE4416	LS5455	2N5458	MEF104	2N5459
J304	2N5486	KE4856	ITE4391	LS5494	2N5484	MEF3069	2N4341
J305	2N5484	KE4857	ITE4392	LS5485	2N5485	MEF3070	2N4339
J309	J309	KE4858	ITE4393	LS5486	2N5488	MEF3458	2N4341
J309	J309	KE4933	ITE4391	LS5556	2N3685	MEF3459	2N4339
J310	J310	KE4960	ITE4392	LS5557	2N3684	MEF3460	2N4338
J315	2N5397	KE4961	ITE4393	LS5558	2N3684	MEF3684	2N3684
J316	J316	KE5110	ITE4393	LS5559	2N5639	MEF3685	2N3685
J317	J317	KE5103	J204	LS5633	2N5639	MEF3686	2N3686
J3970	ITE4391	KE5104	ITE4416	LS5640	2N5640	MEF3687	2N3687
J3971	ITE4392	KE5105	ITE4416	M103	3N161	MEF3821	2N3821
J3972	ITE4393	KE5111	ITE4392	M104	3N161	MEF3822	2N3822
J401	IT501	KH5198	2N5198	M106	3N166	MEF3823	2N3823
J402	IT502	KH5197	2N5197	M107	3N189	MEF3854	2N3854
J403	IT503	KH5199	2N5199	M108	3N191	MEF3855	2N3855
J404	IT503	KH5199	2N5199	M113	3N161	MEF3956	2N3956
J405	IT504	LDF603	2N4221	M114	3N181	MEF3957	2N3957
J406	IT505	LDF604	2N4221	M116	M115	MEF3958	2N3958
J409-1	ITE4091	LDF605	2N4221	M117	2N4351	MEF4223	2N4223
J409-2	ITE4092	LM114	IT120	M119	3N161	MEF4224	2N4224
J409-3	ITE4093	LM114A	IT120A	M163	3N183	MEF4391	ITE4391
J410	IT502	LM114AH	IT120A	M164	3N154	MEF4392	ITE4392
J411	IT503	LM114H	IT120	M511	3N172	MEF4393	ITE4393
J416	IT505	LM115	IT120	M511A	3N172	MEF4416	ITE4416
J420	IT5911	LM115A	IT120A	M517	3N163	MEF4855	2N4855
J421	IT5912	LM115AH	IT120A	MA7807	IT132	MEF4857	2N4857
J4220	J204	LM115H	IT120	MA7809	IT132	MEF4858	2N4858
J4221	J202	LM194	IT120A	MAT-01AH	IT140	MEF4859	2N4859
J4222	J203	LM394	IT120A	MAT-01BH	IT140	MEF4860	2N4860
J4223	J202	LS3069	2N5458	MAT-01GH	IT140	MEF4861	2N4861
J4224	J202	LS3070	2N5458	MAT-01H	IT140	MEF5103	ITE4416
J430	J309(X2)	LS3071	2N5458	MD1120	IT122	MEF5104	ITE4416
J4302	2N4302	LS3459	J204	MD1121	IT122	MEF5105	ITE4416
J4303	2N5459	LS3459	J204	MD1122	IT122	MEF5245	ITE4416
J4304	2N5458	LS3460	J204	MD1123	IT139	MEF5246	2N5484
J431	J310(X2)	LS3684	2N3684	MD1129	IT129	MEF5247	2N5486
J433	2N5457	LS3685	2N3685	MD1130	IT139	MEF5248	2N5486
J4338	2N5457	LS3686	2N3686	MD2219	IT129	MEF5284	2N5484
J4339	2N5457	LS3687	2N3687	MD2219A	IT129	MEF5285	2N5485
J4391	ITE4391	LS3919	2N5484	MD2219	IT129	MEF5286	2N5486
J4392	ITE4392	LS3921	2N5457	MD2219A	IT129	MEF5561	J401
J4393	ITE4393	LS3922	2N5458	MD2369	IT128	MEF5562	J402
J4416	ITE4416	LS3923	2N5458	MD2369A	IT129	MEF5563	J403
J4655	ITE4655	LS3921	2N3921	MD2399B	IT122	MEM511	3N172
J4657	ITE4657	LS3922	2N3922	MD2904	IT139	MEM511A	3N172
J4858	ITE4858	LS3966	ITE4416	MD2904A	IT139	MEM511C	3N172
J4859	ITE4859	LS3967	ITE4416	MD2905	IT139	MEM517	3N172
J4860	ITE4860	LS3968	ITE4416	MD2905A	IT139	MEM517A	3N172
J4861	ITE4861	LS3969	ITE4416	MAT01BH	IT140	MEM517B	3N172
J4867	2N4857	LS4220	J204	MD2975	IT120	MEM517C	3N172
J4867A	2N4867A	LS4221	J202	MD2978	IT120	MEM550	3N189
J4867B	2N4867B	LS4222	J203	MD2979	IT120	MEM550C	3N189
J4868	2N4868	LS4223	J202	MD3009	IT120	MEM550F	3N189
J4868A	2N4868A	LS4224	J202	MD3250	IT132	MEM551	3N190
J4868B	2N4868B	LS4338	2N5457	MD3250A	IT131	MEM551C	3N189
J4868C	2N4868C	LS4339	2N5457	MD3251	IT132	MEM555	3N172
J4868D	2N4868D	LS4340	2N5457	MD3251A	IT131	MEM556C	3N172
J4868E	2N4868E	LS4341	2N5458	MD3409	IT129	MEM560	3N181
J5103	2N5484	LS4381	ITE4391	MD3410	IT129	MEM560C	3N181
J5104	2N5485	LS4392	ITE4392	MD3467	IT139	MEM561	3N163
J5105	2N5486	LS4393	ITE4393	MD3725	IT129	MEM561C	3N163
J6163	2N5486	LS4416	ITE4416	MD3762	IT139	MEM562	2N4351
K114-18	2N5555	LS4858	ITE4091	MD4957	IT132	MEM562C	2N4351
K210-18	2N5397	LS4857	ITE4092	MD5000	IT132	MEM583	2N4351
K211-18	2N5397	LS4859	ITE4093	MD5000A	IT132	MEM583C	2N4351
K212-18	2N5397	LS4859	ITE4091	MD5000B	IT132	MEM711	M116
K300-18	2N5397	LS4860	ITE4092	MD7000	IT129	MEM712	M116
K304-18	2N5486	LS4221	ITE4093	MD7001	IT139	MEM712A	M119
K305-18	2N5484	LS5103	2N5484	MD7002	IT139	MEM712B	3N170
K308-18	J308	LS5104	2N5485	MD7002A	IT122	MEM806	3N163

DISCRETE CROSS REFERENCE (cont.)

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
MEM806A	3N163	MP840	2N5520	NKT80111	2N4220	SA2718	IT122
MEM807	3N172	MP841	2N5521	NKT80112	2N4220	SA2719	IT120
MEM807A	3N172	MP842	2N5523	NKT80113	2N3821	SA2720	IT121
MEM814	3N161	MPF102	2N5486	NKT80211	2N4339	SA2721	IT122
MEM815	3N172	MPF103	2N5457	NKT80212	2N4339	SA2722	IT120
MEM817	3N172	MPF104	2N5458	NKT80213	2N4339	SA2723	IT121
MEM823	MF8223	MPF105	2N5459	NKT80214	2N4339	SA2724	IT122
MEM854	3N188	MPF106	2N5485	NKT80215	2N4339	SA2726	IT122
MEM854A	3N188	MPF107	2N5486	NKT80216	2N4339	SA2727	IT122
MEM854B	3N188	MPF108	2N5486	NKT80421	2N4220	SA2735	IT120A
MEM855	3N190	MPF109	2N5484	NKT80422	2N4220	SA2739	IT120
MEM855A	3N190	MPF111	2N5458	NKT80423	2N4220	SDF1001	2N5432
MEM855B	3N190	MPF112	2N5459	NKT80424	2N4220	SDF1002	2N5433
MF510	2N4082	MPF161	2N5398	NP0109	2N4584	SDF1003	2N5434
MF803	2N4338	MPF208	2N3821	NP0211N	2N4338	SDF500	2N5520
MF918	2N4858	MPF209	2N3821	NP0212N	2N4338	SDF501	2N5520
MF2000	2N4416	MPF255	IT6416	NP0213N	2N4338	SDF502	2N5520
MF2001	2N4416	MPF4391	IT64391	NP0214N	2N4338	SDF503	2N5520
MF2004	2N4093	MPF4392	IT64392	NP0215N	2N4339	SDF504	2N5520
MF2005	2N4082	MPF4393	IT64393	NP0216N	2N4339	SDF505	2N5520
MF2005	2N4091	MPF820	J310	NP05564	IT550	SDF506	2N3950
MF2007	2N4860	MPF870	J175	NP05565	IT550	SDF507	2N3950
MF2008	2N4859	MPF871	J175	NP05566	IT550	SDF508	2N3950
MF2009	2N4859	MTF101	2N5484	NP08301	2N3954	SDF509	2N3954
MF2010	2N4859	MTF102	2N5484	NP08302	2N3955	SDF510	2N3954
MF2011	2N5433	MTF103	2N5457	NP08303	2N3956	SDF512	2N3954
MF2012	2N5433	MTF104	2N5459	Q73	2N4338	SDF513	2N3954
MF2012	2N5434	ND5700	IT120A	P1004	2N5116	SDF514	2N3954
MF2093	2N4338	ND5701	IT120A	P1005	2N5115	SDF551	IT122
MF2094	2N4338	ND5702	IT120	P1027	2N5257	SDF552	IT122
MF2095	2N4340	NDF9401	IT500	P1028	2N5270	SDF663	IT122
MF2133	2N4860	NDF9402	IT501	P1029	2N5270	SES3819	2N5494
MF2012	2N5433	NDF9403	IT502	P1059E	2N5259	SFT801	2N4338
MF3002	3N170	NDF9404	IT504	P1066E	2N5115	SFT802	2N4338
MF3003	3N164	NDF9405	IT504	P1087E	2N5116	SFT803	2N4339
MF3020	3N186	NDF9406	IT500	P1117E	2N5540	SFT804	2N4338
MF3021	3N186	NDF9407	IT501	P1118E	2N5541	SL301AT	IT129
MF3027	2N3886	NDF9408	IT502	P1119E	2N5540	SL301BT	IT129
MF3028	2N3886	NDF9409	IT503	PF510	2N5114	SL301CT	IT129
MF3029	2N3886	NDF9410	IT504	PF5101	2N4867	SL301ET	IT129
MF4010	2N2608	NF3819	2N5484	PF5102	2N4867	SL380C	IT129
MF4011	2N2609	NF4202	2N5485	PF5103	2N5114	SL380E	IT129
MF4012	2N2609	NF4303	2N5459	PF511	2N4117A	SU2000	2N3954
MF4823	IT1700	NF4304	2N5458	PF5301	2N4118A	SU2020	2N3954
MK10	2N4416	NF4445	2N5432	PF5301-1	2N4117A	SU2021	2N3954
MMF1	2N5197	NF4446	2N5433	PF5301-2	2N4118A	SU2022	2N3954
MMF2	2N3921	NF4447	2N5438	PF5301-3	2N4118A	SU2023	2N3954
MMF3	2N5198	NF4448	2N5433	PL1081	2N3823	SU2024	2N3954
MMF4	2N3922	NF500	2N4224	PL1092	2N3823	SU2025	2N3954
MMF5	2N5199	NF501	2N4224	PL1093	2N3823	SU2026	2N3954
MMF5	2N5199	NF501	2N4224	PL1093	2N3823	SU2027	2N3954
MMT3823	2N3955A	NF506	2N4416	PL1094	2N3823	SU2027	2N3954
MP301	IT124	NF5101	2N4867	PN3664	2N3684	SU2028	2N3954
MP302	IT124	NF5102	2N4867	PN3685	2N3685	SU2029	2N3954
MP303	IT124	NF5103	2N4867	PN3686	2N3686	SU2029	2N5187
MP310	2N4045	NF511	2N4860	PN3687	2N3687	SU2030	2N3954
MP311	2N4045	NF5163	2N4341	PN4091	IT64091	SU2030	2N3955
MP312	2N4044	NF520	2N3684	PN4092	IT64092	SU2031	2N3954
MP313	IT124	NF521	2N3685	PN4093	IT64093	SU2031	2N5188
MP318	IT120A	NF522	2N3686	PN4220	J204	SU2032	2N3954
MP318	IT120A	NF523	2N3685	PN4221	J202	SU2033	2N3954
MP350	IT132	NF330	2N4341	PN4222	J203	SU2034	2N3954
MP351	IT130	NF3301	2N4118A	PN4223	J204	SU2034	2N3954
MP352	IT130	NF3301-1	2N4117A	PN4224	J202	SU2035	2N3954
MP358	IT130A	NF3301-2	2N4118A	PN4342	2N5461	SU2036	2N3954
MP360	IT132	NF3301-3	2N4118A	PN4360	2N5460	SU2074	2N3954
MP361	IT130A	NF331	2N4339	PN4391	IT64391	SU2075	2N3954
MP362	IT130A	NF332	2N4339	PN4392	IT64392	SU2076	2N3954
MP3954	2N3954A	NF333	2N4338	PN4416	IT64416	SU2077	2N3954
MP3954A	2N3954A	NF5457	2N5457	PN4856	2N4856	SU2077	2N3955
MP3955	2N3955	NF5458	2N5458	PN4857	2N4857	SU2078	2N3955
MP3955	2N3956	NF5459	2N5459	PN4858	2N4858	SU2078	2N3955
MP3957	2N3957	NF5484	2N5484	PN4859	2N4859	SU2079	2N3955
MP3958	2N3958	NF5485	2N5485	PN4860	2N4860	SU2081	U404
MP5905	2N5905	NF5486	2N5486	PN4861	2N4861	SU2088	2N5197
MP5906	2N5906	NF5555	2N5484	PN5033	2N5460	SU2098A	2N5197
MP5907	2N5907	NF5638	2N5638	PTC151	2N5484	SU2098B	2N5186
MP5908	2N5908	NF5639	2N5639	PTC152	2N5485	SU2099	2N5197
MP5909	2N5909	NF5640	2N5640	SA2253	IT122	SU2099A	2N5197
MP5911	2N5911	NF5653	2N4860	SA2254	IT122	SU2365	2N3954
MP5912	2N5912	NF5654	2N4861	SA2255	IT122	SU2365A	2N3954
MP804	2N5520	NF580	2N5432	SA2644	IT120	SU2365	2N3955
MP830	2N5520	NF581	2N5432	SA2648	IT120	SU2365A	2N3955
MP831	2N5521	NF582	2N5433	SA2710	IT120	SU2367	2N3955
MP832	2N5522	NF583	2N5434	SA2711	IT120	SU2367A	2N3956
MP833	2N5523	NF584	2N5433	SA2712	IT121	SU2368	2N3956
MP835	2N3954	NF585	2N4859	SA2713	IT121	SU2368A	2N3956
MP836	2N3955	U310	U310	SA2714	IT122	SU2369	2N3957
MP837	2N3956	NF8432	U310	SA2715	IT120	SU2369A	2N3957
MP838	2N3956	NF8433	U310	SA2716	IT120	SU2411	2N3957
MP839	2N3957	NF8454	U310	SA2717	IT121	SU2411	2N3958

DISCRETE CROSS REFERENCE (cont.)



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
SU2412	2N5908	TD5909A	2N5909	U183	2N3824	U405	U405
SU2552	U401	TD5911	2N5911	U1837E	2N5486	U406	U406
SU2552M	U401	TD5911A	2N5911	U184	2N5397	U410	2N3959
SU2553	U401	TD5912	2N5912	U1857E	U1857	U411	2N3959
SU2553M	U401	TD5912A	2N5912	U1859E	U1859	U412	2N3959
SU2554	U401	TD700	IT122	U1899E	U1899	U421	2N5908
SU2554M	U401	TD701	IT122	U1897	2N4338	U422	2N5908
SU2555	U402	TD706	IT122	U186	2N4340	U423	2N5909
SU2555M	U402	TD710	IT122	U185	2N4341	U424	2N6009
SU2555M	U404	TD711	IT122	U1994E	2N4416	U425	2N5908
SU2658M	U404	TD713	IT122	U200	2N4661	U428	2N5909
SX3819	2N5484	TS14	2N4540	U201	2N4560	U430	J306(X2)
SX3820	2N2608	TS25	2N3854	U202	2N4858	U431	J310(X2)
TD100	IT129	TS26	2N3854	U2047E	2N4416	U440	IT5911
TD101	IT129	TS27	2N3855	U221	2N4361	U441	IT5912
TD102	IT129	TS34	2N5486	U222	2N4991	UC100	2N3884
TD200	IT129	TS41	2N4959	U231	U231	UC110	2N3885
TD201	IT129	TS42	2N4393	U232	U232	UC115	2N4340
TD202	IT129	TS59	2N5484	U233	U233	UC120	2N3886
TD219	IT129	TS59	2N5486	U234	U234	UC130	2N3887
TD224	IT122	TS69	2N3955A	U235	U235	UC155	2N4416
TD225	IT122	TS69	2N3955A	U240	2N5432	UC1700	3N163
TD225	IT122	TS70	2N3956	U241	2N5433	UC1754	3N163
TD227	IT122	TS73	ITE4361	U242	2N5432	UC20	2N3886
TD228	IT122	TS74	ITE4362	U243	2N5433	UC200	2N3884
TD229	IT122	TS75	ITE4363	U244	2N5433	UC201	2N3884
TD230	IT121	TS89	2N4416	U248	2N5902	UC21	2N3887
TD231	IT121	TS8A	2N4416	U25A	2N5906	UC10	2N4416
TD232	IT122	TXS33	2N4392	U249	2N5902	UC2130	2N5453
TD233	IT122	TXS53	2N4857	U249A	2N5807	UC2132	2N5453
TD234	IT122	TXS36	2N4381	U250	2N5904	UC2134	2N5454
TD235	IT122	TXS41	2N4859	U250A	2N5908	UC2136	2N5454
TD236	IT122	TXS42	2N6339	U251	2N5905	UC2138	2N5454
TD237	IT122	TXS53	2N5459	U251A	2N5908	UC2139	2N5454
TD238	IT122	TXS79	2N4341	U252	IT5911	UC2147	2N3958
TD239	IT122	TXS79	2N4341	U253	IT5912	UC2148	2N3958
TD240	IT121	TN4117	2N4117	U254	2N4859	UC2149	2N3958
TD241	IT121	TN4117A	2N4117A	U255	2N4859	UC220	2N3822
TD242	IT120A	TN4118	2N4118	U255	2N4859	UC240	2N4969
TD243	IT120A	TN4118A	2N4118A	U257	U257	UC241	2N4869
TD244	IT129	TN4119	2N4119	U257/TO-71	U257/TO-71	UC250	2N4081
TD245	IT129	TN4119A	2N4119A	U266	2N4856	UC251	2N4392
TD246	IT129	TN4339	2N4339	U273	2N4118A	UC2755	3N166
TD247	IT129	TN4340	2N4340	U273A	2N4118A	UC300	2N2608
TD248	IT129	TN4340	2N4340	U274	2N4118A	UC310	2N2607
TD250	IT120A	TN4341	2N4341	U274A	2N4118A	UC320	2N2607
TD2505	IT139	TN5277	2N4341	U275	2N4118A	UC330	2N2607
TD400	IT139	TN5278	2N4341	U275A	2N4118A	UC340	2N2607
TD401	IT139	TP5114	2N5114	U280	2N5452	UC40	2N6908
TD402	IT139	TP5115	2N5115	U281	2N5453	UC400	2N5270
TD500	IT139	TP5116	2N5116	U282	2N5453	UC401	2N5116
TD501	IT139	TP5116	2N5116	U283	2N5453	UC41	2N2608
TD502	IT139	TP5116	2N5116	U284	2N5453	UC410	2N5266
TD509	IT132	U112	2N2608	U285	2N5454	UC420	2N5267
TD510	IT132	U113	2N2608	U290	2N5432	UC430	2N5114
TD511	IT132	U114	2N2608	U291	2N5434	UC451	2N5116
TD512	IT132	U1177	2N4220	U295	2N5432	UC588	2N4416
TD513	IT132	U1179	2N3921	U296	2N5434	UC709	2N4220
TD514	IT132	U1179	2N3921	U300	2N5114	UC704	2N4220
TD517	IT132	U1180	2N4221	U3000	2N4341	UC705	2N4224
TD518	IT132	U1181	2N4220	U3001	2N4339	UC707	2N4880
TD519	IT132	U1182	2N3821	U3002	2N4338	UC714	2N3822
TD520	IT139	U1277	2N3684	U301	2N5115	UC714E	2N4341
TD521	IT139	U1279	2N3685	U3010	2N4341	UC734	2N4416
TD522	IT139	U1279	2N3685	U3011	2N4340	UC734E	2N4416
TD523	IT139	U1280	2N3684	U3012	2N4338	UC751	2N4340
TD524	IT139	U1281	2N3822	U304	U304	UC752	2N4340
TD525	IT132	U1284	2N4341	U305	U305	UC753	2N4341
TD526	IT132	U1283	2N4340	U306	U306	UC754	2N4341
TD527	IT131	U1284	2N4341	U308	U308	UC755	2N4341
TD529	IT131	U1285	2N4220	U309	U309	UC756	2N4340
TD5432	2N5432	U1286	2N4341	U310	U310	UC805	2N5270
TD5433	2N5433	U1287	2N4022	U311	U311	UC807	2N5115
TD5434	2N5434	U1321	2N4859	U312	2N5397	UC814	2N5270
TD550	IT129	U1322	2N3922	U314	2N5555	UC851	2N2608
TD5902	2N5902	U1323	2N3822	U315	2N5397	UC853	2N2608
TD5902A	2N5902	U1324	2N3857	U316	U309	UC854	2N2608
TD5903	2N5903	U1325	2N3886	U317	U310	UC855	2N2609
TD5903A	2N5903	U133	2N2608	U320	2N5433	UT100	2N5397
TD5904	2N5904	U1420	2N3921	U321	2N5434	UT101	2N5397
TD5904A	2N5904	U1421	2N3922	U322	2N5433	UXC2910	IT126
TD5905	2N5905	U1422	2N3822	U328	**	VCR10N	2N4889
TD5905A	2N5905	U146	2N2608	U329	**	VCR11N	VNR11N
TD5906	2N5906	U147	2N2608	U330	**	VCR12N	2N3958
TD5906A	2N5906	U148	2N2608	U331	**	VCR13N	2N3958
TD5907	2N5907	U148	2N2609	U330	**	VCR20N	2N4341
TD5907A	2N5907	U149	2N2609	U401	U401	VCR2N	VCR2N
TD5908	2N5908	U1714	2N4340	U402	U402	VCR2P	VCR2P
TD5908A	2N5908	U1715	2N4340	U403	U403	VCR4N	VCR4N
TD5909	2N5906	U182	2N4857	U404	U404	VCR5P	VCR5P

ANALOG SWITCH CROSS REFERENCE (cont.)



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
DG509CJ DGM111AL DGM111AP DGM111BP G115AP	IHS208CPE DG111AL DG111AK G111BK G115AK	H11-5041-5 H11-5041-8 H11-5042-2 H11-5042-5 H11-5042-8	IHS041CJE IHS041MJE/883B IHS042MJE IHS043CJE IHS142MJE/883B	TL182CN TL182L TL182LN TL182ML TL185CJ	DGM182CJ DGM182BA DGM182CJ DGM182AA IHS043CJE		
G1158P G1158P G116AP G116BP	G1158J G1158K G116AK G1168J	H11-5043-2 H11-5043-5 H11-5044-2 H11-5044-5	IHS143MJE IHS143CJE IHS144MJE/883B IHS144MJE IHS144CJE	TL185CN TL185J TL185IN TL185MJ TL188CL	IHS045CPE IHS045CJE IHS045CPE IHS045MJE IHS042CTW		
G1168P G117AL G116AL G118AP G118AL	G1168K G117AL G116AL G116AK G116AL	H11-5044-8 H11-5045-2 H11-5045-5 H11-5045-8 H11-5046-2	IHS144MJE/883B IHS145MJE IHS145CJE IHS145MJE/883B IHS046MJE	TL188CN TL188L TL188IN TL188ML TL191CJ	IHS042CPE IHS042CTW IHS042CPE IHS042MTW IHS043CJE		
G123AL G123AP H10-0201-5 H10-0381-5 H10-0384-5	G123AL G123AK DG201C/D DGM181C/D DGM184C/D	H11-5046-5 H11-5046-8 H11-5047-2 H11-5047-5 H11-5047-8	IHS046CJE IHS046MJE/883B IHS047MJE IHS047CJE IHS047MJE/883B	TL191CN TL191J TL191IN TL191MJ	IHS043CPE IHS043CJE IHS043CPE IHS043MJE		
H10-0387-5 H10-0390-5 H10-0505-5 H10-0508A-5 H10-0507-5	DGM187C/D DGM190C/D IHS118C/D IHS118C/D IHS218C/D	H11-5049-2 H11-5049-5 H11-5049-8 H11-5050-2 H11-5050-5	IHS149MJE IHS149CJE IHS149MJE/883B IHS150MJE IHS150CJE				
H10-0507A-5 H10-0508-5 H10-0508A-5 H10-0509-5 H10-0509A-5	IHS218C/D IHS108C/D IHS108C/D IHS208C/D IHS208C/D	H11-5050-8 H11-5051-2 H11-5051-5 H11-5051-8 H12-0200-2	IHS150MJE/883B IHS151MJE IHS151CJE IHS151MJE/883B DG200AA				
H10-5040-5 H10-5041-5 H10-5042-5 H10-5043-5 H10-5044-5	IHS140C/D IHS141C/D IHS142C/D IHS143C/D IHS144C/D	H12-0200-4 H12-0200-5 H12-0200-8 H12-0381-2 H12-0381-5	DG200BA DG200BA DG200AA/883B DGM187AA DGM181BA				
H10-5045-5 H10-5046-5 H10-5047-5 H10-5049-5 H10-5050-5	IHS145C/D IHS046C/D IHS047C/D IHS149C/D IHS150C/D	H12-0381-8 H12-0387-5 H12-0387-5 H12-0387-8 H12-0200-5	DGM181AA/883B DGM187BA DGM187BA DGM188AA/883B DG200CJ				
H10-5051-5 H11-0200-2 H11-0200-4 H11-0200-5 H11-0200-5	IHS051C/D DG200AK DG200BK DG200BK DG200C/D	H13-0201-5 H13-0381-5 H13-0384-5 H13-0390-5 H13-0505-5	DG201CJ DGM181CJ DGM184CJ DGM190CJ IHS116CPI				
H11-0200-8 H11-0201-2 H11-0201-4 H11-0201-5 H11-0201-8	DG200AK/883B DG201AK DG201BK DG201BK DG201AK/883B	H13-0506A-5 H13-0507-5 H13-0507A-5 H13-0508-5 H13-0508A-5	IHS116CPI IHS216CPI IHS216CPI IHS108CPE IHS108CPE				
H11-0381-2 H11-0381-5 H11-0381-8 H11-0384-5 H11-0384-5	DGM182AK DGM181BK DGM182AK/883B DGM182AK DGM184BK	H13-0509-5 H13-0509A-5 LF11201D LF11201D/883B LF11202D	IHS208CPE IHS208CPE DG201AK DG201AK/883B IHS202MJE				
H11-0384-8 H11-0387-2 H11-0387-5 H11-0387-8 H11-0390-2	DGM185AK/883B DGM188AK DGM187BK DGM188AK/883B DGM191AK	LF11202D/883B LF11508D LF11508D/883B LF11508D LF11509D/883B	IHS202MJE/883B IHS109MJE IHS109MJE/883B IHS208MJE IHS208MJE/883B				
H11-0390-5 H11-0390-8 H11-0506-2 H11-0506-5 H11-0506-5	DGM190BK DGM191AK/883B IHS116MJ IHS116CJ IHS116MJ/883B	LF13201D LF13201N LF13202D LF13508D LF13508N	DG201BK DG201CJ IHS202CJE IHS108CJE IHS108CPE				
H11-0506A-2 H11-0506A-5 H11-0506A-5 H11-0507-2 H11-0507-5	IHS118MJ IHS118MJ IHS118MJ/883B IHS216MJ IHS216CJ	LF13509C LF13509N MM450H MM451H MM452D	IHS208CJE IHS208CPE MM450H MM451H MM452J				
H11-0507-8 H11-0507A-2 H11-0507A-5 H11-0507A-8 H11-0508-2	IHS216MJ/883B IHS216MJ IHS216MJ IHS216MJ/883B IHS108MJE	MM452F MM455H MM550H MM551H MM552D	MM452F MM455H MM550H MM551H MM552J				
H11-0508-5 H11-0508-8 H11-0508A-2 H11-0508A-5 H11-0508A-8	IHS108CJE IHS108MJE/883B IHS108MJE IHS108MJE IHS108MJE/883B	MM552F MM555H SJM1818CC SJM1818IC SJM1828CC	MM552F MM555H JM38510/111018CC JM38510/111018IC JM38510/111028CC				
H11-0509-2 H11-0509-5 H11-0509-8 H11-0509A-2 H11-0509A-5	IHS208MJE IHS208CJE IHS208MJE/883B IHS208MJE IHS208MJE	SJM1828IC SJM18485C SJM18585C SJM18785CC SJM1878IC	JM38510/111028IC JM38510/1110385C JM38510/1110485C JM38510/1110585C JM38510/1110685C				
H11-0509A-8 H11-5040-2 H11-5040-5 H11-5040-8 H11-5041-2	IHS208MJE/883B IHS040MJE IHS040CJE IHS040MJE/883B IHS041MJE	SJM1888CC SJM1888IC SJM18085C SJM18185C TL182CL	JM38510/111068CC JM38510/111068IC JM38510/1110785C JM38510/1110885C DGM182BA				

DATA ACQUISITION CROSS REFERENCE



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
AD7520JD AD7520JN AD7520KD AD7520KN AD7520LD	AD7520JD AD7520JN AD7520KD AD7520KN AD7520LD	MP7521LN MP7521SD MP7521TD MP7521UD MP7523JN	AD7521LN AD7521SD AD7521TD AD7521UD AD7523JN				
AD7520LN AD7520SD AD7520TD AD7520UD AD7521JD	AD7520LN AD7520SD AD7520TD AD7520UD AD7521JD	MP7523KN MP7523LN MP7521AD MP7521BD MP7521JN	AD7523KN AD7523LN AD7541AD AD7541BD AD7541JN				
AD7521JN AD7521KD AD7521KN AD7521LD AD7521LN	AD7521JN AD7521KD AD7521KN AD7521LD AD7521LN	MP7521KN MP7521SD MP7521TD	AD7541KN AD7541SD AD7541TD				
AD7521SD AD7521TD AD7521UD AD7523AD AD7523BD	AD7521SD AD7521TD AD7521UD AD7523AD AD7523BD						
AD7523CD AD7523JN AD7523KN AD7523LN AD7523SD	AD7523CD AD7523JN AD7523KN AD7523LN AD7523SD						
AD7523TD AD7523UD AD7530JD AD7530JN AD7530KD	AD7523TD AD7523UD AD7530JD AD7530JN AD7530KD						
AD7530KN AD7530LD AD7530LN AD7531JD AD7531JN	AD7530KN AD7530LD AD7530LN AD7531JD AD7531JN						
AD7531KD AD7531KN AD7531LD AD7531LN AD7533AD	AD7531KD AD7531KN AD7531LD AD7531LN AD7533AD						
AD7533BD AD7533CD AD7533JN AD7533KN AD7533LN	AD7533BD AD7533CD AD7533JN AD7533KN AD7533LN						
AD7533SD AD7533TD AD7533UD AD7541AD AD7541BD	AD7533SD AD7533TD AD7533UD AD7541AD AD7541BD						
AD7541JN AD7541KN AD7541SD AD7541TD DAC1020LCD	AD7541JN AD7541KN AD7541SD AD7541TD AD7520LD						
DAC1020LD DAC1021LCD DAC1021LD DAC1022LCD DAC1022LD	AD7520UD AD7520KD AD7520TD AD7520JD AD7520SD						
DAC1218LCD DAC1218LCN DAC1218LCD DAC1219LCD DAC1219LCN	AD7541BD AD7541KN AD7541LN AD7541AD AD7541JN						
DAC1220LCD DAC1220LD DAC1221LCD DAC1221LD DAC1222LCD	AD7521LD AD7521UD AD7521KD AD7521TD AD7521JD						
DAC1222LD MP7520LD MP7520JN MP7520KD MP7520KN	AD7521SD AD7520JD AD7520JN AD7520KD AD7520KN						
MP7520LD MP7520LN MP7520SD MP7520TD MP7520UD	AD7520LD AD7520LN AD7520SD AD7520TD AD7520UD						
MP7521JD MP7521JN MP7521KD MP7521KN MP7521LD	AD7521JD AD7521JN AD7521KD AD7521KN AD7521LD						

**CONSULT FACTORY

A

WATCH & CLOCK CROSS REFERENCE

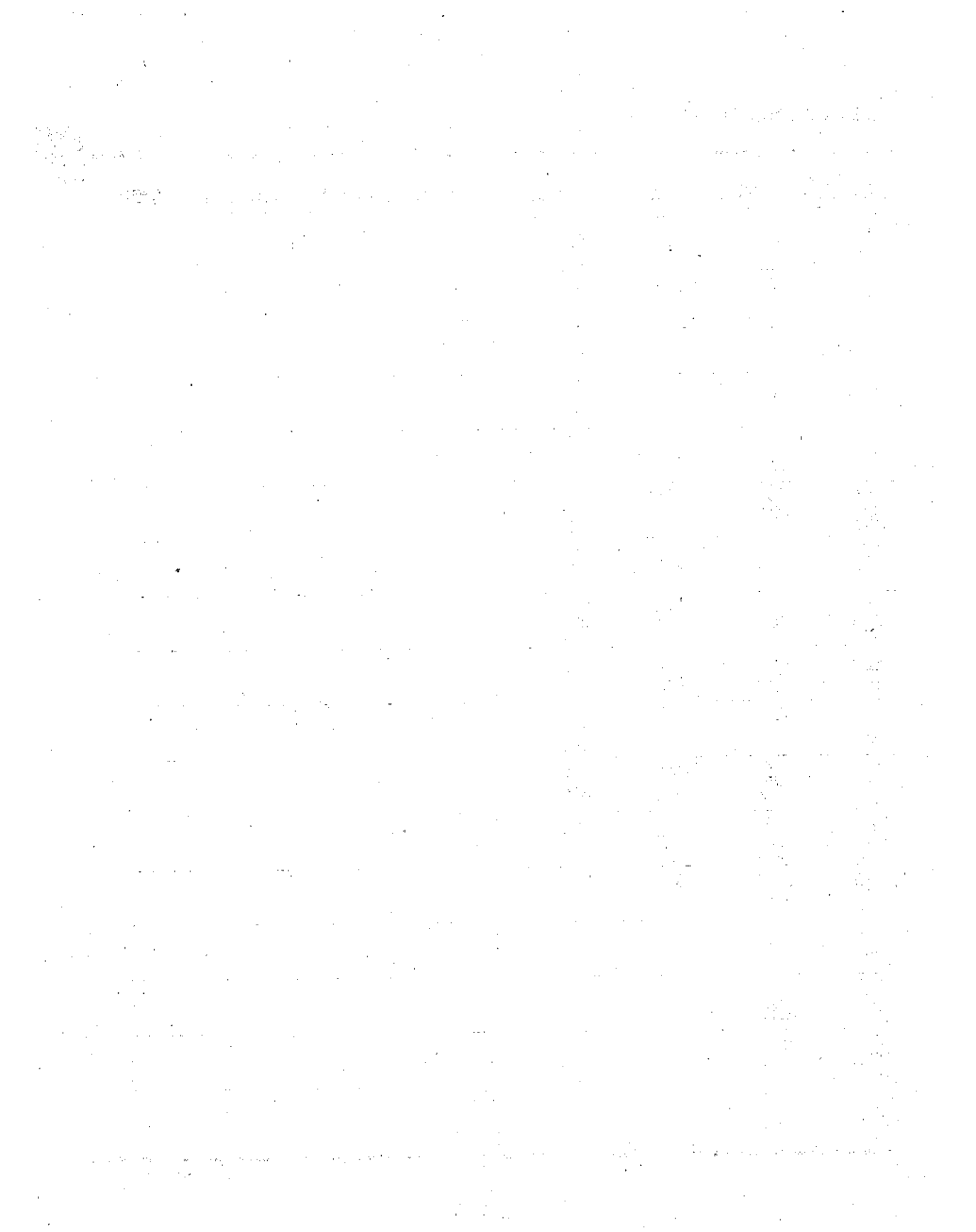
ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
CD22001H CD22015E E1115 E1151 E1426	ICM1424C ICM7051A ICM1115A ICM1115B ICM7050U						
HD43871 HD43871 K55189 K55240B01H K55240B01J	ICM7050G ICM7050H ICM7269 ICM7245B ICM7245A						
K55240B1GH K55240B12H K55240B20H K55240UD1E M5001	ICM7245D ICM7245E ICM7245F ICM7245U ICM7269						
M5B434P M5B435P M5B437-001P MB101	ICM7038D ICM1115B ICM7050G ICM7070L ICM7245B						
MB103 MB105 MB107 MB108 MB143	ICM7245E ICM7245U ICM7245D ICM7245E ICM7245A						
MB144 MB510 MB511 MB512 MB513	ICM7245F ICM1115B ICM7050H ICM7050H ICM7050G						
MB521 MB522 MB531 MB533 MB541	TS9088 TS9088 ICM7050H ICM7050H ICM7052						
MB542 MB7B MCC14440 MCC14493 ML41	ICM7052 ICM7245U ICM1424C ICM7210 ICM1424C						
MJ6 MNB081 MNB082A MNB093 MNB252	ICM7220 ICM7038B ICM7038E ICM7051A ICM7050G						
M5M8001 M5M5011 M5M5977 S1424 SCL54301	ICM7269 ICM1424C ICM1424C ICM1424C ICM1424C						
SDL547B SM5011 SM5510 SM5530B TC8031P	ICM7269 ICM7050G ICM1115B ICM7070P ICM7039A						
TC8032P TC8051P TC8052P TC8056PA TC8057P	ICM7038F ICM7038B ICM7038E ICM1115B ICM7039D						
UCN-4111M UCN-4112M UCN-4113M UPD1952P UPD1962C	ICM7039C ICM7051A ICM7039B ICM7220MFA ICM7050G						
UPD1963C UPD815C UPD816C UPD820C UPD833C	ICM7050 ICM7038E ICM7038E ICM1115B ICM7223						

LINEAR CROSS REFERENCE



ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
723 738 741 748 AD101	UA723 UA733 UA741 UA748 LM101	MC1741 MC1745 MH-W590 MP55010 NE590	UA741 UA748 AD590 ICL8068 AD590				
AD108 AD301 AD308 AD503 AD532	LM108 LM301 LM308 AD503 AD532	NE592 OP-05 OP-07 OP-08 PM308	NE592 OP-05 OP-07 OP-08 LM308				
AD534 AD590 AD741 AM2502 AM2503	AD534 AD590 UA741 AM2502 AM2503	RC723 RC733 RC741 RC748 RM723	UA723 UA733 UA741 UA748 UA723				
AM2504 AM5402 AM5402 CA101 CA107	AM2504 HA2505 HA2525 LM101 LM107	RM741 RM748 SC748 SG101 SG105	UA741 UA748 UA748 LM101 LM105				
CA111 CA301 CA307 CA309 CA311	LM111 LM301 LM307 LM308 LM311	SG107 SG108 SG110 SG111 SG2502	LM107 LM108 LM110 LM111 AM2502				
CA723 CA741 CA748 DG503 DM2502	UA723 UA741 UA748 AD503 AM2502	SG2503 SG301 SG305 SG307 SG308	AM2503 LM301 LM305 LM307 LM308				
DM2503 DM2504 HA2500 HA2502 HA2505	AM2503 AM2504 HA2500 HA2502 HA2505	SG311 SG4250 SG723 SG733 SG741	LM311 LM4250 UA723 UA733 UA741				
HA2507 HA2510 HA2512 HA2515 HA2517	HA2507 HA2510 HA2512 HA2515 HA2517	SG748 SG5741 SU535 TL509 TL592	UA748 UA741 SU536 AD503 NE592				
HA2520 HA2522 HA2525 HA2527 HA2530	HA2520 HA2522 HA2525 HA2527 HA2530	TT-590 UA101 UA102 UA109 UA107	AD590 LM101 LM102 LM105 LM107				
HA2602 HA2605 HA2607 HA2620 HA2622	HA2602 HA2605 HA2607 HA2620 HA2622	UA108 UA110 UA111 UA301 UA302	LM108 LM110 LM111 LM301 LM302				
HA2625 HA2627 HA2720 LH0042 LH2101	HA2625 HA2627 ICL8021 LH0042 LH2101	UA305 UA307 UA308 UA310 UA311	LM305 LM307 LM308 LM310 LM311				
LH2108 LH2110 LH2111 LH2301 LH2308	LH2108 LH2110 LH2111 LH2301 LH2308	UA723 UA733 UA740 UA741 UA748	UA723 UA733 UA740 UA741 UA748				
LH2310 LH2311 LM100 LM101 LM102	LH2310 LH2311 LM100 LM101 LM102	UA777 UHP-503 VR-8068 WG-8038 XR6038	UA777 AD503 ICL8068 ICL8038 ICL8038				
LM105 LM107 LM108 LM110 LM111	LM105 LM107 LM108 LM110 LM111						
LM300 LM301 LM302 LM305 LM307	LM300 LM301 LM302 LM305 LM307						
LM308 LM310 LM311 LM4250 LM723	LM308 LM310 LM311 LM4250 UA723						
LM738 LM740 LM741 LM748 MC1723	UA738 UA740 UA741 UA748 UA723						

**CONSULT FACTORY



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Switches — Junction FET

Ordering Information		r _{DS(on)} max Ω	V _p min/max V		I _{DSS} max μA	BV _{DSS} min V	I _{D(off)} max μA	I _{DSS} min/max mA	t _{total} max ns	C _{iss} max pF	C _{rss} max pF	
Preferred Part Number	Package											
N-channel: Generally requires driver circuit to translate the popular logic levels to voltages required to drive the JFET.												
2N3970	TO-18	30	-4.0	-10.0	(-250)	-40	250	50	150	50	25	6.0
2N3971	TO-18	60	-2.0	-5.0	(-250)	-40	250	25	75	90	25	6.0
2N3972	TO-18	100	-0.5	-3.0	(-250)	-40	250	5	30	180	25	6.0
2N4091	TO-18	30	-5.0	-10.0	-200	-40	200	30		65	16	5.0
2N4092	TO-18	50	-2.0	-7.0	-200	-40	200	15		95	16	5.0
2N4093	TO-18	80	-1.0	-5.0	-200	-40	200	8		140	16	5.0
2N4391	TO-18	30	-4.0	-10.0	-100	-40	100	50	150	55	14	3.5
2N4392	TO-18	60	-2.0	-5.0	-100	-40	100	25	75	75	14	3.5
2N4393	TO-18	100	-0.5	-3.0	-100	-40	100	5	30	100	14	3.5
2N4856	TO-18	25	-4.0	-10.0	-250	-40	250	50		34	18	8.0
2N4857	TO-18	40	-2.0	-6.0	-250	-40	250	20	100	60	18	8.0
2N4858	TO-18	60	-0.8	-4.0	-250	-40	250	8	80	120	18	8.0
2N4859	TO-18	25	-4.0	-10.0	-250	-30	250	50		34	18	8.0
2N4860	TO-18	40	-2.0	-6.0	-250	-30	250	20	100	60	18	8.0
2N4861	TO-18	60	-0.8	-4.0	-250	-30	250	8	80	120	18	8.0
2N5432	TO-52	5	-4.0	-10.0	-200	-25	200	150		41	30	15.0
2N5433	TO-52	7	-3.0	-9.0	-200	-25	200	100		41	30	15.0
2N5434	TO-52	10	-1.0	-4.0	-200	-25	200	30		41	30	15.0
2N5638	TO-92	30		-12.0	-1nA	-30	1nA	50		24	10	4.0
2N5639	TO-92	60		-8.0	-1nA	-30	1nA	25		44	10	4.0
2N5640	TO-92	100		-6.0	-1nA	-30	1nA	5		63	10	4.0
ITE4091	TO-92	30+	-5.0	-10.0	-200	-40	200	30		65	16	5.0
ITE4092	TO-92	50	-2.0	-7.0	-200	-40	200	15		95	16	5.0
ITE4093	TO-92	80	-1.0	-5.0	-200	-40	200	8		140	16	5.0
ITE4391	TO-92	30	-4.0	-10.0	-100	-40	100	50	150	55	14	3.5
ITE4392	TO-92	60	-2.0	-5.0	-100	-40	100	25	75	75	14	3.5
ITE4393	TO-92	100	-0.5	-3.0	-100	-40	100	5	30	100	14	3.5
J105	TO-92	3	-4.5	-10.0	-3nA	-25	3nA	500	—	60	(70)	(3.5)
J106	TO-92	6	-2.0	-6.0	-3nA	-25	3nA	200	—	60	(70)	(3.5)
J107	TO-92	8	-0.5	-4.5	-3nA	-25	3nA	100	—	60	(70)	(3.5)
J111	TO-92	30	-3.0	-10.0	-1nA	-35	1nA	20		48	(16)	(5.0)
J112	TO-92	50	-1.0	-5.0	-1nA	-35	1nA	5		48	(16)	(5.0)
J113	TO-92	100	-0.5	-3.0	-1nA	-35	1nA	2		48	(16)	(5.0)
P-channel:												
2N3993	TO-72	150	4.0	9.5	1.2nA	25	1.2nA	-10.0			16	4.5
2N3994	TO-72	300	1.0	5.5	1.2nA	25	1.2nA	-2.0			16	4.5
2N5114	TO-18	75	5.0	10.0	500	30	500	-30.0	-90	37	25	7.0
2N5115	TO-18	100	3.0	6.0	500	30	500	-15.0	-60	68	25	7.0
2N5116	TO-18	150	1.0	4.0	500	30	500	-5.0	-25	102	25	7.0
IT100	TO-18	75	2.0	4.5	200	35	100	-10.0			35	12.0
IT101	TO-18	60	4.0	10.0	200	35	100	-20.0			35	12.0
J174	TO-92	85	5.0	10.0	1nA	30	-1nA	-20.0	-100	22	(25)	(8.0)
J175	TO-92	125	3.0	6.0	1nA	30	-1nA	-7.0	-60	45	(25)	(8.0)
J176	TO-92	250	1.0	4.0	1nA	30	-1nA	-2.0	-25	70	(25)	(8.0)
J177	TO-92	300	0.8	2.25	1nA	30	-1nA	-1.5	-20	90	(25)	(8.0)
J270	TO-92	—	0.5	2.0	200	30	—	-2.0	-15	—	32 typ.	4.0 typ.
J271	TO-92	—	1.5	4.5	200	30	—	-6.0	-50	—	32 typ.	4.0 typ.
P1086	TO-92	75	—	10.0	2nA	30	-10nA	-10.0	—	100	45	10.0
P1087	TO-92	150	—	5.0	2nA	30	-10nA	-5.0	—	215	45	10.0

() Approximate Value

Switches and Amplifiers — MOSFET

Ordering Information		$V_{GS(TH)}$		BV_{GSS} min V	I_{DSS} max pA	I_{GSS} max pA	G_{fs} min μ mho	$r_{DS(ON)}$ max Ω	I_D min/max mA	
Preferred Part Number	Package	$V_{GS(OFF)}$ min/max V	$V_{GS(ON)}$ min/max V							
P-Channel Enhancement: Gen. used where max isolation between signal source and logic drive required; sw: "On" resistance varies with signal amplitude.										
3N161	T0-72	-1.5	-5.0	-25	-10nA	-100.0	3500.0	(125)	-40	-120 Diode Protected
3N163	T0-72	-2.0	-5.0	-40	-200	-10.0	2000.0	250	-5	-30
3N164	T0-72	-2.0	-5.0	-30	-400	-10.0	2000.0	300	-3	-30
3N172	T0-72	-2.0	-5.0	-40	-400	-200.0	(2000.0)	250	-5	-30 Diode Protected
3N173	T0-72	-2.0	-5.0	-30	-10nA	-500.0	(1000.0)	350	-5	-30 Diode Protected
IT1700	T0-72	-2.0	-5.0	-40	-200	-10.0	2000.0	400	-2	
N-Channel Enhancement: Can switch positive signals directly from TTL logic; gen. requires driver or translator circuit to switch bipolar signals.										
2N4351	T0-72	1.0	5.0	25	10nA	10.0	1000.0	300	3	
3N170	T0-72	1.0	2.0	25	10nA	10.0	1000.0	200	10	
3N171	T0-72	1.5	3.0	25	10nA	10.0	1000.0	200	10	
IT1750	T0-72	0.5	3.0	25	10nA	10.0	3000.0	50	10	100
M116	T0-72	1.0	5.0	30	(10nA)	100.0	(1000.0)	100	—	Diode Protected

Amplifiers — N-Channel Junction FET

Ordering Information		G_{fs} min μ mho	I_{DSS} min/max mA	V_p min/max V	I_{GSS} max pA	BV_{GSS} min V	C_{iss} max pF	C_{rss} max pF	e_n max nv/ \sqrt Hz		
Preferred Part Number	Package										
2N3684	T0-72	2000	2.5	7.5	-2.0	-5.0	-100	-50	4	1.2	140 @ 100Hz
2N3685	T0-72	1500	1.0	3.0	-1.0	-3.5	-100	-50	4	1.2	140 @ 100Hz
2N3686	T0-72	1000	0.4	1.2	-0.6	-2.0	-100	-50	4	1.2	140 @ 100Hz
2N3687	T0-72	500	0.1	0.5	-0.3	-1.2	-100	-50	4	1.2	140 @ 100Hz
2N3821	T0-72	1500	0.5	2.5	-4.0	-100	-50	-50	6	3.0	200 @ 10Hz
2N3822	T0-72	3000	2.0	10.0	-6.0	-100	-50	-50	6	3.0	200 @ 10Hz
2N3823	T0-72	3500	4.0	20.0	-8.0	-500	-30	-30	6	2.0	—
2N3824	T0-72	—	—	—	(-8.0)	-100	-50	-50	6	3.0	—
2N4117	T0-72	70	0.03	0.09	-0.6	-1.8	-10	-40	3	1.5	—
2N4117A	T0-72	70	0.03	0.09	-0.6	-1.8	-1	-40	3	1.5	—
2N4118	T0-72	80	0.08	0.24	-1.0	-3.0	-10	-40	3	1.5	—
2N4118A	T0-72	80	0.08	0.24	-1.0	-3.0	-1	-40	3	1.5	—
2N4119	T0-72	100	0.2	0.6	-2.0	-6.0	-10	-40	3	1.5	—
2N4119A	T0-72	100	0.2	0.6	-2.0	-6.0	-1	-40	3	1.5	—
2N4220	T0-72	1000	-0.5	0.3	-4.0	-100	-30	-30	6	2.0	—
2N4221	T0-72	2000	2.0	6.0	-6.0	-100	-30	-30	6	2.0	—
2N4222	T0-72	2500	5.0	15.0	-8.0	-100	-30	-30	6	2.0	—
2N4223	T0-72	3000	3.0	18.0	-0.1	-8.0	-250	-30	6	2.0	—
2N4224	T0-72	2000	2.0	20.0	-0.1	-8.0	-500	-30	6	2.0	—
2N4338	T0-18	600	0.2	0.6	-0.3	-1.0	-100	-50	7	3.0	65 @ 1kHz
2N4339	T0-18	800	0.5	1.5	-0.6	-1.8	-100	-50	7	3.0	65 @ 1kHz
2N4340	T0-18	1300	1.2	3.6	-1.0	-3.0	-100	-50	7	3.0	65 @ 1kHz
2N4341	T0-18	2000	3.0	9.0	-2.0	-6.0	-100	-50	7	3.0	65 @ 1kHz
2N4416	T0-72	4500	5.0	15.0	-6.0	-100	-30	-30	4	2.0	—
2N4867	T0-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5.0	10 @ 1kHz
2N4867A	T0-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5.0	5 @ 1kHz
2N4868	T0-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5.0	10 @ 1kHz
2N4868A	T0-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5.0	5 @ 1kHz
2N4869	T0-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5.0	10 @ 1kHz
2N4869A	T0-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5.0	5 @ 1kHz
2N5397	T0-72	6000	10.0	30.0	-1.0	-6.0	-100	-25	5	1.2	3.5dB @ 450MHz
2N5398	T0-72	5500	5.0	40.0	-1.0	-6.0	-100	-25	5.5	1.3	—
2N5457	T0-92	1000	1.0	5.0	-0.1	-6.0	-1nA	-25	7	3.0	—
2N5458	T0-92	1500	2.0	9.0	-1.0	-7.0	-1nA	-25	7	3.0	—
2N5459	T0-92	2000	4.0	16.0	-2.0	-8.0	-1nA	-25	7	3.0	—

Amplifiers — N-Channel Junction FET (continued)

Ordering Information		g _{fs} min μmho	I _{DSS} min/max mA	V _p min/max V	I _{GSS} max μA	BV _{GSS} min V	C _{iss} max pF	C _{rss} max pF	e _n max nV/√Hz		
Preferred Part Number	Package										
2N5484	TO-92	3000	1.0	5.0	-0.3	-3.0	-1nA	-25	5	1.0	120 @ 1kHz
2N5485	TO-92	3500	4.0	10.0	-0.5	-4.0	-1nA	-25	5	1.0	120 @ 1kHz
2N5486	TO-92	4000	8.0	20.0	-2.0	-6.0	-1nA	-25	5	1.0	120 @ 1kHz
ITE4416	TO-92	4500	5.0	15.0	-	-6.0	-100	-30	4	2.0	—
J201	TO-92	500	0.2	1.0	-0.3	-1.5	-100	-40	4	1.0	5 @ 1kHz
J202	TO-92	1000	0.9	4.5	-0.8	-4.0	-100	-40	4	1.0	5 @ 1kHz
J203	TO-92	1500	4.0	20.0	-2.0	-10.0	-100	-40	4	1.0	5 @ 1kHz
J204	TO-92	1500	1.2	typ.	-0.5	-2.0	-100	-25	4	1.0	10 @ 1kHz
J308	TO-92	8000	12.0	60.0	-1.0	-6.5	-1nA	-25	(8)	(5.0)	—
J309	TO-92	10,000	12.0	30.0	-1.0	-4.0	-1nA	-25	(8)	(5.0)	—
J310	TO-92	8000	24.0	60.0	-2.0	-6.5	-1nA	-25	(8)	(5.0)	—
U308	TO-52	10,000	12.0	60.0	-1.0	-6.0	-150	-25	7 typ.	4.0 typ.	10 @ 100Hz typ.
U309	TO-52	10,000	12.0	30.0	-1.0	-4.0	-150	-25	7 typ.	4.0 typ.	10 @ 100Hz typ.
U310	TO-52	10,000	24.0	60.0	-2.5	-6.0	-150	-25	7 typ.	4.0 typ.	10 @ 100Hz typ.

Amplifiers — P-Channel Junction FET

Ordering Information		g _{fs} min μmho	I _{DSS} min/max mA	V _p min/max V	I _{GSS} max nA	BV _{GSS} min V	C _{iss} max pF	C _{rss} max pF	e _n max nV/√Hz		
Preferred Part Number	Package										
2N2607	TO-18	330	-0.3	-1.5	1.0	4.0	3	30	10	—	400 @ 1kHz
2N2608	TO-18	1000	-0.9	-4.5	1.0	4.0	10	30	17	—	140 @ 1kHz
2N2609	TO-18	2500	-2.0	-10.0	1.0	4.0	30	30	30	—	140 @ 1kHz
2N5460	TO-92	1000	-1.0	-5.0	0.75	6.0	5	40	7	2	115 @ 100Hz
2N5461	TO-92	1500	-2.0	-9.0	1.0	7.5	5	40	7	2	115 @ 100Hz
2N5462	TO-92	2000	-4.0	-16.0	1.8	9.0	5	40	7	2	115 @ 100Hz
2N5463	TO-92	1000	-1.0	-5.0	0.75	6.0	5	60	7	2	115 @ 100Hz
2N5464	TO-92	1500	-2.0	-9.0	1.0	7.5	5	60	7	2	115 @ 100Hz
2N5465	TO-92	2000	-4.0	-16.0	1.8	9.0	5	60	7	2	115 @ 100Hz
U304	TO-18	—	-30.0	-90.0	5.0	10.0	.5	30	27	7	—
U305	TO-18	—	-15.0	-60.0	3.0	6.0	.5	30	27	7	—
U306	TO-18	—	-5.0	-25.0	1.0	4.0	.5	30	27	7	—

Differential Amplifiers — Dual Monolithic N-Channel Junction FET

Preferred Part Number	Package	V _{GS1-2} max mV	ΔV _{GS} max μV/°C	I _G max pA	BV _{GS} min V	V _P min/max V	I _S min/max μmho	I _{DSS} min/max mA	g _m max nV/√Hz			
2N3921	TO-71	5	10	-250	-50	-	-3.0	1500	7500	1.0	10.0	-
2N3922	TO-71	5	25	-250	-50	-	-3.0	1500	7500	1.0	10.0	-
2N3954	TO-71	5	10	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3954A	TO-71	5	5	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3955	TO-71	10	25	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3955A	TO-71	15	15	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3956	TO-71	15	50	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3957	TO-71	20	75	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N3958	TO-71	25	100	-50	-50	-1.0	-4.5	1000	3000	0.5	5.0	160 @ 100Hz
2N5196	TO-71	5	5	-15	-50	-0.7	-4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5197	TO-71	5	10	-15	-50	-0.7	-4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5198	TO-71	10	20	-15	-50	-0.7	-4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5199	TO-71	15	40	-15	-50	-0.7	-4.0	700 @ 200μA		0.7	7.0	20 @ 1kHz
2N5452	TO-71	5	5	IGSS-100	-50	-1.0	-4.5	1000	4000	0.5	5.0	20 @ 1kHz
2N5453	TO-71	10	10	IGSS-100	-50	-1.0	-4.5	1000	4000	0.5	5.0	20 @ 1kHz
2N5454	TO-71	15	25	IGSS-100	-50	-1.0	-4.5	1000	4000	0.5	5.0	20 @ 1kHz
2N5515	TO-71	5	5	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5516	TO-71	5	10	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5517	TO-71	10	20	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5518	TO-71	15	40	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5519	TO-71	15	80	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	30 @ 10Hz
2N5520	TO-71	5	5	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5521	TO-71	5	10	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5522	TO-71	10	20	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5523	TO-71	15	40	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5524	TO-71	15	80	-100	-40	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10Hz
2N5902	TO-99	5	5	-3	-40	-0.6	-4.5	70	250	0.3	0.5	200 @ 1kHz
2N5903	TO-99	5	10	-3	-40	-0.6	-4.5	70	250	0.03	.05	200 @ 1kHz
2N5904	TO-99	10	20	-3	-40	-0.6	-4.5	70	250	0.03	.05	200 @ 1kHz
2N5905	TO-99	15	40	-3	-40	-0.6	-4.5	70	250	0.03	.05	200 @ 1kHz
2N5906	TO-99	5	5	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1kHz
2N5907	TO-99	5	10	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1kHz
2N5908	TO-99	10	20	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1kHz
2N5909	TO-99	15	40	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1kHz
2N5911	TO-99	10	20	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
2N5912	TO-99	15	40	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
2N6483	TO-71	5	5	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	10 @ 10Hz
2N6484	TO-71	10	10	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	10 @ 10Hz
2N6485	TO-71	15	25	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	10 @ 10Hz
IMF6485	TO-71	25	40	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10Hz
IT500	TO-52	5	5	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10Hz
IT501	TO-52	5	10	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10Hz
IT502	TO-52	10	20	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10Hz
IT503	TO-52	15	40	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10Hz
IT504	TO-52	25	100	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10Hz
IT505	TO-52	50	200	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10Hz
IT5911	TO-71	10	20	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
IT5912	TO-71	15	40	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10kHz
U257	TO-99	100	-	IGSS-100	-25	-1.0	-5.0	5000	10000	5.0	40.0	30 @ 10kHz
U401	TO-71	5	10	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10Hz
U402	TO-71	10	10	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10Hz
U403	TO-71	10	25	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10Hz
U404	TO-71	15	25	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10Hz
U405	TO-71	20	40	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10Hz
U406	TO-71	40	80	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10Hz
U421	TO-99	10	10	0.1	-60	-0.4	-2.0	300	800	60-1000μA		20 @ 10Hz
U422	TO-99	15	25	0.1	-60	-0.4	-2.0	300	800	60-1000μA		20 @ 10Hz
U423	TO-99	25	40	0.1	-60	-0.4	-2.0	300	800	60-1000μA		20 @ 10Hz
U424	TO-99	10	10	0.5	-60	-0.4	-3.0	300	1000	60-1000μA		20 @ 10Hz
U425	TO-99	15	25	0.5	-60	-0.4	-3.0	300	1000	60-1000μA		20 @ 10Hz
U426	TO-99	25	40	0.5	-60	-0.4	-3.0	300	1000	60-1000μA		20 @ 10Hz

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Differential Amplifiers — Dual Monolithic P-Channel MOSFETS (Enhancement)

Ordering Information											
Preferred Part Number	Package	$V_{GS(TH)}$ min/max V		BV_{OSS} min/max V	I_{DSS} max pA	I_{GSS} max pA	G_{fs} min μ mho	$I_{DS(ON)}$ min/max mA		$r_{DS(ON)}$ max Ω	V_{OS} 1-2 max mV
3N165	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	100
3N166	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	
3N188	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	100 Zener Protected
3N189	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	Zener Protected
3N190	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	100 Zener Protected
3N191	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	

Differential Amplifiers — Dual NPN Bipolar Transistors

Ordering Information											
Preferred Part Number	Package	V_{BE} 1-2 mV max	ΔV_{BE} μ V/ $^{\circ}$ C max	$h_{FE} \oplus$		BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz@ I_C min	C_{ob0} pF max	Structure
				$I_C = 10 \mu$ A $V_{CE} = 5V$ min	$I_C = 10 \mu$ A $V_{CE} = 5V$ max						
2N4044	TO-78	3	3	200	5	60	.1	2	200 @ 1mA	0.8	Dielec. Isol.
2N4045	TO-78	5	10	80	25	45	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4100	TO-78	5	5	150	10	55	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4878	TO-71	3	3	200	5	60	.1	2	200 @ 1mA	0.8	Dielec. Isol.
2N4879	TO-71	5	5	150	10	55	.1	3	150 @ 1mA	0.8	Dielec. Isol.
2N4880	TO-71	5	10	80	25	45	.1	3	150 @ 1mA	0.8	Dielec. Isol.
IT120	TO-78 TO-71	2	5	200	5	45	1	2 typ.	220 @ 1mA	2	Junc. Isol.
IT120A	TO-78 TO-71	1	3	200	2.5	45	1	2 typ.	220 @ 1mA	2	Junc. Isol.
IT121	TO-78 TO-71	3	10	80	25	45	1	2 typ.	180 @ 1mA	2	Junc. Isol.
IT122	TO-78 TO-71	5	20	80	25	45	1	2 typ.	180 @ 1mA	2	Junc. Isol.
IT124	TO-78	5	15	1500	0.6 @ $V_{CE} = 1V$	2	.1	3	100 @ 100 μ A	0.8	Junc. Isol.
IT126	TO-78 TO-71	1	3	200	2.5	60	.1	1 typ.	250 @ 10mA	4	Dielec. Isol.
IT127	TO-78 TO-71	2	5	200	5	60	.1	1 typ.	250 @ 10mA	4	Dielec. Isol.
IT128	TO-78 TO-71	3	10	150	10	45	.1	1 typ.	200 @ 10mA	4	Dielec. Isol.
IT129	TO-78 TO-71	5	20	100	20	45	.1	1 typ.	150 @ 10mA	4	Dielec. Isol.

Differential Amplifiers — Dual PNP Bipolar Transistors

Ordering Information		V_{BE} 1-2 mV max	ΔV_{BE} $\mu V/^{\circ}C$ max	h_{FE} @	$I_C = 10\mu A$	$I_C = 5V$	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz @ I_C min	C_{obo} pF max	Structure
Preferred Part Number	Package			$I_C = 10\mu A$ min	$V_{CE} = 5V$ max	$V_{CE} = 5V$ nA max						
2N5117	TO-78	3	3	100	10	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.	
2N5118	TO-78	5	5	100	15	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.	
2N5119	TO-78	5	10	50	40	45	.1	4	100 @ 0.5mA	.8	Dielec. Isol.	
IT130	TO-78 TO-71	2	5	200	5	-45	1	2 typ.	110 @ 1mA	2	Junc. Isol.	
IT130A	TO-78 TO-71	1	3	200	2.5	-60	1	2 typ.	110 @ 1mA	2	Junc. Isol.	
IT131	TO-78 TO-71	5	10	80	10	-45	1	2 typ.	90 @ 1mA	2	Junc. Isol.	
IT132	TO-78 TO-71	10	20	80	25	-45	1	2 typ.	90 @ 1mA	2	Junc. Isol.	
IT136	TO-78 TO-71	1	3	150	2.5	-60	.1	2 typ.	150 @ 10mA	4	Dielec. Isol.	
IT137	TO-78 TO-71	2	5	150	5	-60	.1	2 typ.	150 @ 10mA	4	Dielec. Isol.	
IT138	TO-78 TO-71	3	10	120	10	-55	.1	2 typ.	180 @ 10mA	4	Dielec. Isol.	
IT139	TO-78 TO-71	5	20	70	20	-45	.1	2 typ.	100 @ 10mA	4	Dielec. Isol.	

Specialty Items

ID-100 This product is a diode combination used to protect those P-channel MOSFET duals which are not diode protected. Their chief characteristic is < 1 pA leakage when voltage across them is less than 5 mV. If voltage across diodes is adjusted to $0V \pm 0.1mV$, leakage is less than 0.01 pA.

VCR2N

VCR3P

VCR4N

VCR5P

VCR7N

VCR11N (Dual)

The VCR family consists of three terminal variable resistors where the resistance value between two of the terminals is controlled by the voltage potential applied to the third.

Note: Intersil offers the following military qualified devices:*

N-channel switches	N-channel amplifiers	P-channel switches	P-channel amplifiers
2N4091 JAN, JANTX, JANTXV	2N3821 JAN, JANTX, JANTXV	2N5114 JAN, JANTX, JANTXV	2N2609 JAN
2N4092 JAN, JANTX, JANTXV	2N3823 JAN, JANTX, JANTXV	2N5115 JAN, JANTX, JANTXV	
2N4093 JAN, JANTX, JANTXV		2N5116 JAN, JANTX, JANTXV	
2N4856 JAN, JANTX, JANTXV			
2N4857 JAN, JANTX, JANTXV			
2N4858 JAN, JANTX, JANTXV			

*JAN processing consists of a sample Group B pulled from the production run.

JANTX processing consists of JAN processing plus 100% electrical read and record, and 100% burn-in.

JANTXV processing consists of JANTX processing plus 100% pre-cap visual and on-shore assembly.

DISCRETE SELECTOR GUIDE

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	Detailed Application	Important Parameters	Recommended Part Numbers							
			Single N-Channel JFET	Single P-Channel JFET	Dual N-Channel JFET	Single N-Channel MOSFET	Single P-Channel MOSFET	Dual P-Channel MOSFET	Dual NPN Bipolar	Dual PNP Bipolar
Amplifiers	Audio	low noise	2N4220, 2N3821	2N2607, 2N5460	2N3958 1T505	2N4351 3N170-1	3N163 3N164	3N165	2N4044 2N4878	1T130
	Buffer	low leakage, high gain	2N4221	2N2609 2N5462	2N5905 1T505	M116 1T1750	3N172 1T1700		1T120	1T136
	Differential	good matching & drift	—	—	2N3954 U401 2N5515	—	—		1T126	2N3810
	Fet Input Op Amp		—	—	—	—	—	—	—	—
	High Impedance	low leakage	2N4117A	1T100 J176 2N5116	2N5905 1T505 U426	1T1750	1T1700	—	—	—
	High Frequency	high gain, low capacitance	U308	2N5114	2N5912	2N4351	3N163	3N188	2N4044 2N4878	1T130
	Low Supply Voltage	low pinch-off voltage	2N5397	J176	1T5912	—	3N164		1T120	1T136
	Low Noise	low noise	2N4338 2N3687	2N5266 J177	U406 2N3958	3N170-1	—	1T126 1T140	2N3810	—
	Preamplifier	high gain	2N4867A	2N5116 J176	2N5519 2N5199	M116	3N172	—	2N4044 2N4878	1T130 1T136
	Video	high gain, low capacitance	2N5397 U310	2N5116 J176	1T550 U406	—	—	—	1T120 1T126	2N3810
Mixers	VHF	RF parameters,	U310 2N5397	1T100 J174	2N6485	—	—	—	—	—
	UHF	high g_{fs}/C_{iss}	J310 2N5484	2N5114	1T5912 2N5912	—	—	—	—	—
Switches	Commutators	low C_{rss}	2N4391 1TE4391	2N3993-4 1T100-1 2N5114-6	1T550	1T1750	1T1700	—	—	—
	Sample and Hold		—	—	—	—	3N163	3N165	—	—
	Analog Gates	fast switching,	2N4091-3 2N4391-3	2N5114-6	2N5912	—	—	—	—	—
	Digital	low $r_{DS(on)}$	1TE4391-3	J174-7	1T5912	3N170-1	3N164	3N188	—	—
	Chopper		2N5432-4	1T100-1	—	—	3N172		—	—
Integrator Reset	low $r_{DS(on)}$, high I_{DSS}	J111-3 J105-7	—	—	—	—	—	—	—	
Voltage Control Resistors	Gain Control Amplitude Stability Attenuators	high $V_{GS(off)}$	VCR2N VCR4N VCR7N	VCR3P	VCR11N	—	—	—	—	—
Protection Diodes	Signal Clipping and Clamping	low leakage current	—	—	—	—	—	ID100-1	1T139	

2N2607-2N2609 2N2609 JAN P-Channel JFET

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APPLICATIONS


- Low-level Choppers
- Data Switches
- Commutators

ABSOLUTE MAXIMUM RATINGS

 (T_A = 25°C unless otherwise noted)

Gate-Source Voltage	30 V
Gate-Drain Voltage	30 V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2 mW/°C

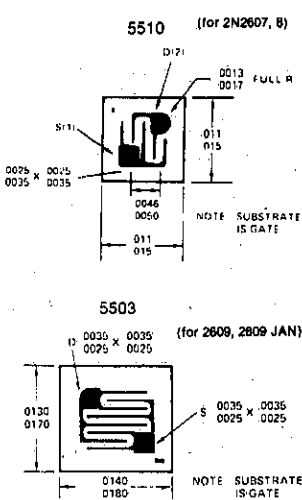
PIN CONFIGURATION



TO-18

D G.C S

CHIP TOPOGRAPHY



5510 (for 2N2607, B)

5503 (for 2609, 2809 JAN)

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N2607	2N2607/W	2N2607/D
2N2608	2N2608/W	2N2608/D
2N2609	2N2609/W	2N2609/D
2N2609 JAN	—	—

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER	2N2607		2N2608		2N2609		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
I _{GSSR} Gate Reverse Current		3		10		30	nA	V _{GS} = 30 V, V _{DS} = 0
		3		10		30	μA	V _{GS} = 5 V, V _{DS} = 0, T _A = 150°C
BV _{GSS} Gate-Drain Breakdown Voltage	30		30		30		V	I _G = 1 μA, V _{DS} = 0
V _P Gate-Source Pinch-Off Voltage	1	4	1	4	1	4	V	V _{DS} = -5 V, I _D = -1 μA
I _{DSS} Drain Current at Zero Gate Voltage	-0.30	-1.50	-0.90	-4.50	-2	-10	mA	V _{DS} = -5 V, V _{GS} = 0
g _{fs} Small-Signal Common-Source Forward Transconductance	330		1000		2500		μmho	V _{DS} = -5 V, V _{GS} = 0, f = 1 kHz
C _{iss} Common-Source Input Capacitance		10		17		30	pF	V _{DS} = -5 V, V _{GS} = 1 V, f = 140 kHz
NF Noise Figure		3					dB	V _{DS} = -5 V, V _{GS} = 0, f = 1 kHz, R _G = 10 MΩ
				3		3		R _G = 1 MΩ

FEATURES

- Low Noise
- High Input Impedance
- Low Capacitance

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APPLICATIONS

- Low Level Choppers
- Data Switches
- Multiplexers
- Low Noise Amplifiers

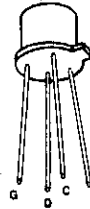
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	50 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

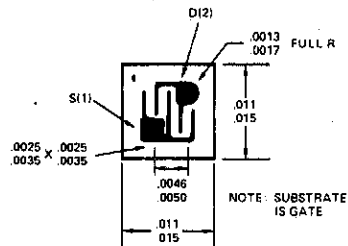
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5010°



*DICE WITH 4 MIL BONDING PADS, AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

	TO-72	WAFER	DICE
2N3684	2N3684/W	2N3684/D	
2N3685	2N3685/W	2N3685/D	
2N3686	2N3686/W	2N3686/D	
2N3687	2N3687/W	2N3687/D	

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3684		2N3685		2N3686		2N3687		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	-50		-50		-50		-50		V	$V_{DS} = 0, I_G = 1.0 \mu\text{A}$
V_p	Pinch-Off Voltage	2.0	5.0	1.0	3.5	0.6	2.0	0.3	1.2		$V_{DS} = 20 \text{ V}, I_D = 0.001 \mu\text{A}$
I_{GSS}	Total Gate Leakage Current		-0.1		-0.1		-0.1		-0.1	nA	$V_{GS} = -30 \text{ V}, V_{DS} = 0$
		$T_A = 150^\circ\text{C}$		-0.5		-0.5		-0.5		-0.5	μA
I_{DSS}	Saturation Current, Drain-to-Source	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA	$V_{GS} = 0, V_{DS} = 20 \text{ V}$
$ Y_{fs} $	Forward Transadmittance	2000	3000	1500	2500	1000	2000	500	1500	μmhos	$V_{DS} = 20 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ kHz}$
G_{os}	Common Source Output Conductance		50		25		10		5	μmhos	
C_{iss}	Common Source Input Capacitance		4.0		4.0		4.0		4.0	pF	
C_{rss}	Common Source Short Circuit Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF	
$r_{DS(on)}$	On Resistance		600		800		1200		2400	Ohms	$V_{DS} = 0, V_{GS} = 0$
NF	Noise Figure		0.5		0.5		0.5		0.5	dB	$f = 100 \text{ Hz}, R_G = 10 \text{ M}\Omega$ $NBW = 6 \text{ Hz}, V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}$



2N3810/A, 2N3811/A Monolithic Dual Matched PNP Transistor

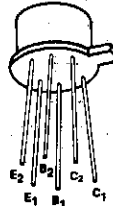
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ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

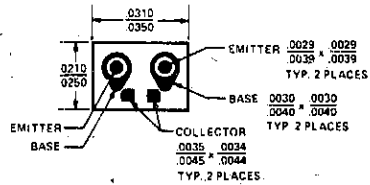
Emitter-Base Voltage (Note 1)	-5V	
Collector-Base or Collector-Emitter Voltage (Note 1)	-60V	
Collector Current (Note 1)	50 mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	+300°C	
Power Dissipation	ONE SIDE	BOTH SIDES
Derate above 25°C	500 mW	600 mW
	2.9 mW/°C	3.4 mW/°C

PIN CONFIGURATION
TO-78



4501

CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-78	WAFER	DICE
2N3810	2N3810/W	2N3810/D
2N3810A		
2N3811	2N3811/W	2N3811/D
2N3811A		

ELECTRICAL CHARACTERISTICS

*When ordering wafer/dice refer to Appendix B-23.

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	PARAMETER	2N3810/A		2N3811/A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
BV_{CBO}	Collector-Base Breakdown Voltage	-60		-60		V	$I_C = -10 \mu\text{A}, I_E = 0$
BV_{CEO}	Collector-Emitter Breakdown Voltage (Note 2)	-60		-60			
BV_{EBO}	Emitter-Base Breakdown Voltage	-5		-5		nA	$I_C = -10 \text{ mA}, I_B = 0$ $I_E = -10 \mu\text{A}, I_C = 0$
$I_{C(off)}$	Collector Cutoff Current		-10		-10		
			-10		-10	μA	$V_{CB} = -50\text{V}, I_E = 0$
$I_{E(off)}$	Emitter Cutoff Current		-20		-20		
h_{FE}	Static Forward Current Transfer Ratio (Note 2)	100		225		V	$V_{CE} = -5\text{V}$ $I_C = -10 \mu\text{A}$ $I_C = -100 \mu\text{A}$ to -1 mA $I_C = 10 \text{ mA}$ $I_C = 100 \mu\text{A}$
		150	450	300	900		
		125		250			
		75		150			
			-0.7		-0.7	V	$V_{CE} = -5\text{V}, I_B = -10 \mu\text{A}$ $I_C = -100 \mu\text{A}, I_B = -100 \mu\text{A}$ $I_B = -10 \mu\text{A}, I_C = -100 \mu\text{A}$ $I_B = -100 \mu\text{A}, I_C = -1 \text{ mA}$
$V_{BE(sat)}$	Base-Emitter Saturation Voltage (Note 2)		-0.8		-0.8		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 2)		-0.2		-0.2		
			-0.25		-0.25		
h_{ie}	Input Impedance	3	30	10	40	kΩ	$V_{CE} = -10\text{V}$ $I_C = -1 \text{ mA}$ $f = 1 \text{ KHz}$
h_{fe}	Forward Current Transfer Ratio	150	600	300	900		
h_{re}	Reverse Voltage Transfer Ratio		0.25		0.25		
h_{oe}	Output Admittance	5	60	5	60		
$ h_{re} $	Magnitude of small signal current gain	1	5	1	5	μmho	$V_{CE} = -5\text{V}$ $I_C = -1 \text{ mA}, f = 100 \text{ MHz}$ $I_C = -500 \mu\text{A}, f = 30 \text{ MHz}$
		1		1			

NOTES:

- Per transistor.
- Pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

2N3810/A, 2N3811/A



ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature, unless otherwise noted

1

SYMBOL	PARAMETER	2N3810/A		2N3811/A		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
C_{obo}	Output Capacitance		4		4		$V_{CB} = -5V, I_E = 0, f = 100 \text{ MHz}$	
C_{ibo}	Input Capacitance		8		8	pF	$V_{GB} = -0.5V, I_C = 0, f = 100 \text{ KHz}$	
h_{FE1} / h_{FE2}	DC Current Gain Ratio	0.9	1.0	0.9	1.0		$V_{CE} = -5V, I_C = 100 \mu A$	
$ V_{BE1} - V_{BE2} $	Base-Emitter Voltage Differential	A devices	0.95	1.0	0.95	1.0	mV	$V_{CE} = -5V$ $I_C = 10 \mu A \text{ to } 10 \text{ mA}$ $I_C = 100 \mu A$
				-5		-5		
				-2.5		-2.5		
		A devices		-3		-3		
		A devices		-1.5		-1.5		
$\Delta V_{BE1} - V_{BE2}$	Base-Emitter Voltage Differential		10		10	$\mu V / ^\circ C$	$V_{CE} = -5, I_C = 100 \mu A$	
ΔT	Differential Gradient							
		A devices	5		5			
				7		4		
NF	Spot Noise Figure			3		1.5	$V_{CE} = -10V, I_C = -100 \mu A, R_G = 3k\Omega, f = 100 \text{ Hz}, \text{ Noise Bandwidth} = 20\text{Hz}$	
							$V_{CE} = -10V, I_C = -100 \mu A, R_G = 3k\Omega, f = 1\text{kHz}, \text{ Noise Bandwidth} = 200 \text{ kHz}$	
				2.5		1.5	$V_{CE} = -10V, I_C = -100 \mu A, R_G = 3k\Omega, f = 10 \text{ kHz}, \text{ Noise Bandwidth} = 2 \text{ kHz}$	
				3.5		2.5	$V_{CE} = -10V, I_C = -100 \mu A, R_G = 3k\Omega, \text{ Noise Bandwidth} = 15.7 \text{ kHz (Note 3)}$	

NOTES:

3 3 dB down at 10 Hz and 10 kHz.

FEATURES

- Low Capacitance
- Up to 6500 μmho Transconductance

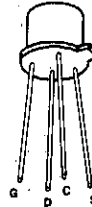
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source Voltage	-50V
Gate-Drain Voltage	-50V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

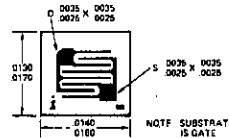
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5003



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3821		2N3822		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Current		-0.1	-0.1	-0.1	nA	$V_{GS} = -30\text{ V}, V_{DS} = 0$
			-0.1	-0.1	-0.1	μA	
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50			$I_G = -1\ \mu\text{A}, V_{DS} = 0$ $V_{DS} = 15\text{ V}, I_D = 0.5\ \text{nA}$ $V_{DS} = 15\text{ V}, I_D = 50\ \mu\text{A}$ $V_{DS} = 15\text{ V}, I_D = 200\ \mu\text{A}$ $V_{DS} = 15\text{ V}, V_{GS} = 0$
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6	V	
V_{GS}	Gate-Source Voltage	-0.5	-2				
I_{DSS}	Saturation Drain Current	0.5	2.5	2	10	mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	4500	3000	6500	μmho	$f = 1\ \text{kHz}$
$ y_{fs} $	Common-Source Forward Transadmittance	1500		3000			$f = 100\ \text{MHz}$
g_{os}	Common-Source Output Conductance (Note 1)		10		20	pF	$V_{DS} = 15\text{ V}, V_{GS} = 0$ $f = 1\ \text{kHz}$
C_{iss}	Common-Source Input Capacitance		6		6		$f = 1\ \text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		
NF	Noise Figure		5		5	dB	$V_{DS} = 15\text{ V}, V_{GS} = 0,$ $R_{gen} = 1\ \text{meg}, BW = 5\ \text{Hz}$ $f = 10\ \text{Hz}$
\bar{e}_n	Equivalent Input Noise Voltage		200		200	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$V_{DS} = 15\text{ V}, V_{GS} = 0, BW = 5\ \text{Hz}$

Note 1: These parameters are measured during a 2 msec interval 100 msec after DC power is applied.

1

FEATURES

- Low Noise
- Low Capacitance
- Transconductance up to 6500 μmho

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION

CHIP TOPOGRAPHY

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3823	2N3823/W	2N3823/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.5	nA	$V_{GS} = -20V, V_{DS} = 0$	
			-0.5	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-30			$I_G = 1 \mu\text{A}, V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-8	V		
V_{GS}	Gate-Source Voltage	-1.0	-7.5		$V_{DS} = 15V, I_D = 0.5 \text{ nA}$	
I_{DSS}	Saturation Drain Current	4	20	mA		
g_{fs}	Common-Source Forward Transconductance	3,500	6,500	μmho	$V_{DS} = 15V, V_{GS} = 0$	$f = 1 \text{ kHz}$ (Note 1)
$ Y_{fs} $	Common-Source Forward Transadmittance	3,200				$f = 100 \text{ MHz}$
g_{os}	Common-Source Output Transconductance		35			$f = 1 \text{ kHz}$ (Note 1)
g_{iss}	Common-Source Input Conductance		800			$f = 200 \text{ MHz}$
g_{oss}	Common-Source Output Conductance		200			$f = 1 \text{ MHz}$
C_{iss}	Common-Source Input Capacitance		6	pF	$V_{DS} = 15V, V_{GS} = 0$	$R_G = 1 \text{ k}\Omega$
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Noise Figure		2.5	dB		$f = 100 \text{ MHz}$

NOTE 1: These parameters are measured during a 2 msec interval 100 msec after DC power is applied.

FEATURES

- $r_{ds} < 250$ ohms
- $I_{D(off)} < 0.1$ nA


ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	10 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Load Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

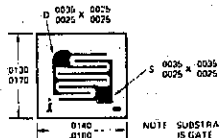
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5003



NOTE: SUBSTRATE IS GATE.

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3824	2N3824/W	2N3824/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS
I _{GSS}	Gate Reverse Current		-0.1	nA	V _{GS} = -30V, V _{DS} = 0
		T _A = 150°C	-0.1	μA	
BV _{GSS}	Gate-Source Breakdown Voltage	-50		V	I _G = 1 μA, V _{DS} = 0
I _{D(off)}	Drain Cutoff Current		0.1	nA	V _{DS} = 15V, V _{GS} = -8V
		T _A = 150°C	0.1	μA	
r _{ds(on)}	Drain-Source ON Resistance		250	Ω	V _{GS} = 0V, I _D = 0 f = 1 kHz
C _{iss}	Common-Source Input Capacitance		6	pF	V _{DS} = 15V, V _{GS} = 0
C _{rss}	Common-Source Reverse Transfer Capacitance		3		V _{GS} = -8V, V _{DS} = 0



2N3921, 2N3922 Monolithic Dual N-Channel JFET

1

FEATURES

- Low Drain Current
- High Output Impedance
- Matched V_{GS} , ΔV_{GS} , and g_{fs}

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate Current (Note 1)	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Load Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION
TO-71

CHIP TOPOGRAPHY
6037

ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N3921	2N3921/W	2N3921/D
2N3922	2N3922/W	2N3922/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: (25°C unless otherwise noted)

*When ordering wafer/dice refer to Appendix B-23.

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSSR}	Gate Reverse Current		-1	nA	$V_{GS} = -30V, V_{DS} = 0$ $I_D = 1 \mu A, I_S = 0$	
BV_{DGO}	Drain-Gate Breakdown Voltage	50	-1	μA		
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3	V	$V_{DS} = 10V, I_D = 1 nA$ $V_{DS} = 10V, I_D = 100 \mu A$	
V_{GS}	Gate-Source Voltage	-0.2	-2.7			
I_G	Gate Operating Current		-250	pA	$V_{DG} = 10V, I_D = 700 \mu A$ $V_{DS} = 10V, V_{GS} = 0$	
I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA		
g_{fs}	Common-Source Forward Transconductance (Note 2)	1500	7500	μmho	$V_{DS} = 10V, V_{GS} = 0$ $f = 1 kHz$	
g_{os}	Common-Source Output Conductance		35			
C_{iss}	Common-Source Input Capacitance		18	pF	$V_{DG} = 10V, I_D = 700 \mu A$ $f = 1 kHz$	
C_{rss}	Common-Source Reverse Transfer Capacitance		6			
g_{fs}	Common-Source Forward Transconductance	1500		μmho	$V_{DS} = 10V, V_{GS} = 0$ $f = 1 kHz, R_G = 1 meg$	
g_{oss}	Common-Source Output Conductance		20			
NF	Spot Noise Figure		2	dB		

MATCHING CHARACTERISTICS		2N3921		2N3922		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		5		5	mV	$V_{DG} = 10V, I_D = 700 \mu A$ $T_A = 0^\circ C$ $T_B = 100^\circ C$ $f = 1 kHz$	
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		10		25	$\mu V/^\circ C$		
g_{fs2}	Transconductance Ratio	0.95	1.0	0.95	1.0			

NOTES: 1. Per transistor.

2. Pulse test duration = 2 ms.

2N3954-2N3958 Monolithic Dual N-Channel JFET

1

FEATURES

- Low Offset and Drift
- Low Capacitance
- Low Noise
- Superior Tracking Ability
- Low Output Conductance

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Source or Gate-Drain
 Breakdown Voltage (Note 1) 50V
 Any Pin to Case Voltage 100V
 Gate Current (Note 1) 50 mA
 Storage Temperature .. -65°C to +200°C
 Operating Temperature .. -55°C to +150°C
 Lead Temperature
 (Soldering, 10 sec.) +300°C

ONE **BOTH**
SIDE **SIDES**

Power Dissipation 250 mW 500 mW
 Derate above 25°C 2.8 mW/°C 4.3 mW/°C

PIN CONFIGURATION

TO-71

CHIP TOPOGRAPHY

6037 .023 G₂

S₁ D₂ .017

D₁ G₁ S₂

ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I _{GSS}	Gate Reverse Current		-100		-100		-100		-100		-100		-100		pA	V _{GS} = -30 V, V _{DS} = 0
	T _A = 125°C		-500		-500		-500		-500		-500		-500			
BV _{GSS}	Gate-Source Breakdown Voltage		-50		-50		-50		-50		-50		-50		V	V _{DS} = 0 I _G = -1 μA
V _{GS(off)}	Gate-Source Cutoff Voltage		-1.0		-4.5		-1.0		-4.5		-1.0		-4.5			
V _{GS(f)}	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		2.0		2.0			
V _{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2		nA	V _{DS} = 20 V, I _D = 1 nA
	T _A = 125°C		-0.5		-4.0		-0.5		-4.0		-0.5		-4.0			
I _G	Gate Operating Current		-50		-50		-50		-50		-50		-50		nA	V _{DS} = 20 V, I _D = 200 μA
	T _A = 125°C		-250		-250		-250		-250		-250		-250			
I _{DSS}	Saturation Drain Current		0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V _{DS} = 20 V, V _{GS} = 0
g _{fs}	Common-Source Forward Transconductance		1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000		
	g _{os}	Common-Source Output Conductance		35		35		35		35		35		35		pF
C _{iss}		Common-Source Input Capacitance		4.0		4.0		4.0		4.0		4.0		4.0		
C _{rss}	Common Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2		1.2		1.2		pF	V _{DS} = 20 V, V _{GS} = 0
C _{dgc}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		1.5		1.5			pF
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5		0.5		0.5		0.5		dB	
I _{G1} -I _{G2}	Differential Gate Current		10		10		10		10		10		10			nA
I _{DSS1} /I _{DSS2}	Drain Saturation Current Ratio		0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	mV	
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0		15		25			mV
ΔV _{GS1} -V _{GS2} /ΔT	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		4.0		8.0		T = 25°C to -55°C T = 25°C to 125°C	
g _{fs1} /g _{fs2}	Transconductance Ratio		0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	mV	f = 1 kHz

NOTE 1: Per transistor.

FEATURES

- Low $r_{DS(on)}$
- $I_{D(off)} < 250 \text{ pA}$
- Fast Switching

ABSOLUTE MAXIMUM RATINGS

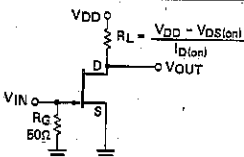
($T_A = 25^\circ \text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to $+200^\circ \text{C}$
Operating Temperature Range	-55°C to $+150^\circ \text{C}$
Lead Temperature (Soldering, 10. sec.)	$+300^\circ \text{C}$
Power Dissipation	1.8W
Derate above 25°C .	10 mW/ $^\circ \text{C}$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETER	2N3970		2N3971		2N3972		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS} Gate Reverse Breakdown Voltage	-40		-40		-40		V	$I_G = -1\mu\text{A}$, $V_{DS} = 0$	
I_{DGO} Drain Reverse Current		250		250		250	pA	$V_{DG} = 20\text{V}$, $I_S = 0$	
$I_{D(off)}$ Drain Cutoff Current		500		500		500	nA	$V_{DG} = 20\text{V}$, $V_{GS} = -12\text{V}$	
	$T_A = 150^\circ \text{C}$	500		500		500	nA		
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20\text{V}$, $I_D = 1 \text{ nA}$	
I_{DSS} Saturation Drain Current (Pulse width $300\mu\text{s}$, duty cycle $\leq 3\%$)		50	150	25	75	5	30	mA	$V_{DS} = 20\text{V}$, $V_{GS} = 0$
	$V_{DS(on)}$ Drain-Source ON Voltage				1.5			V	$V_{GS} = 0$ $I_D = 5 \text{ mA}$ $I_D = 10 \text{ mA}$ $I_D = 20 \text{ mA}$
$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1 \text{ mA}$	
$r_{DS(on)}$ Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$	
C_{iss} Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20\text{V}$, $V_{GS} = 0$ $f = 1 \text{ kHz}$	
C_{rss} Common-Source Reverse Transfer Capacitance		6		6		6	pF	$V_{DS} = 0$, $V_{GS} = -12\text{V}$ $f = 1 \text{ MHz}$	
t_d Turn-On Delay Time		10		15		40	ns	$V_{DD} = 10\text{V}$, $V_{GS(on)} = 0$ $I_{D(on)}$ $V_{GS(off)}$ R_L	
t_r Rise Time		10		15		40	ns	2N3970 20 mA -10V 450 Ω	
t_{off} Turn-Off Time		30		60		100	ns	2N3971 10 mA -5V 850 Ω	
								2N3972 5 mA -3V 1.6K Ω	



INPUT PULSE
 RISE TIME 0.25 ns
 FALL TIME 0.75 ns
 PULSE WIDTH 200 ns
 PULSE RATE 550 pps

SAMPLING SCOPE
 RISE TIME 0.4 ns
 INPUT RESISTANCE 10 M
 INPUT CAPACITANCE 1.5 pF

PIN CONFIGURATION

TO-18

CHIP TOPOGRAPHY

5001

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N3970	2N3970/W	2N3970/D
2N3971	2N3971/W	2N3971/D
2N3972	2N3972/W	2N3972/D

*When ordering wafer/dice refer to Appendix B-23.

FEATURES

- Low $r_{DS(on)}$
- High Y_{fs}/C_{iss} Ratio (High-Frequency Figure-of-Merit)

APPLICATIONS


Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ± 10 VAC. Can be driven direct from T²L or CMOS logic.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

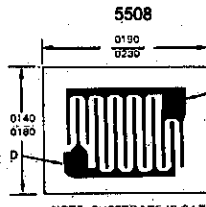
PIN CONFIGURATION



TO-72

D G C S

CHIP TOPOGRAPHY



5508

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N3993	2N3993/W	2N3993/D
2N3994	2N3994/W	2N3994/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

SYMBOL	PARAMETER	2N3993		2N3994		UNIT	TEST CONDITIONS (Note 3)
		MIN	MAX	MIN	MAX		
BV _{GSS}	Gate-Source Breakdown Voltage	25		25		V	$I_G = 1 \mu\text{A}$, $V_{DS} = 0$
I _{DGO}	Drain Reverse Current		-1.2		-1.2	nA	$V_{DG} = -15 \text{ V}$, $I_S = 0$
I _{DSS}	Zero-Gate-Voltage Drain Current	-10		-2		mA	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, (See Note 1)
I _{D(off)}	Drain Cutoff Current				-1.2	nA	$V_{DS} = -10 \text{ V}$, $V_{GS} = 6 \text{ V}$
					-1	μA	$V_{DS} = -10 \text{ V}$, $V_{GS} = 6 \text{ V}$, $T_A = 150^\circ\text{C}$
			-1.2			nA	$V_{DS} = -10 \text{ V}$, $V_{GS} = 10 \text{ V}$
			-1			μA	$V_{DS} = -10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $T_A = 150^\circ\text{C}$
V _{GS(off)}	Gate-Source Voltage	4	9.5	1	5.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \mu\text{A}$
r _{ds(on)}	Small-Signal Drain-Source On-State Resistance		150		300	Ω	$V_{GS} = 0$, $I_D = 0$, $f = 1 \text{ kHz}$
y _{fs}	Small-Signal Common-Source Forward Transfer Admittance	6	12	4	10	mmho	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ kHz}$, (See Note 1)
C _{iss}	Common-Source Short-Circuit Input Capacitance		16		16	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$, (See Note 2)
C _{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance				5	pF	$V_{DS} = 0$, $V_{GS} = 6 \text{ V}$, $f = 1 \text{ MHz}$
			4.5			pF	$V_{DS} = 0$, $V_{GS} = 10 \text{ V}$, $f = 1 \text{ MHz}$

NOTES: 1. These parameters must be measured using pulse techniques. $t_p = 100 \text{ ms}$, duty cycle $\leq 10\%$.

2. This parameter must be measured with bias voltage applied for less than 5 seconds to avoid overheating.

3. The case should be connected to the source for all measurements.



2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor

1

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

ABSOLUTE MAXIMUM RATINGS

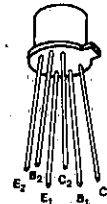
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)	
2N4044, 2N4878	60V
2N4100, 2N4879	55V
2N4045, 2N4880	45V
Collector-Collector Voltage	100V
Emitter-Base Voltage (Note 2)	7V
Collector Current (Note 1)	10 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C ($\text{mW}/^\circ\text{C}$)	1.7	2.9	2.3	4.3

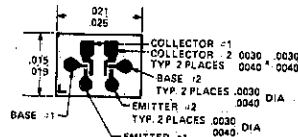
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4000



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS		
	MIN	MAX	MIN	MAX	MIN	MAX				
h_{FE}	DC Current Gain		200	600	150	600	80	800	V	$I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$ $I_C = 1.0 \text{mA}, V_{CE} = 5\text{V}$ $I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$
	$T_A = -55^\circ\text{C}$		225		175		100			
			75		50		30			
$V_{BE(on)}$	Emitter-Base On Voltage			0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage			0.35		0.35		0.35		
I_{CBO}	Collector Cutoff Current			0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45\text{V}, 30\text{V}^*$
	$T_A = 150^\circ\text{C}$			0.1		0.1		0.1*		
I_{EBO}	Emitter Cutoff Current			0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5\text{V}$
C_{obo}	Output Capacitance			0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5\text{V}$

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS	
	MIN	MAX	MIN	MAX	MIN	MAX			
C_{te}	Emitter Transition Capacitance			1	1	1	pF	$I_C = 0, V_{EB} = 0.5V$	
$C_{C1, C2}$	Collector to Collector Capacitance			0.8	0.8	0.8	pF	$V_{CC} = 0$	
$I_{C1, C2}$	Collector to Collector Leakage Current			5	5	5	pA	$V_{CC} = \pm 100V$	
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage		60		55		45	V	$I_C = 1mA, I_B = 0$
f_{t1}	Current Gain Bandwidth Product		200		150		150	MHZ	$I_C = 1mA, V_{CE} = 10V$
f_{t2}	Current Gain Bandwidth Product		20		15		15	MHZ	$I_C = 10\mu A, V_{CE} = 10V$
NF	Narrow Band Noise Figure			2	3		3	dB	$I_C = 10\mu A, V_{CE} = 5V, f = 1kHz, R_G = 10 kohms, BW = 200 Hz$
BV_{CBO}	Collector Base Breakdown Voltage		60		55		45	V	$I_C = 10\mu A, I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage		7		7		7	V	$I_E = 10\mu A, I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE1}/h_{FE2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A \text{ to } 1mA, V_{CE} = 5V$
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\mu A, V_{CE} = 5V$
$ I_{B1} - I_{B2} $	Base Current Differential		5		10		25	nA	$I_C = 10\mu A, V_{CE} = 5V$
$ \Delta(V_{BE1} - V_{BE2})/\Delta T $	Base Emitter Voltage Differential Change with Temperature		3		5		10	$\mu V/^\circ C$	$I_C = 10\mu A, V_{CE} = 5V, T_A = -55^\circ C \text{ to } +125^\circ C$
$ \Delta(I_{B1} - I_{B2})/\Delta T $	Base Current Differential Change with Temperature		0.3		0.5		1	$nA/^\circ C$	

SMALL SIGNAL CHARACTERISTICS

PARAMETER	TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	$I_C = 1mA, V_{CB} = 5V$
h_{rb}	Voltage Feedback Ratio	43	
h_{fe}	Small Signal Current Gain	250	$I_C = 1mA, V_{CE} = 5V$
h_{ob}	Output Conductance	60	
h_{ie}	Input Resistance	9.6	
h_{re}	Voltage Feedback Ratio	42	
h_{oe}	Output Conductance	12	$\mu mhos$

NOTES:

- Per transistor.
- The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μ amps.
- The lowest of two h_{FE} readings is taken as h_{FE1} for purposes of this ratio.

1



ITE4091-ITE4093 2N4091-2N4093, JANTX* N-Channel JFET

FEATURES

- Low $r_{DS(on)}$
- $I_D(OFF) < 100$ pA (JAN TX Types)
- Fast Switching

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	10.0 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	TO-18: 1.8W TO-92: 360 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$... 3.0 mW/ $^\circ\text{C}$

PIN CONFIGURATIONS

CHIP TOPOGRAPHY

ORDERING INFORMATION*

	TO-92	TO-18†	WAFER	DICE
ITE 4091	2N4091	2N4091/W	2N4091/W	2N4091/D
ITE 4091A	2N4091A			
ITE 4092	2N4092	2N4092/W	2N4092/W	2N4092/D
ITE 4092A	2N4092A			
ITE 4093	2N4093	2N4093/W	2N4093/W	2N4093/D
ITE 4093A	2N4093A			

†add JANTX to these part numbers if JANTX processing is desired.

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N/ITE 4091		2N/ITE 4092		2N/ITE 4093		Unit	Test Conditions	
	Min.	Max.	Min.	Max.	Min.	Max.			
BV_{GS}	Gate-Source Breakdown Voltage		-40		-40		V	$I_G = -1\mu\text{A}$, $V_{DS} = 0$	
$I_{D(O)}$	Drain Reverse Current			200		200	pA	$V_{GS} = -20\text{V}$, $I_S = 0$	
	(Not JANTX Specified); $T_A = 150^\circ\text{C}$			400		400	nA		
I_{RSS}	Gate Reverse Current		-100		-100		pA	$V_{GS} = -20\text{V}$, $V_{DS} = 0$	
	(JANTX, ITE devices only); $T_A = 150^\circ\text{C}$		-200		-200		nA		
$I_{D(OFF)}$	JANTX; $T_A = 25^\circ\text{C}$			100		100	pA	$V_{DS} = 20\text{V}$ $V_{GS} = -12\text{V}$ (4091) $V_{GS} = -8\text{V}$ (4092) $V_{GS} = -6\text{V}$ (4093)	
	Drain Cutoff Current			200		200	nA		
V_P	JANTX, $T_A = 150^\circ\text{C}$			400		400	nA	$V_{DS} = 20\text{V}$, $I_D = 1\text{ nA}$	
	Gate-Source Pinch-Off Voltage		-5	-10	-2	-7	-1		-5
I_{DSS}	Drain Current at Zero Gate Voltage		30		15		8	mA	$V_{GS} = 0$, Pulse Test Duration = 2 ms
$V_{DS(ON)}$	Drain-Source ON Voltage					0.2		V	$V_{GS} = 0$ $I_D = 2.5\text{ mA}$ $I_D = 4\text{ mA}$ $I_D = 6.6\text{ mA}$
						0.2			
						0.2			
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	$V_{GS} = 0$, $I_D = 1\text{ mA}$	
$r_{DS(off)}$	Static Drain Source ON Resistance		30		50		80	$V_{GS} = 0$; $I_D = 0$; $f = 1\text{ kHz}$	
C_{iss}	Common-Source Input Capacitance		16		16		16	$V_{DS} = 20\text{V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$	
C_{rss}	JANTX Only		5		5		5	$V_{DS} = 0$, $V_{GS} = -20\text{V}$, $f = 1\text{ MHz}$	
	Common-Source Reverse Transfer Capacitance		5		5		5		
$t_{d(ON)}$	Turn-ON Delay Time		15		15		20	$V_{DD} = 3\text{V}$, $V_{GS(ON)} = 0$ $I_{D(on)}$ $V_{GS(off)}$ R_s 4091 5.5 mA -12V 425 Ω 4092 4 mA -8V 700 Ω 4093 2.5 mA -6V 1120 Ω	
t_r	Rise Time		10		20		40		
t_{off}	Turn-OFF Time		40		60		80		



2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)

2N4044, 2N4878 60V

2N4100, 2N4879 55V

2N4045, 2N4880 45V

Collector-Collector Voltage 100V

Emitter-Base Voltage (Note 2) 7V

Collector Current (Note 1) 10 mA

Storage Temperature Range -65°C to $+200^\circ\text{C}$

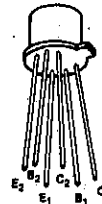
Operating Temperature Range -55°C to $+150^\circ\text{C}$

Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation ..	300 mW	500 mW	400 mW	750 mW
Derate above 25°C (mW/ $^\circ\text{C}$)	1.7	2.9	2.3	4.3

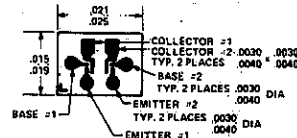
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4000



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200	600	150	600	80	800	V	$I_C = 10\ \mu\text{A}, V_{CE} = 5\text{V}$
		225		175		100			$I_C = 1.0\ \text{mA}, V_{CE} = 5\text{V}$
	$T_A = -55^\circ\text{C}$	75		50		30			$I_C = 10\ \mu\text{A}, V_{CE} = 5\text{V}$
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		$I_C = 1.0\ \text{mA}, I_B = 0.1\ \text{mA}$
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45\text{V}, 30\text{V}^*$
		$T_A = 150^\circ\text{C}$		0.1		0.1		0.1*	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5\text{V}$
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5\text{V}$

1

ELECTRICAL CHARACTERISTICS (25 °C unless otherwise noted)

PARAMETER	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
C_{te}	1		1		1		pF	$I_C = 0, V_{EB} = 0.5V$
$C_{C1, C2}$	0.8		0.8		0.8		pF	$V_{CC} = 0$
$I_{C1, C2}$	5		5		5		pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	60		55		45		V	$I_C = 1mA, I_B = 0$
f_t	200		150		150		MHz	$I_C = 1mA, V_{CE} = 10V$
f_t	20		15		15		MHz	$I_C = 10\mu A, V_{CE} = 10V$
NF	2		3		3		dB	$I_C = 10\mu A, V_{CE} = 5V$ $R_G = 10 \text{ kohms}$ $f = 1kHz$ $BW = 200 \text{ Hz}$
BV_{CBO}	60		55		45		V	$I_C = 10\mu A, I_E = 0$
BV_{EBO}	7		7		7		V	$I_E = 10\mu A, I_C = 0$

MATCHING CHARACTERISTICS (25 °C unless otherwise noted)

h_{FE1}/h_{FE2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A \text{ to } 1mA,$ $V_{CE} = 5V$
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\mu A, V_{CE} = 5V$
$ I_{B1} - I_{B2} $	Base Current Differential		5		10		25	nA	$I_C = 10\mu A, V_{CE} = 5V$
$ \Delta(V_{BE1} - V_{BE2})/\Delta T $	Base Emitter Voltage Differential Change with Temperature		3		5		10	$\mu V/^\circ C$	$I_C = 10\mu A,$ $V_{CE} = 5V$ $T_A = -55^\circ C \text{ to } +125^\circ C$
$ \Delta(I_{B1} - I_{B2})/\Delta T $	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	

SMALL SIGNAL CHARACTERISTICS

PARAMETER	TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	28	ohms	$I_C = 1mA, V_{CB} = 5V$
h_{rb}	43	$\times 10^{-3}$	
h_{fe}	250		
h_{ob}	60	$\mu mhos$	$I_C = 1mA, V_{CE} = 5V$
h_{ie}	9.6	k ohms	
h_{re}	42	$\times 10^{-3}$	
h_{oe}	12	$\mu mhos$	

NOTES:

- Per transistor.
- The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μ amps.
- The lowest of two h_{FE} readings is taken as h_{FE1} for purposes of this ratio.

2N4117-19, 2N4117A-19A N-Channel JFET

FEATURES

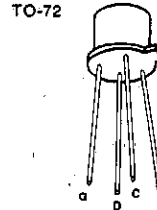
- Low Leakage
- Low Capacitance

ABSOLUTE MAXIMUM RATINGS

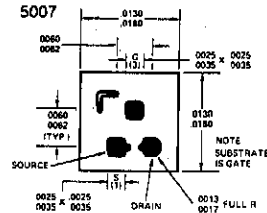
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	—	—
2N4118	2N4118/W	2N4118/D
2N4118A	—	—
2N4119	2N4119/W	2N4119/D
2N4119A	—	—

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4117		2N4118		2N4119		UNIT	TEST CONDITIONS
		2N4117A	MAX	2N4118A	MAX	2N4119A	MAX		
BV _{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1 \mu\text{A}$, $V_{DS} = 0$
I _{GSSR}	Gate Reverse Current		-10		-10		-10	pA	$V_{GS} = -20 \text{ V}$, $V_{DS} = 0$
		A devices	-1		-1		-1		
		$T_A = +100^\circ\text{C}$		-25		-25		-25	
V _{GS} (off)	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ nA}$
I _{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μmho	$V_{DS} = 10 \text{ V}$, $f = 1 \text{ kHz}$
g_{fs}	Common-Source Forward Transconductance	60		70		90			$V_{GS} = 0$, $f = 30 \text{ MHz}$
g_{os}	Common-Source Output Conductance		3		5		10	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ kHz}$
C _{iss}	Common-Source Input Capacitance		3		3		3		$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ kHz}$
C _{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5		$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ kHz}$

NOTE: 1. Pulse test: Pulse duration of 2 ms used during test.

1

2N4220 - 2N4222 N-Channel JFET

FEATURES

- $C_{rss} < 2 \text{ pF}$
- Moderately High Forward Transconductance

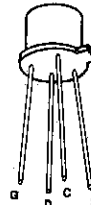
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ABSOLUTE MAXIMUM RATINGS

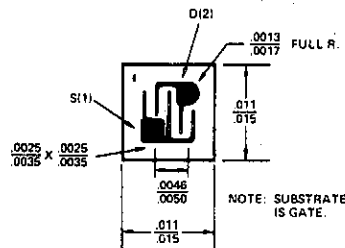
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION TO-72



CHIP TOPOGRAPHY 5010*



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4220		2N4221		2N4222		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{GSSR}	Gate Reverse Current	$T_A = 150^\circ\text{C}$							$V_{GS} = -15 \text{ V}, V_{DS} = 0$
			-0.1		-0.1		-0.1	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	$I_G = -10 \mu\text{A}, V_{DS} = 0$
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3	-4	-3	-4	-3	-4	V	$V_{DS} = 15 \text{ V}, I_D = 0.1 \text{ nA}$
V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-8	V	$V_{DS} = 15 \text{ V}$ $I_D = 50 \mu\text{A}$ (2N4220) $I_D = 200 \mu\text{A}$ (2N4221) $I_D = 500 \mu\text{A}$ (2N4222)
I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	2000	5000	2500	6000	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$
$ Y_{fs} $	Common-Source Forward Transadmittance	750		750		750			
g_{os}	Common-Source Output Conductance (Note 1)		10		20		40	μmho	f = 100 MHz
C_{iss}	Common-Source Input Capacitance		6		6		6		f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2	pF	f = 1 MHz

NOTE 1: Pulse test duration 2 ms.



2N4223, 2N4224 N-Channel JFET

FEATURES

- $NF = 3 \text{ dB}$ Typical at 200 MHz
- $C_{rss} < 2 \text{ pF}$

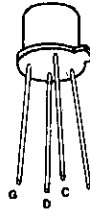
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

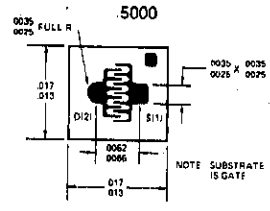
Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4223	2N4223/W	2N4223/D
2N4224	2N4224/W	2N4224/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4223		2N4224		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current $T_A = +150^\circ\text{C}$		-0.25		-0.5	nA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$	
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		μA	$I_G = -10 \mu\text{A}, V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	$V_{DS} = 15 \text{ V}$	$I_D = 0.25 \text{ nA}$ (2N4223) $I_D = 0.5 \text{ nA}$ (2N4224) $I_D = 0.3 \text{ mA}$ (2N4223) $I_D = 0.2 \text{ mA}$ (2N4224)
V_{GS}	Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5			
I_{DSS}	Saturation Drain Current (Note 1)	3	18	2	20			
g_{fs}	Common-Source Forward Transconductance (Note 1)	3000	7000	2000	7500	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	$f = 1 \text{ kHz}$
C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		$f = 1 \text{ MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
$ Y_{fs} $	Common-Source Forward Transadmittance	2700		1700		μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	$f = 200 \text{ MHz}$
g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
G_{ps}	Small Signal Power Gain	10					$V_{DS} = 15 \text{ V}, V_{GS} = 0, R_{gen} = 1 \text{ k}\Omega$	
NF	Noise Figure		5			dB		

Note 1: Pulse test, duration 2 msec.

1

FEATURES

- Exceptionally High Figure of Merit
- Radiation Immunity
- Extremely Low Noise and Capacitance
- High Input Impedance

APPLICATIONS

- Low-level Choppers
- Data Switches
- Multiplexers and Low Noise Amplifiers

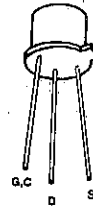
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

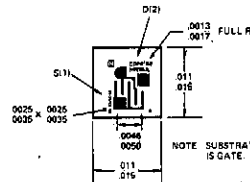
Gate-Source or Gate-Drain Voltage	-50V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY 5040



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N4338	2N4338/W	2N4338/D
2N4339	2N4339/W	2N4339/D
2N4340	2N4340/W	2N4340/D
2N4341	2N4341/W	2N4341/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N4338		2N4339		2N4340		2N4341		UNITS	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{GSS} Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	$V_{GS} = -30\text{ V}, V_{DS} = 0$
		-0.1		-0.1		-0.1		-0.1	μA	
BV_{GSS} Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6	nA	$V_{DS} = 15\text{ V}, I_D = 0.1\ \mu\text{A}$
$I_D(off)$ Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	$V_{DS} = 15\text{ V}, V_{GS} = ()$
I_{DSS} Saturation Drain Current	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	$V_{DS} = 15\text{ V}, V_{GS} = 0$
g_{fs} Common-Source Forward Transconductance	600	1800	800	2400	1300	3000	2000	4000	μmho	$V_{DS} = 15\text{ V}, V_{GS} = 0$
g_{os} Common-Source Output Conductance		5		15		30		60		
$r_{DS(on)}$ Drain-Source ON Resistance		2500		1700		1500		800	ohm	$V_{DS} = 0, I_{DS} = 0$
C_{iss} Common-Source Input Capacitance		7		7		7		7	pF	$V_{DS} = 15\text{ V}, V_{GS} = 0$
C_{rss} Common-Source Reverse Transfer Capacitance		3		3		3		3		
NF Noise Figure		1		1		1		1	dB	$V_{DS} = 15\text{ V}, V_{GS} = 0$ $R_{gen} = 1\text{ meg}, BW = 200\text{ Hz}$

2N4351 N-Channel Enhancement Mode MOS FET

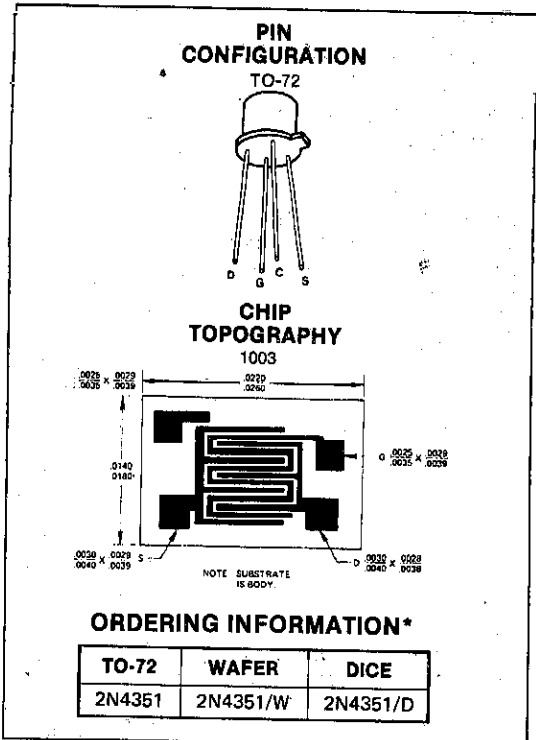
FEATURES

- Low ON Resistance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source Voltage or Drain-Gate Voltage	25V
Peak Gate-Source Voltage (Note 1)	$\pm 125\text{V}$
Drain Current	100 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	375 mW
Derate above 25°C	3 mW/ $^\circ\text{C}$



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*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Substrate connected to source.

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	25		V	$I_D = 10 \mu\text{A}$, $V_{GS} = 0$
I_{GSS}		10	pA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
I_{DSS}		10	nA	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$
$V_{GS(th)}$	1	.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 10 \mu\text{A}$
$I_{D(on)}$	3		mA	$V_{GS} = 10 \text{ V}$, $V_{DS} = 10 \text{ V}$
$V_{DS(on)}$		1	V	$I_D = 2 \text{ mA}$, $V_{GS} = 10 \text{ V}$
$r_{DS(on)}$		300	ohms	$V_{GS} = 10 \text{ V}$, $I_D = 0$, $f = 1 \text{ kHz}$
$ y_{fs} $	1000		μmho	$V_{DS} = 10 \text{ V}$, $I_D = 2 \text{ mA}$, $f = 1 \text{ kHz}$
C_{rss}		1.3	pF	$V_{DS} = 0$, $V_{GS} = 0$, $f = 140 \text{ kHz}$
C_{iss}		5.0		$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 140 \text{ kHz}$
$C_{d(sub)}$		5.0		$V_{D(SUB)} = 10 \text{ V}$, $f = 140 \text{ kHz}$
$t_{d(on)}$		45	ns	
t_r		65		
$t_{d(off)}$		60		
t_f		100		

Note 1. Device must not be tested at $\pm 125\text{V}$ more than once or longer than 300 ms.



ITE4391-ITE4393 2N4391-2N4393 N-Channel JFET

FEATURES

- $r_{ds(on)} \leq 30 \text{ ohms (2N4391)}$
- $I_{D(off)} < 100 \text{ pA}$
- Switches $\pm 10 \text{ VAC}$ with $\pm 15\text{V}$ Supplies (2N4392, 2N4393)

1

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage -40V
 Gate Current 50 mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$

	TO-18	TO-92
Power Dissipation	1.8W	360 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$	3.0 mW/ $^\circ\text{C}$

PIN CONFIGURATIONS

TO-18

TO-92

CHIP TOPOGRAPHY

ORDERING INFORMATION*

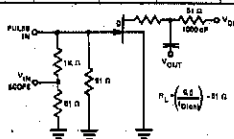
	TO-92	TO-18	WAFER	DICE
ITE 4391	2N4391	2N4391/W	2N4391/D	
ITE 4392	2N4392	2N4392/W	2N4392/D	
ITE 4393	2N4393	2N4393/W	2N4393/D	

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	4391		4392		4393		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
I_{GSS} Gate Reverse Current		-100		-100		-100	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$
BV_{GSS} Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = 1 \mu\text{A}, V_{DS} = 0$
$I_{D(off)}$ Drain Cutoff Current		100		100		100	pA	$V_{DS} = 20 \text{ V}, V_{GS} = -5 \text{ V (4393)}$ $V_{GS} = -7 \text{ V (4392)}$ $V_{GS} = -12 \text{ V (4391)}$
		200		200		200	nA	
$V_{GS(f)}$ Gate-Source Forward Voltage		1		1		1	V	$I_G = 1 \text{ mA}, V_{DS} = 0$
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ nA}$
I_{DSS} Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$
$V_{DS(on)}$ Drain Source ON-Voltage		0.4		0.4		0.4	V	$V_{GS} = 0$ $I_D = 3 \text{ mA (4393)}$ $I_D = 6 \text{ mA (4392)}$ $I_D = 12 \text{ mA (4391)}$
$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 1 \text{ mA}$
$r_{DS(on)}$ Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 0$
C_{iss} Common-Source Input Capacitance		14		14		14	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$
C_{rss} Common-Source Reverse Transfer Capacitance				3.5		3.5	pF	$V_{DS} = 0$ $V_{GS} = -5 \text{ V}$ $V_{GS} = -7 \text{ V}$ $V_{GS} = -12 \text{ V}$
t_d Turn-ON Delay Time		15		15		15	ns	$V_{DD} = 10 \text{ V}, V_{GS(on)} = 0$
t_r Rise Time		5		5		5	ns	$I_{D(on)} = 12 \text{ mA}, V_{GS(off)} = -12 \text{ V}$
t_{off} Turn-OFF Delay Time		20		35		50	ns	
t_f Fall Time		15		20		30	ns	

NOTE:

1. Pulse test required, pulse width = 300 μs , duty cycle $\leq 3\%$



INPUT PULSE

RISE TIME $< 0.5 \text{ ns}$
 FALL TIME $< 0.5 \text{ ns}$
 PULSE DUTY CYCLE 1%

SAMPLING SCOPE

RISE TIME 0.4 ns
 INPUT RESISTANCE 50 Ω

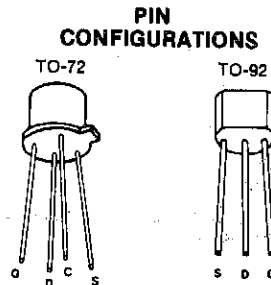
FEATURES

- Low Noise
- Low Feedback Capacitance
- Low Output Capacitance
- High Transconductance
- High Power Gain

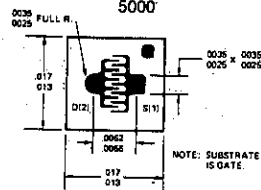
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	2N4416, ITE4416	-30V
	2N4416A	-35V
Gate Current		10 mA
Storage Temperature Range	2N4416/2N4416A	-65°C to +200°C
	ITE4416	-55°C to +125°C
Operating Temperature Range	2N4416/2N4416A	-65°C to +200°C
	ITE4416	-55°C to +125°C
Lead Temperature (Soldering, 10 sec.)		+300°C
Power Dissipation		300 mW
Derate, above 25°C	2N4416/2N4416A	1.7 mW/°C
	ITE4416	3.0 mW/°C



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	TO-72	WAFER	DICE
ITE 4416	2N4416	2N4416/W	2N4416/D
—	2N4416A	2N4416A/W	2N4416A/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS		
$V_{GS(f)}$	Gate-Source Forward Voltage		1	V	$I_G = 1 \text{ mA}, V_{DS} = 0$		
I_{GSS}	Gate Reverse Current		-0.1	nA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$		
			-0.1	μA			
		$T_A = 150^\circ\text{C}$					
BV_{GSS}	Gate-Source Breakdown Voltage	2N4416/ITE4416 -30		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$		
		2N4416A -35					
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N4416/ITE4416 -2.5	-6	V	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$		
		2N4416A -2.5	-6				
I_{DSS}	Drain Current at Zero Gate Voltage	5	15	mA			
g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$		
g_{os}	Common-Source Output Conductance		50	μmho			
C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF			
C_{iss}	Common-Source Input Capacitance		4	pF			
C_{oss}	Common-Source Output Capacitance		2	pF			
PARAMETER		100 MHz		400 MHz		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
g_{iss}	Common-Source Input Conductance		100		1000	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$
b_{iss}	Common-Source Input Susceptance		2500		10,000		
g_{oss}	Common-Source Output Conductance		75		100		
b_{oss}	Common-Source Output Susceptance		1000		4000		
g_{fs}	Common-Source Forward Transconductance			4000			
G_{ps}	Common-Source Power Gain	18		10			
NF	Noise Figure		2		4	dB	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ mA}$ $V_{DS} = 15 \text{ V}, I_D = 5 \text{ mA}, R_G = 1 \text{ K}\Omega$



2N4856-2N4861 2N4856-2N4858 JAN, JTX, JTXV* N-Channel JFET

1

FEATURES

- Low $r_{DS(on)}$
- $I_{D(off)} < 250$ pA
- Switches $\pm 10V$ Signals with $\pm 15V$ Supplies (2N4858, 2N4861)

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage		
2N4856-58	-40V
2N4859-61	-30V
Gate Current	50 mA
Storage Temperature	$-65^\circ C$ to $+200^\circ C$
Operating Temperature Range	$-55^\circ C$ to $+150^\circ C$
Led Temperature (Soldering, 10 sec.)	$+300^\circ C$
Power Dissipation	1.8W
Derate above $25^\circ C$	10 mW/ $^\circ C$

PIN CONFIGURATION

TO-18

CHIP TOPOGRAPHY

5001

ORDERING INFORMATION*

TO-18	WAFER	DICE
2N4856 †	2N4856/W	2N4856/D
2N4857 †	2N4857/W	2N4857/D
2N4858 †	2N4858/W	2N4858/D
2N4859	2N4859/W	2N4859/D
2N4860	2N4860/W	2N4860/D
2N4861	2N4861/W	2N4861/D

† add JAN, JTX, JTXV, to basic part number to specify these devices.

ELECTRICAL CHARACTERISTICS

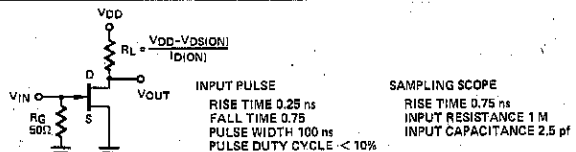
($25^\circ C$ unless otherwise noted)

*When ordering wafer/dice refer to Appendix B-23.

PARAMETER		2N4856,59		2N4857,60		2N4858,61		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
BV _{GSS}	Gate-Source Breakdown Voltage	2N4856-58	-40		-40		-40	V	$I_G = -1 \mu A, V_{DS} = 0$	
		2N4859-61	-30		-30		-30			
I _{GSSR}	Gate-Reverse Current	$T_A = 150^\circ C$		-250		-250		pA	$V_{GS} = -20 V, V_{DS} = 0$ $V_{GS} = -15 V, V_{DS} = 0$	
				-500		-500				-500
I _{D(off)}	Drain Cutoff Current	$T_A = 150^\circ C$		250		250		pA	$V_{DS} = 15 V, V_{GS} = -10 V$	
				500		500				500
V _{GS(off)}	Gate-Source Cutoff Voltage		-4 -10	-2	-6	-0.8	-4	V	$V_{DS} = 15 V, I_D = 0.5 nA$	
I _{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15 V, V_{GS} = 0$
V _{DS(on)}	Drain-Source ON Voltage		0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0, I_D = I$	
r _{ds(on)}	Drain-Source ON Resistance		25		40		60	ohm	$V_{GS} = 0, I_D = 0$	
C _{iss}	Common-Source Input Capacitance		18		18		18	pF	$V_{DS} = 0, V_{GS} = -10 V$	
C _{rss}	Common-Source Reverse Transfer Capacitance		8		8		8	pF	$f = 1 MHz$	
t _d	Turn-ON Delay Time		6		6		10	ns	$V_{DD} = 10 V, R_L = 464 \Omega$ (2N4856,59) $V_{GS(on)} = 0$ 953Ω (2N4857,60) 1910Ω (2N4858,61) $V_{GS(off)} = -10 V, I_D = 20 mA$ (2N4856, 9) $V_{GS(off)} = -6 V, I_D = 10 mA$ (2N4857, 60) $V_{GS(off)} = -4 V, I_D = 5 mA$ (2N4858, 61)	
t _r	Rise Time		3		4		10			
t _{off}	Turn-OFF Time		25		50		100			

NOTE:

1. Pulse test required, pulsewidth = 100 μs , duty cycle $\leq 10\%$.



FEATURES

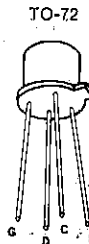
- Low Noise Voltage
- Low Leakage
- High Gain

ABSOLUTE MAXIMUM RATINGS

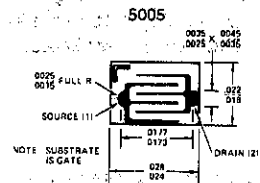
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-72	WAFER	DICE
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	$V_{GS} = -30\text{ V}, V_{DS} = 0$	
			-0.25		-0.25		-0.25	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		$V_{DS} = 20\text{ V}, I_D = 1\ \mu\text{A}$	
I_{DSS}	Saturation Drain Current (Note 1)	0.4	1.2	1	3	2.5	7.5	mA	$V_{DS} = 20\text{ V}, V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	2000	1000	3000	1300	4000	μmho	$V_{DS} = 20\text{ V}, V_{GS} = 0$	
g_{os}	Common-Source Output Conductance		1.5		4		10			f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF	f = 1 MHz	
C_{iss}	Common-Source Input Capacitance		25		25		25			
E_n	Short Circuit Equivalent Input Noise Voltage.		20		20		20	nV	$V_{DS} = 10\text{ V}, V_{GS} = 0$	f = 10 Hz
			10		10		10			f = 1 kHz
		A devices	10		10		10			f = 10 Hz
			5		5		5	$\sqrt{\text{Hz}}$	f = 1 kHz	
NF	Spot Noise Figure		1		1		1	dB	$V_{DS} = 10\text{ V}, V_{GS} = 0$ $R_{gen} = 20\text{ K}, (2\text{N4867 Series})$ $R_{gen} = 5\text{ K}, (2\text{N4867A Series})$	f = 1 kHz

NOTE: 1. Pulse test duration = 2 ms.



2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880 Dielectrically Isolated Dual NPN Transistor

1

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

ABSOLUTE MAXIMUM RATINGS

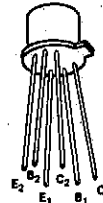
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)	2N4044, 2N4878	60V
	2N4100, 2N4879	55V
	2N4045, 2N4880	45V
Collector-Collector Voltage		100V
Emitter-Base Voltage (Note 2)		7V
Collector Current (Note 1)		10 mA
Storage Temperature Range		-65°C to $+200^\circ\text{C}$
Operating Temperature Range		-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)		$+300^\circ\text{C}$

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	300 mW	500 mW	400 mW	750 mW
Derate above 25°C ($\text{mW}/^\circ\text{C}$)	1.7	2.9	2.3	4.3

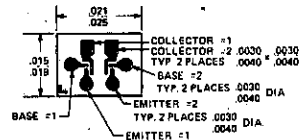
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4000



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044		2N4100		2N4045		UNIT	TEST CONDITIONS
		2N4878		2N4879		2N4880			
h_{FE}	DC Current Gain	200	600	150	600	80	800	V	$I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$
		225		175		100			$I_C = 1.0 \text{mA}, V_{CE} = 5\text{V}$
		$T_A = -55^\circ\text{C}$	75		50		30		
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7		
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35		$I_C = 1.0 \text{mA}, I_B = 0.1 \text{mA}$
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45 \text{V}, 30 \text{V}^*$
		$T_A = 150^\circ\text{C}$		0.1		0.1	0.1*	μA	
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5\text{V}$
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5\text{V}$

1

ELECTRICAL CHARACTERISTICS (25 °C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
C_{te}	Emitter Transition Capacitance		1		1		1	pF	$I_C = 0, V_{EB} = 0.5V$
C_{C1}, C_{C2}	Collector to Collector Capacitance		0.8		0.8		0.8	pF	$V_{CC} = 0$
I_{C1}, I_{C2}	Collector to Collector Leakage Current		5		5		5	pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		55		45		V	$I_C = 1mA, I_B = 0$
f_t	Current Gain Bandwidth Product	200		150		150		MHZ	$I_C = 1mA, V_{CE} = 10V$
f_t	Current Gain Bandwidth Product	20		15		15		MHZ	$I_C = 10\mu A, V_{CE} = 10V$
NF	Narrow Band Noise Figure		2		3		3	dB	$I_C = 10\mu A, V_{CE} = 5V, f = 1kHz$ $R_G = 10\text{ kohms}, BW = 200\text{ Hz}$
BV_{CBO}	Collector Base Breakdown Voltage	60		55		45		V	$I_C = 10\mu A, I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		V	$I_E = 10\mu A, I_C = 0$

MATCHING CHARACTERISTICS (25 °C unless otherwise noted)

h_{FE1}/h_{FE2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A \text{ to } 1mA, V_{CE} = 5V$
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\mu A, V_{CE} = 5V$
$ I_{B1} - I_{B2} $	Base Current Differential		5		10		25	nA	$I_C = 10\mu A, V_{CE} = 5V$
$ \Delta(V_{BE1} - V_{BE2})/\Delta T $	Base Emitter Voltage Differential Change with Temperature		3		5		10	$\mu V/^\circ C$	$I_C = 10\mu A, V_{CE} = 5V, T_A = -55^\circ C \text{ to } +125^\circ C$
$ \Delta(I_{B1} - I_{B2})/\Delta T $	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	

SMALL SIGNAL CHARACTERISTICS

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	ohms	$I_C = 1mA, V_{CB} = 5V$
h_{rb}	Voltage Feedback Ratio	43	$\times 10^{-3}$	
h_{fe}	Small Signal Current Gain	250		$I_C = 1mA, V_{CE} = 5V$
h_{ob}	Output Conductance	60	$\mu mhos$	
h_{ie}	Input Resistance	9.6	k ohms	
h_{re}	Voltage Feedback Ratio	42	$\times 10^{-3}$	
h_{oe}	Output Conductance	12	$\mu mhos$	

NOTES:

1. Per transistor.
2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10 μ amps.
3. The lowest of two h_{FE} readings is taken as h_{FE1} for purposes of this ratio.

1

FEATURES

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
- Purely Resistive

APPLICATIONS

- Analog Switches
- Commutators
- Choppers

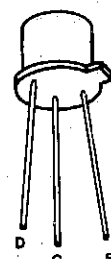
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V
 Gate Current 50 mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec.) $\pm 300^\circ\text{C}$
 Power Dissipation 500 mW
 Derate above 25°C 3 mW/ $^\circ\text{C}$

PIN CONFIGURATION

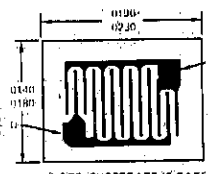
TO-18



D
G
S

CHIP TOPOGRAPHY

5508



NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

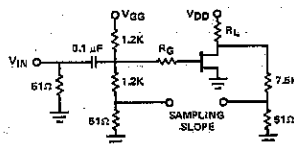
TO-18	WAFER	DICE
2N5018	2N5018/W	2N5018/D
2N5019	2N5019/W	2N5019/D

*When ordering wafer/dice refer to Appendix B-28.

ELÉCTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		2N5018		2N5019		Unit	Test Conditions
		Min	Max	Min	Max		
BV _{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1 \mu\text{A}, V_{DS} = 0$
I _{GSSR}	Gate Reverse Current		2		2	nA	$V_{GS} = 15 \text{ V}, V_{DS} = 0$
I _{D(off)}	Drain Cutoff Current		-10		-10	μA	$V_{DS} = -15 \text{ V}, V_{GS} = 12 \text{ V (2N5018)}$ $V_{GS} = 7 \text{ V (2N5019)}$
I _{DGO}	Drain Reverse Current		-2		-2	nA	$V_{DG} = -15 \text{ V}, I_S = 0$
V _{GS(off)}	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15 \text{ V}, I_D = -1 \mu\text{A}$
I _{DSS}	Saturation Drain Current	-10		-5		mA	$V_{DS} = -20 \text{ V}, V_{GS} = 0$
V _{DS(on)}	Drain-Source ON Voltage		-0.5		-0.5	V	$V_{GS} = 0, I_D = -6 \text{ mA (2N5018)}$ $I_D = -3 \text{ mA (2N5019)}$
r _{DS(on)}	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1 \text{ mA}, V_{GS} = 0$
r _{ds(on)}	Drain-Source ON Resistance		75		150	Ω	$I_D = 0, V_{GS} = 0$
C _{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15 \text{ V}, V_{GS} = 0$
C _{rss}	Common-Source Reverse Transfer Capacitance		10		10	pF	$V_{DS} = 0, V_{GS} = 12 \text{ V (2N5018)}$ $V_{GS} = 7 \text{ V (2N5019)}$
t _{d(on)}	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6 \text{ V}, V_{GS(on)} = 0$
t _r	Rise Time		20		75	ns	
t _{d(off)}	Turn-Off Delay Time		15		25	ns	
t _f	Fall Time		50		100	ns	

NOTE 1: Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



INPUT PULSE
 RISE TIME < 1 ns
 FALL TIME < 1 ns
 PULSE WIDTH 100 ns
 REPLETION RATE 1 MHz

SAMPLING SCOPE
 RISE TIME 0.4 ns
 INPUT RESISTANCE 10 M Ω
 INPUT CAPACITANCE 1.5 pF

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FEATURES

- Low ON Resistance
- $I_{D(off)} < 500 \text{ pA}$
- Switches directly from T²L Logic

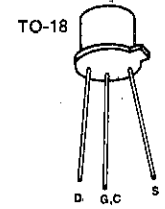
GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and $\pm 10 \text{ VAC}$ signals can be handled using only +5V logic (T²L or CMOS).

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Drain or Gate-Source Voltage 30V
 Gate Current 50 mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec.) ... $+300^\circ\text{C}$
 Power Dissipation 500 mW
 Derate above 25°C 3 mW/ $^\circ\text{C}$

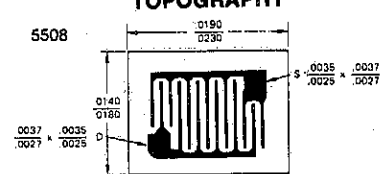
PIN CONFIGURATION



TO-18

D, G.C, S

CHIP TOPOGRAPHY



5508

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO18 †	WAFER	DICE
2N5114	2N5114/W	2N5114/D
2N5115	2N5115/W	2N5115/D
2N5116	2N5116/W	2N5116/D

† Add JAN, JTX to basic part number to specify these devices

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5114		2N5115		2N5116		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
BV _{GSS}	30	500	30	500	30	500	V	$I_G = 1 \mu\text{A}, V_{DS} = 0$
I _{GSSR}		1.0		1.0		1.0	μA	$V_{GS} = 20 \text{ V}, V_{DS} = 0$
I _{D(off)}		-1.0		-1.0		-1.0	μA	$V_{DS} = -15 \text{ V}, V_{GS} = 2\text{N}5115 = 7 \text{ V}$ $2\text{N}5116 = 5 \text{ V}$
V _p	5	10	3	6	1	4	V	$V_{DS} = -15 \text{ V}, I_D = -1 \text{ nA}$
I _{DSS}	-30	-90	-15	-60	-5	-25	mA	$V_{GS} = 0, V_{DS} = 2\text{N}5114 = -18 \text{ V}$ $2\text{N}5115 = -15 \text{ V}$ $2\text{N}5116 = -15 \text{ V}$
V _{GSSF}		-1		-1		-1	V	$I_G = -1 \text{ mA}, V_{DS} = 0$
V _{DS(on)}		-1.3		-0.8		-0.6	V	$V_{GS} = 0, I_D = 2\text{N}5114 = -15 \text{ mA}$ $2\text{N}5115 = -7 \text{ mA}$ $2\text{N}5116 = -3 \text{ mA}$
r _{DS(on)}		75		100		150	Ω	$V_{GS} = 0, I_D = -1 \text{ mA}$
r _{ds(on)}		75		100		150	Ω	$V_{GS} = 0, I_D = 0, f = 1 \text{ kHz}$
C _{iss}		25		25		25	pF	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$
C _{rss}		7		7		7	pF	$V_{DS} = 0, V_{GS} = 2\text{N}5114 = 12 \text{ V}$ $2\text{N}5115 = 7 \text{ V}$ $2\text{N}5116 = 5 \text{ V}$ $f = 1 \text{ MHz}$

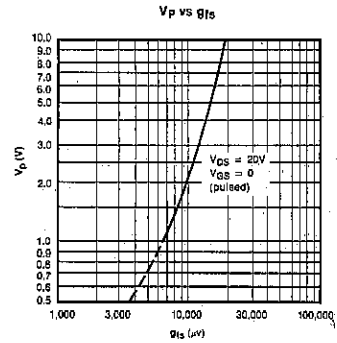
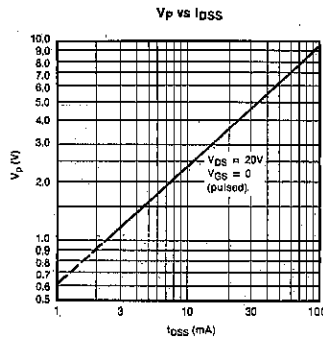
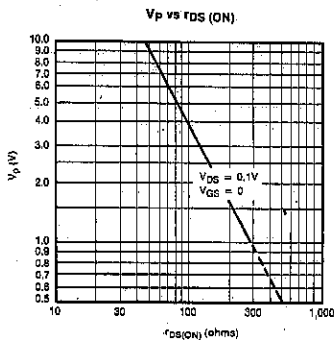
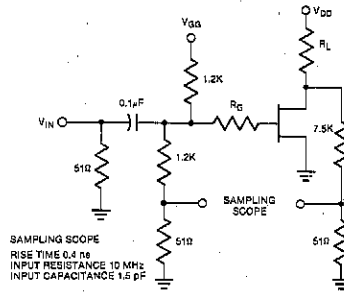
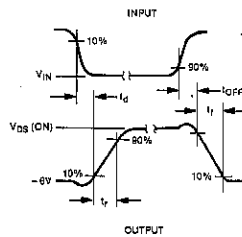
Note 1. Pulse test; duration = 2 ms.

SWITCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	UNIT
	MAX	MAX	MAX	MAX	MAX	MAX	
t_d Turn-ON Delay Time	6	10	12	6	10	25	ns
t_r Rise Time	10	20	30	10	20	35	
t_{off} Turn-OFF Delay Time	6	8	19	6	8	29	
t_f Fall Time	15	30	50	(not JAN TX specified)			

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TEST CONDITIONS			
	2N5114	2N5115	2N5116
V_{DD}	-10V	-6V	-6V
V_{GG}	20V	12V	8V
R_L	430Ω	910Ω	2 KΩ
R_G	100Ω	220Ω	390Ω
$I_{D(ON)}$	-15mA	-7mA	-3mA
V_{IN}	-12V	-7V	-5V





2N5117-2N5119 Dielectrically Isolated Dual PNP Transistor

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1) 45V
 Emitter-Base Voltage (Notes 1 and 2) 7V
 Collector-Collector Voltage 100V
 Collector Current (Note 1) 10 mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$

	ONE SIDE	BOTH SIDES
Power Dissipation	400 mW	750 mW
Derate above 25°C	2.3 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$

PIN CONFIGURATION

TO-78

CHIP TOPOGRAPHY

4501

EMITTER 0029 0029
0039 * 0039
TYP. 2 PLACES

BASE 0030 0030
0040 * 0040
TYP. 2 PLACES

COLLECTOR 0035 0034
0045 * 0044
TYP. 2 PLACES

ORDERING INFORMATION*

TO-78	WAFER	DICE
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

1

*When ordering wafer/dice refer to Appendix B-23

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117		2N5119		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	100	300	50			$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
		100		50			$I_C = 500 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
				20			$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
I_{CBO}	Collector Cutoff Current		0.1	0.1		nA	$I_E = 0, V_{CB} = 30 \text{ V}$
			0.1	0.1			μA
I_{EBO}	Emitter-Cutoff Current		0.1	0.1		nA	$I_C = 0, V_{EB} = 5.0 \text{ V}$
I_{C1-C2}	Collector-Collector Leakage		5.0	5.0		pA	$V_{CC} = 100 \text{ V}$
GBW	Current Gain Bandwidth Product	100		100		MHz	$I_C = 500 \mu\text{A}, V_{CE} = 10 \text{ V}$
C_{ob}	Output Capacitance		0.8	0.8		pF	$I_E = 0, V_{CB} = 5.0 \text{ V}$
C_{te}	Emitter Transition Capacitance		1.0	1.0			$I_C = 0, V_{EB} = 0.5 \text{ V}$
C_{C1-C2}	Collector-Collector Capacitance		0.8	0.8			$V_{CC} = 0$
$V_{CE0(sust)}$	Collector-Emitter Sustaining Voltage	45		45		V	$I_C = 1.0 \text{ mA}, I_B = 0$
NF	Narrow Band Noise Figure		4.0	4.0		dB	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$ $BW = 200 \text{ Hz}$ $f = 1 \text{ KHz}, R_G = 10 \text{ K}\Omega$
BV_{CBO}	Collector Base Breakdown Voltage	45		45		V	$I_C = 10 \mu\text{A}, I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7.0		7.0		V	$I_E = 10 \mu\text{A}, I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117		2N5118		2N5119		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
h_{FE1}/h_{FE2}	DC Current Gain Ratio (Note 3)	0.9	1.0	0.85	1.0	0.8	1.0		$I_C = 10 \mu\text{A}$ to $500 \mu\text{A}, V_{CE} = 5 \text{ V}$	
									$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$	
$V_{BE1}-V_{BE2}$	Base-Emitter Voltage Differential		3.0		5.0		5.0	mV	$I_C = 10 \mu\text{A}$ to $500 \mu\text{A}, V_{CE} = 5 \text{ V}$	
$I_{B1}-I_{B2}$	Base Current Differential		10.0		15		40	nA	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$	
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base Voltage Differential Change with Temperature		3.0		5.0		10	$\mu\text{V}/^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
$\Delta(I_{B1}-I_{B2})/\Delta T$	Base-Current Differential Change with Temperature		0.3		0.5		1.0	$\text{nA}/^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

1. Par transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed $10 \mu\text{A}$.
3. Lower of two h_{FE} readings is defined as h_{FE1} .

2N5196-2N5199

Dual Monolithic N-Channel JFET

ABSOLUTE MAXIMUM RATINGS

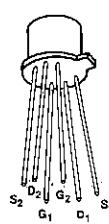
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate Current (Note 1)	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
ONE SIDE BOTH SIDE		
Power Dissipation	250 mW 500 mW
Derate above 25°C	2.6 mW/°C 4.3 mW/°C

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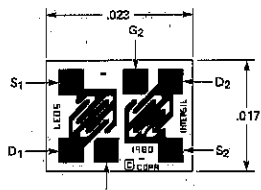
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

6037



ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-71	WAFER	DICE
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

*When ordering wafer/dice refer to Appendix B-23.

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS				
I_{GSSR}	Gate Reverse Current		-25	μA	$V_{GS} = -30\text{ V}, V_{DS} = 0$				
		$T_A = 150^\circ\text{C}$	-50	nA					
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$				
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4						
V_{GS}	Gate-Source Voltage	-0.2	-3.8						
I_G	Gate Operating Current		-15	μA	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$				
		$T_A = 125^\circ\text{C}$	-15	nA					
I_{DSS}	Saturation Drain Current (Note 2)	0.7	7	mA	$V_{DS} = 20\text{ V}, V_{GS} = 0$				
g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	$V_{DS} = 20\text{ V}, V_{GS} = 0$				
g_{fs}	Common-Source Forward Transconductance	700	1600			$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$			
g_{os}	Common-Source Output Conductance		50			$V_{DS} = 20\text{ V}, V_{GS} = 0$			
g_{os}	Common-Source Output Conductance		4			$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$			
C_{iss}	Common-Source Input Capacitance		6	pF	$V_{DS} = 20\text{ V}, V_{GS} = 0$				
C_{rss}	Common-Source Reverse Transfer Capacitance		2						
NF	Spot Noise Figure		0.5			$f = 100\text{ Hz}, R_G = 10\text{ M}\Omega$			
\bar{e}_n	Equivalent Input Noise Voltage		20	$\frac{\mu\text{N}}{\sqrt{\text{Hz}}}$	$f = 1\text{ kHz}$				
PARAMETER					UNIT	TEST CONDITIONS			
	2N5196		2N5197				2N5198		2N5199
$ I_{G1} - I_{G2} $	Differential Gate Current		5		5		5	nA	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}, 125^\circ\text{C}$
I_{DSS1} / I_{DSS2}	Saturation Drain Current Ratio (Note 2)	0.95	1	0.95	1	0.95	1		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$
g_{fs1} / g_{fs2}	Transconductance Ratio (Note 2)	0.97	1	0.97	1	0.95	1		$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		5		5		10	mV	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$
$\frac{\Delta(V_{GS1} - V_{GS2})}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 3)		5		10		20	$\mu\text{V}/^\circ\text{C}$	
			5		10		40		
$ g_{os1} - g_{os2} $	Differential Output Conductance		1		1		1	μmho	$f = 1\text{ kHz}$

- NOTES: 1. Per transistor.
 2. Pulse test required, pulsewidth = 300 μs , duty cycle < 3%.
 3. Measured at endpoints T_A and T_B .

FEATURES

- $G_{ps} = 15$ dB Minimum (Common Gate) at 450 MHz
- Low Noise
- Low Capacitance

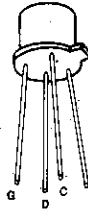
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

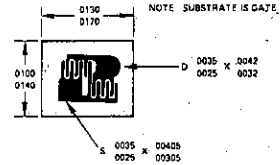
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5011



1

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N5397	2N5397/W	2N5397/D
2N5398	2N5398/W	2N5398/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5397		2N5398		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX		
I_{GSSR} Gate Reverse Current		-0.1		-0.1	nA	$V_{GS} = -15\text{ V}, V_{DS} = 0$
		-0.1		-0.1	μA	150°C
BV_{GSS} Gate-Source Breakdown Voltage	-25		-25		V	$V_{DS} = 0, I_G = -1\ \mu\text{A}$
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-1.0	-6.0	-1.0	-6.0		$V_{DS} = 10\text{ V}, I_D = 1\ \text{nA}$
I_{DSS} Saturation Drain Current (Note 1)	10	30	5	40	mA	$V_{DS} = 10\text{ V}, V_{GS} = 0$
$V_{GS(f)}$ Gate-Source Forward Voltage		1		1	V	$V_{DS} = 0, I_G = 1\ \text{mA}$
g_{fs} Common-Source Forward Transconductance (Note 1)	6000	10,000		5500 10,000	μmho	$V_{DS} = 10\text{ V}, I_D = 10\ \text{mA}$
g_{oss} Common-Source Output Conductance		200		400		$V_{DS} = 10\text{ V}, V_{GS} = 0$
C_{rss} Common-Source Reverse Transfer Capacitance		1.2		1.3	pF	$V_{DS} = 10\text{ V}, I_D = 10\ \text{mA}$
C_{iss} Common-Source Input Capacitance		5.0		5.5		$V_{DS} = 10\text{ V}, V_{GS} = 0$
g_{iss} Common-Source Input Conductance		2000		3000		$V_{DG} = 10\text{ V}, I_D = 10\ \text{mA}$
g_{oss} Common-Source Output Conductance		400		500	μmho	$V_{DG} = 10\text{ V}, V_{GS} = 0$
g_{fs} Common-Source Forward Transconductance (Note 1)	5500	9000		5000 10,000		$V_{DG} = 10\text{ V}, I_D = 10\ \text{mA}$
G_{ps} Common-Source Power Gain (neutralized)	15				dB	$V_{DG} = 10\text{ V}, I_D = 10\ \text{mA}$
NF Common-Source, Spot Noise Figure (neutralized)		3.5				$V_{GS} = 0$

Note 1: Pulse test duration = 2ms

FEATURES

- Low $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

1

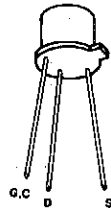
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source Voltage	-25V
Gate-Drain Voltage	-25V
Gate Current	100mA
Drain Current	400 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	2.3 mW/°C

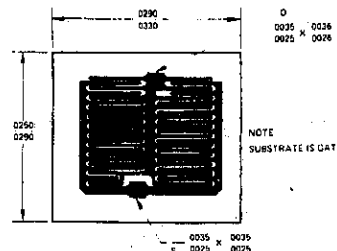
PIN CONFIGURATION

TO-52



CHIP TOPOGRAPHY

5018



ORDERING INFORMATION*

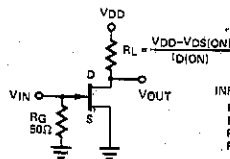
TO-52	WAFER	DICE
2N5432	2N5432/W	2N5432/D
2N5433	2N5433/W	2N5433/D
2N5434	2N5434/W	2N5434/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5432		2N5433		2N5434		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{GSSR}	Gate Reverse Current		-200		-200		-200	pA	$V_{GS} = -15\text{ V}, V_{DS} = 0$
			-200		-200		-200	nA	
BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	$V_{DS} = 5\text{ V}, V_{GS} = -10\text{ V}$
			200		200		200	nA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	$V_{DS} = 5\text{ V}, I_D = 3\text{ nA}$
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	$V_{DS} = 15\text{ V}, V_{GS} = 0$
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	$V_{GS} = 0, I_D = 10\text{ mA}$
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV	
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	$V_{GS} = 0, I_D = 0$
C_{iss}	Common-Source Input Capacitance		30		30		30	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15	pF	$V_{DS} = 0, V_{GS} = -10\text{ V}$
t_d	Turn-ON Delay Time		4		4		4	ns	$V_{DD} = 1.5\text{ V}, V_{GS(on)} = 0, V_{GS(off)} = -12\text{ V}, I_{D(on)} = 10\text{ mA}$
t_r	Rise Time		1		1		1	ns	
t_{off}	Turn-OFF Delay Time		6		6		6	ns	
t_f	Fall Time		30		30		30	ns	

NOTE: 1. Pulse test required, pulsewidth 300 μs , duty cycle $\leq 3\%$.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M Ω
INPUT CAPACITANCE 1.5 pF

146 Ω (2N5432)
143 Ω (2N5433)
140 Ω (2N5434)

2N5452-2N5454 Dual Monolithic N-Channel JFET

FEATURES

- Low Offset Voltage
- Low Drift
- Low Capacitance
- Low Output Conductance

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

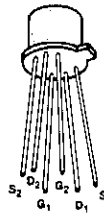
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate Drain Voltage (Note 1)	-50V	
Gate Current (Note 1)	50 mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	+300°C	
	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	2.9 mW/°C	4.3 mW/°C

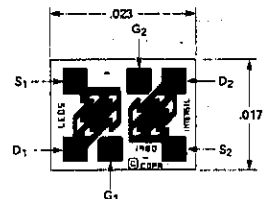
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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ORDERING INFORMATION*

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	%	2N5452		2N5453		2N5454		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSSR}	Gate Reverse Current		-100		-100		-100	μA	$V_{GS} = -30\text{V}, V_{DS} = 0$	
			-200		-200		-200	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	$V_{DS} = 0, I_G = -1\mu\text{A}$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5	V	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$	
V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	V	$V_{DS} = 20\text{V}, I_D = 50\mu\text{A}$	
$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2	V	$V_{DS} = 0, I_G = 1\text{mA}$	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	$V_{DS} = 20\text{V}, V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	$V_{DS} = 20\text{V}, V_{GS} = 0$ $f = 1\text{kHz}$	
g_{os}	Common-Source Output Conductance		3.0		3.0		3.0	μmho	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$ $f = 1\text{kHz}$	
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	$V_{DS} = 20\text{V}, V_{GS} = 0$	
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2	pF	$f = 1\text{MHz}$	
C_{dgs}	Drain-Gate Capacitance		1.5		1.5		1.5	pF	$V_{DG} = 10\text{V}, I_S = 0$	
e_n	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$V_{DS} = 20\text{V}, V_{GS} = 0$ $f = 1\text{kHz}$	
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	$V_{DS} = 20\text{V}, V_{GS} = 0$ $R_G = 10\text{M}\Omega$ $f = 100\text{Hz}$	
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0		$V_{DS} = 20\text{V}, V_{GS} = 0$	
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$	
$\Delta V_{GS1}-V_{GS2} $	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			$T = 25^\circ\text{C to } -55^\circ\text{C}$ $T = 25^\circ\text{C to } +125^\circ\text{C}$
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.95	1.0			
$ g_{os1}-g_{os2} $	Differential Output Conductance		0.25		0.25		0.25	μmhos	$f = 1\text{kHz}$	

NOTE: 1. Per transistor.



2N5457-2N5459 N-Channel JFET

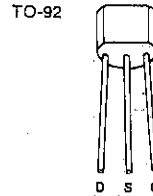
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

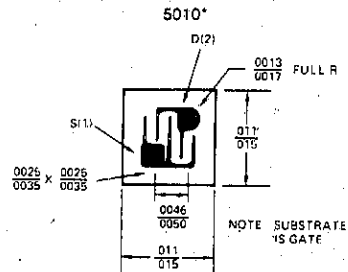
Drain-Gate Voltage	25V
Drain-Source Voltage	25V
Continuous Forward Gate Current	10 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

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PIN CONFIGURATION



CHIP TOPOGRAPHY



*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5457	2N5457/W	2N5457/D
2N5458	2N5458/W	2N5458/D
2N5459	2N5459/W	2N5459/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		V	$I_G = -10\ \mu\text{A}$, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current		.05	-1.0 -200	nA	$V_{GS} = -15\ \text{V}$, $V_{DS} = 0$ $V_{GS} = -15\ \text{V}$, $V_{DS} = 0$, $T_A = 100^\circ\text{C}$
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	2N5457 -0.5 2N5458 -1.0 2N5459 -2.0		-6.0 -7.0 -8.0	V	$V_{DS} = 15\ \text{V}$, $I_D = 10\ \text{mA}$
V_{GS}	Gate-Source Voltage	2N5457 2N5458 2N5459	2.5 3.5 4.5		V	$V_{DS} = 15\ \text{V}$, $I_D = 100\ \mu\text{A}$ $V_{DS} = 15\ \text{V}$, $I_D = 200\ \mu\text{A}$ $V_{DS} = 15\ \text{V}$, $I_D = 400\ \mu\text{A}$
I_{DSS}	Zero-Gate-Voltage Drain Current	2N5457 2N5458 2N5459	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mA $V_{DS} = 15\ \text{V}$, $V_{GS} = 0$
$ y_{fs} $	Forward Transfer Admittance	2N5457 2N5458 2N5459	1000 1500 2000	3000 4000 4500	5000 5500 6000	μmho $V_{DS} = 15\ \text{V}$, $V_{GS} = 0$, $f = 1\ \text{kHz}$
$ y_{os} $	Output Admittance		10	50	μmho	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0$, $f = 1\ \text{kHz}$
C_{iss}	Input Capacitance		4.5	7.0	pF	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$
C_{rss}	Reverse Transfer Capacitance		1.5	3.0	pF	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$
NF	Noise Figure			3.0	dB	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0$, $R_G = 1\ \text{MHz}$ $BW = 1\ \text{Hz}$, $f = 1\ \text{kHz}$

Pulse test required. $PW \leq 630\ \text{ms}$, duty cycle $\leq 10\%$

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

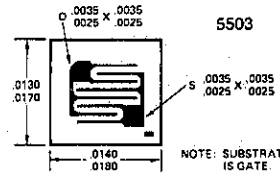
Drain-Gate or Source-Gate Voltage	
2N5460 - 2N5462	40V
2N5463 - 2N5465	60V
Gate Current	10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	310 mW
Derate above 25°C	2.8 mW/°C

PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

*When ordering wafer/dice refer to Appendix B-23.

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS			
BV _{GSS}	Gate-Source Breakdown Voltage	2N5460, 2N5461, 2N5462	40			V	I _G = 10 μA, V _{DS} = 0		
		2N5463, 2N5464, 2N5465	60						
V _{GS(off)}	Gate-Source Cutoff Voltage	2N5460, 2N5463	0.75	6.0		V	V _{DS} = 15 Vdc, I _D = 1.0 μA		
		2N5461, 2N5464	1.0	7.5					
		2N5462, 2N5465	1.8	9.0					
I _{GSSR}	Gate Reverse Current	2N5460, 2N5461, 2N5462		5.0		nA	V _{DS} = 0		
			2N5463, 2N5464, 2N5465		5.0				
		TA = 100°C	2N5460, 2N5461, 2N5462		1.0			μA	V _{GS} = 20V
			2N5463, 2N5464, 2N5465		1.0				V _{GS} = 30V
					1.0				V _{GS} = 20V
		1.0		V _{GS} = 30V					
I _{DSS}	Zero-Gate Voltage Drain Current	2N5460, 2N5463	-1.0	-5.0		mA	V _{DS} = -15V		
		2N5461, 2N5464	-2.0	-9.0					
		2N5462, 2N5465	-4.0	-16					
		2N5460, 2N5463	0.5	4.0					
V _{GS}	Gate-Source Voltage	2N5461, 2N5464	0.8	4.5		V	V _{GS} = 0		
		2N5462, 2N5465	1.5	6.0			I _D = 0.1 mA		
							I _D = -0.2 mA		
						I _D = -0.4 mA			
g _{fs}	Forward Transadmittance	2N5460, 2N5463	1000	4000		μmho	V _{DS} = -15V V _{GS} = 0V		
		2N5461, 2N5464	1500	5000					
		2N5462, 2N5465	2000	6000					
g _{os}	Output Admittance			75					
C _{iss}	Input Capacitance		5.0	7					
C _{rss}	Reverse Transfer Capacitance		1.0	2.0					
NF	Common-Source Noise Figure		1.0	2.5					
e _n	Equivalent Short-Circuit Input Noise Voltage		.60	115		nV/√Hz	f = 1.0 kHz BW = 1.0 Hz R _G = 1.0 MΩ		



2N5484-2N5486 N-Channel JFET

FEATURES

- Up to 400 MHz Operation
- Economy Packaging
- $C_{rss} < 1.0$ pF

1

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain-Gate Voltage	25V
Source Gate Voltage	25V
Drain Current	30 mA
Forward Gate Current	10 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	310 mW
Derate above 25°C	2.8 mW/ $^\circ\text{C}$

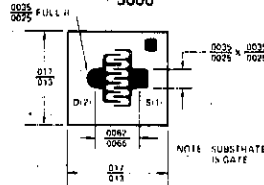
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5000



ORDERING INFORMATION*

TO-92	WAFER	DICE
2N5484	2N5484/W	2N5484/D
2N5485	2N5485/W	2N5485/D
2N5486	2N5486/W	2N5486/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5484		2N5485		2N5486		UNITS	TEST CONDITIONS		
	MIN	MAX	MIN	MAX	MIN	MAX				
I_{GSSR}	Gate Reverse Current $T_A = 100^\circ\text{C}$		-1.0	-1.0	-1.0	-1.0	nA	$V_{GS} = -20\text{ V}, V_{DS} = 0$		
BV_{GSS}	Gate-Source Breakdown Voltage		-25	-25	-25	-25	V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$		
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-0.3	-3.0	-0.5	-4.0	-2.0	-6.0	$V_{DS} = 15\text{ V}, I_D = 10\text{ mA}$	
I_{DSS}	Saturation Drain Current		1.0	5.0	4.0	10	8.0	20	$V_{DS} = 15\text{ V}, V_{GS} = 0$ (Note 1)	
g_{fs}	Common-Source Forward Transconductance		3000	6000	3500	7000	4000	8000	$f = 1\text{ kHz}$	
g_{os}	Common-Source Output Conductance			50		50		75	$f = 100\text{ MHz}$	
$Re(f_{fs})$	Common-Source Forward Transconductance		2500		3000		3500		$f = 400\text{ MHz}$	
$Re(f_{os})$	Common-Source Output Conductance			75		100	100		$f = 100\text{ MHz}$	
$Re(f_{is})$	Common-Source Input Conductance			100		1000	1000		$f = 400\text{ MHz}$	
C_{iss}	Common-Source Input Capacitance			5.0		5.0	5.0		$f = 100\text{ MHz}$	
C_{rss}	Common-Source Reverse Transfer Capacitance			1.0		1.0	1.0		$f = 1\text{ MHz}$	
C_{oss}	Common-Source Output Capacitance			2.0		2.0	2.0			
NF	Noise Figure		2.5	2.5	2.5	2.5		$V_{DS} = 15\text{ V}, V_{GS} = 0, R_G = 1\text{ M}\Omega$	$f = 1\text{ kHz}$	
			3.0					$V_{DS} = 15\text{ V}, I_D = 1\text{ mA}, R_G = 1\text{ k}\Omega$	$f = 100\text{ MHz}$	
				2.0	2.0	2.0		$V_{DS} = 15\text{ V}, I_D = 4\text{ mA}, R_G = 1\text{ k}\Omega$	$f = 400\text{ MHz}$	
				4.0	4.0	4.0				
G_{ps}	Common-Source Power Gain		16	25				$V_{DS} = 15\text{ V}, I_D = 1\text{ mA}$	$f = 100\text{ MHz}$	
					18	30	18	30		$f = 100\text{ MHz}$
					10	20	10	20		$f = 400\text{ MHz}$
									$V_{DS} = 15\text{ V}, I_D = 4\text{ mA}$	$f = 400\text{ MHz}$

NOTE: Pulse test required. Pulse width = 300 μs , duty cycle $\leq 3\%$.



2N5515-2N5524 Monolithic Dual N-Channel JFET

1

FEATURES

- Tight Temperature Tracking
- Tight Matching
- High Common Mode Rejection
- Low Noise

ABSOLUTE MAXIMUM RATINGS

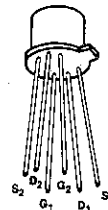
(T_A = 25°C unless otherwise specified)

Gate-Source or Gate-Drain Voltage	-40V	
Gate Current (Note 1)	50 mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	+300°C	

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/°C	7.7 mW/°C

PIN CONFIGURATION

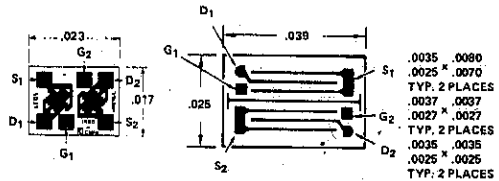
TO-71



CHIP TOPOGRAPHY

(2N5515-19)
6037

(2N5520-24)
6019



ALL BOND PADS ARE 4 x 4 MIL.

ORDERING INFORMATION*

TO-72	WAFER	DICE
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520		
2N5521		
2N5522		
2N5523		
2N5524		

*When ordering wafer/dice refer to Appendix B-23.

NOTE: Per transistor.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

1

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I _{GSSR}	Gate Reverse Current	T _A = 150°C		pA	V _{GS} = -30 V, V _{DS} = 0	
			-250	nA		
BV _{GSS}	Gate-Source Breakdown Voltage	-40		V	I _G = -1 μA, V _{DS} = 0	
V _p	Gate-Source Pinch-Off Voltage	-0.7	-4			
I _{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.5	7.5	mA	V _{DS} = 20 V, I _D = 1 nA	
g _{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V _{DS} = 20 V, V _{GS} = 0	
g _{oss}	Common-Source Output Conductance		10			f = 1 kHz
C _{rSS}	Common-Source Reverse Transfer Capacitance		5	pF		f = 1 MHz
C _{iSS}	Common-Source Input Capacitance		25			
ē _n	Equivalent Input Noise Voltage	2N5515-19		30	nV/√Hz	f = 10 Hz
		2N5520-24		15		f = 1 kHz
		2N5515-24		10		
I _G	Gate Current	T _A = 125°C		pA	V _{DG} = 20 V, I _D = 200 μA	
V _{GS}	Gate Source Voltage	-0.2	-3.8	V		
g _{fs}	Common-Source Forward Transconductance (Note 1)	500	1000	μmho		f = 1 kHz
g _{oss}	Common-Source Output Conductance		1	μmho		

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT	TEST CONDITIONS		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
I _{DSS1}	Drain Current Ratio at												V _{DS} = 20 V, V _{GS} = 0	
I _{DSS2}	Zero Gate Voltage (Note 1)													
I _{G1} - I _{G2}	Differential Gate Current (+125°C)												nA	V _{DG} = 20 V, I _D = 200 μA
g _{fs1}	Transconductance Ratio												μmho	V _{DG} = 20 V, I _D = 200 μA f = 1 kHz
g _{fs2}	(Note 1)													
g _{oss1} - g _{oss2}	Differential Output Conductance												μmho	V _{DG} = 20 V, I _D = 200 μA f = 1 kHz
V _{GS1} - V _{GS2}	Differential Gate-Source Voltage												mV	V _{DG} = 20 V, I _D = 200 μA
Δ V _{GS1} - V _{GS2} ΔT	Gate-Source Voltage Differential Drift (T _A = -55°C to +125°C)												μV/°C	V _{DG} = 20 V, I _D = 200 μA
CMRR	Common Mode Rejection Ratio (Note 2)												dB	V _{DD} = 10 to 20 V, I _D = 200 μA

NOTES:

1. Pulse duration of 28 ms used during test.
2. CMRR = 20 Log₁₀ ΔV_{DD} / Δ|V_{GS1} - V_{GS2}|, (ΔV_{DD} = 10V)

FEATURES

- Economy Packaging
- Fast Switching
- Low Drain-Source 'ON' Resistance

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain-Source Voltage	30V
Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Forward Gate Current	10 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	310 mW
Derate above 25°C	2.8 mW/ $^\circ\text{C}$

PIN CONFIGURATION

TO-92

CHIP TOPOGRAPHY

5001

ORDERING INFORMATION*

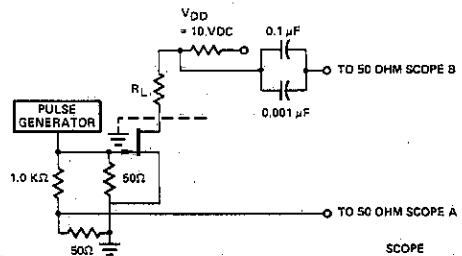
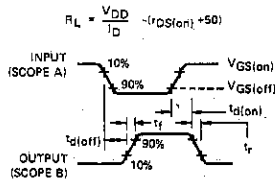
TO-92	WAFER	DICE
2N5638	2N5638/W	2N5638/D
2N5639	2N5639/W	2N5638/D
2N5640	2N5640/W	2N5640/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	2N5638		2N5639		2N5640		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	-30		-30		-30		V	$I_G = -10 \mu\text{A}$, $V_{DS} = 0$
I_{GSSR}	-1.0		-1.0		-1.0		nA	$V_{GS} = -15 \text{ V}$, $V_{DS} = 0$
$I_{D(off)}$	$T_A = 100^\circ\text{C}$		$T_A = 100^\circ\text{C}$		$T_A = 100^\circ\text{C}$		μA	$V_{DS} = 15 \text{ V}$, $V_{GS} = -12 \text{ V}$ (2N5638) $V_{GS} = -8 \text{ V}$ (2N5639), $V_{GS} = -6 \text{ V}$ (2N5640)
	1.0		1.0		1.0			
I_{DSS}	50		25		5.0		mA	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0$ (Note 1)
$V_{DS(on)}$	0.5		0.5		0.5		V	$V_{GS} = 0$, $I_D = 12 \text{ mA}$ (2N5638), $I_D = 6 \text{ mA}$ (2N5639), $I_D = 3 \text{ mA}$ (2N5640)
$r_{DS(on)}$	30		60		100		Ω	$I_D = 1 \text{ mA}$, $V_{GS} = 0$
$r_{dS(on)}$	30		60		100		Ω	$V_{GS} = 0$, $I_D = 0$
C_{iss}	10		10		10		pF	$V_{GS} = -12 \text{ V}$, $V_{DS} = 0$
C_{rss}	4.0		4.0		4.0		pF	$f = 1 \text{ MHz}$
$t_{d(on)}$	4.0		6.0		8.0		ns	$V_{DD} = 10 \text{ V}$, $I_{D(on)} = 12 \text{ mA}$ (2N5638)
t_r	5.0		8.0		10		ns	$V_{GS(on)} = 0$, $I_{D(on)} = 6 \text{ mA}$ (2N5639)
t_d	5.0		10		15		ns	$V_{GS(off)} = -10 \text{ V}$, $I_{D(on)} = 3 \text{ mA}$ (2N5640)
t_f	10		20		30		ns	$R_G = 50 \Omega$

NOTE: 1. Pulse test; $PW \leq 300 \mu\text{s}$, duty cycle $\leq 3.0\%$.



SCOPE
TEKTRONIX 567A
OR EQUIVALENT

2N5902-2N5909 Monolithic Dual N-Channel JFET

1

FEATURES

- Tight Tracking
- Good Matching

ABSOLUTE MAXIMUM RATINGS

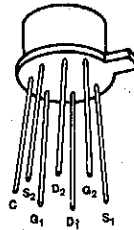
($T_A = 25^\circ\text{C}$ unless otherwise specified)

Gate-Drain or Gate-Source

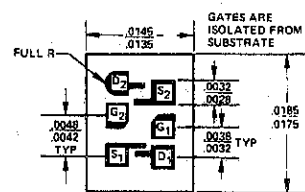
Voltage (Note 1)	-40V
Gate Current (Note 1)	10 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$

	ONE SIDE	BOTH SIDES
Power Dissipation	367 mW	500 mW
Derate above 25°C	3 mW/ $^\circ\text{C}$	4 mW/ $^\circ\text{C}$

PIN CONFIGURATION TO-99



CHIP TOPOGRAPHY 6015



ORDERING INFORMATION*

TO-99	WAFER	DICE	TO-99	WAFER	DICE
2N5902	2N5902/W	2N5902/D	2N5906	2N5906/W	2N5906/D
2N5903	2N5903/W	2N5903/D	2N5907	2N5907/W	2N5907/D
2N5904	2N5904/W	2N5904/D	2N5908	2N5908/W	2N5908/D
2N5905	2N5905/W	2N5905/D	2N5909	2N5905/W	2N5909/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5902-5		2N5906-9		UNIT	TEST CONDITIONS				
		MIN	MAX	MIN	MAX						
I_{GSSR}	Gate Reverse Current		-5		-2	pA	$V_{GS} = -20\text{ V}, V_{DS} = 0$				
			-10		-5	nA					
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$				
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$				
V_{GS}	Gate Source Voltage		-4		-4	V					
I_G	Gate Operating Current		-3		-1	pA	$V_{DG} = 10\text{ V}, I_D = 30\ \mu\text{A}$				
			-3		-1	nA					
I_{DSS}	Saturation Drain Current	30	500	30	500	μA					
g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho	$V_{DS} = 10\text{ V}, V_{GS} = 0$				
g_{os}	Common-Source Output Conductance		5		5	μmho					
C_{iss}	Common-Source Input Capacitance		3		3	pF	$f = 1\text{ MHz}$				
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5	pF					
g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	$V_{DG} = 10\text{ V}, I_D = 30\ \mu\text{A}$				
g_{os}	Common-Source Output Conductance		1		1	μmho					
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$	$f = 1\text{ kHz}$				
NF	Spot Noise Figure		3		1	dB	$V_{DS} = 10\text{ V}, V_{GS} = 0$ $f = 100\text{ Hz}$ $R_G = 10\text{ M}\Omega$				
PARAMETER		2N5902-6		2N5903-7		2N5904-8		2N5905-9		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$ I_{G1}-I_{G2} $	Differential Gate Current		2.0		2.0		2.0		2.0	nA	$V_{DG} = 10\text{ V}, I_D = 30\ \mu\text{A}, T_A = 125^\circ\text{C}$
			0.2		0.2		0.2		0.2		2N5902-5 2N5906-9
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1	0.95	1	0.95	1		$V_{DS} = 10\text{ V}, V_{GS} = 0$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1		$f = 1\text{ kHz}$
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage		5		5		10		15	mV	
$\frac{\Delta V_{BS1}-V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)		5		10		20		40	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 10\text{ V}, I_D = 30\ \mu\text{A}$ $T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$ $f = 1\text{ kHz}$
$ g_{os1}-g_{os2} $	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho	

NOTE 1: Per transistor.



2N5911, 2N5912 IT5911, IT5912 Monolithic Dual N-Channel JFET

FEATURES

- Tight Tracking
- Low Insertion Loss
- Good Matching

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

	TO-71		TO-99	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Power Dissipation	300 mW	500 mW	300 mW	500 mW
Derate above 25°C	1.7 mW/°C	2.9 mW/°C	3.0 mW/°C	4.0 mW/°C

PIN CONFIGURATION

TO-99 TO-71

CHIP TOPOGRAPHY

6022

ORDERING INFORMATION*

TO-71	TO-99	WAFER	DICE
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS					
I_{GSSR}	Gate Reverse Current		-100	pA	$V_{GS} = -15\text{ V}, V_{DS} = 0$					
		$T_A = 150^\circ\text{C}$	-250	nA						
BV_{GSS}	Gate Reverse Breakdown Voltage	-25		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$ $V_{DS} = 10\text{ V}, I_D = 1\text{ nA}$					
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5							
V_{GS}	Gate-Source Voltage	-0.3	-4		$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}$					
I_G	Gate Operating Current		-100	pA						
			-100	nA	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$					
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs , duty cycle $\leq 3\%$)	7	40	mA						
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}$					
g_{os}	Common-Source Output Conductance		100							
g_{oss}	Common-Source Output Conductance		150							
C_{iss}	Common-Source Input Capacitance		5	pF			f = 1 kHz			
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2				f = 100 MHz			
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage		20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$			f = 1 kHz			
NF	Spot Noise Figure		1				dB	f = 10 kHz $R_G = 100\text{ k}\Omega$		
PARAMETER		IT, 2N5911		IT, 2N5912			UNIT	TEST CONDITIONS		
$ I_{G1} - I_{G2} $	Differential Gate Current		20				20	nA	$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}, 125^\circ\text{C}$	
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95			1		$V_{DS} = 10\text{ V}, V_{GS} = 0$ (Pulsewidth 300 μs , duty cycle $\leq 3\%$)	
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		10		15	mV	$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}$			
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		20		40	$\mu\text{V}/^\circ\text{C}$			$T_A = 25^\circ\text{C}$	
			20		40				$T_B = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1		f = 1 kHz			



2N6483-2N6485 Monolithic Low Noise Dual N-Channel JFET

FEATURES

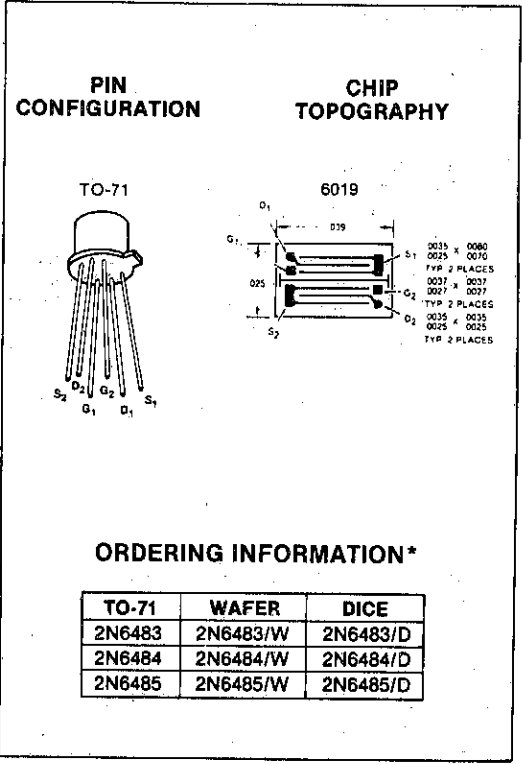
- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking

1

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate-Gate Voltage	$\pm 50\text{V}$
Gate Current (Note 1)	50 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW / 500 mW
Derate above 25°C	3.8 mW/ $^\circ\text{C}$ / 7.7 mW/ $^\circ\text{C}$



ORDERING INFORMATION*

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		200	μA	$V_{GS} = -30\text{V}, V_{DS} = 0,$ $T_A = 150^\circ\text{C}$
			200	nA	
BV_{GSS}	Gate Source Breakdown Voltage	50		V	$I_G = 1\mu\text{A}, V_{DS} = 0$
V_P	Gate Source Pinch Off Voltage	0.7	4.0	V	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	$V_{DS} = 20\text{V}, V_{GS} = 0$
g_{fs}	Common Source Forward Transconductance (Note 2)	1000	4000	μmho	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{KHz}$
g_{oss}	Common Source Output Conductance		10		
C_{iss}	Common Source Input Capacitance		20	pF	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{MHz}$
C_{rss}	Common Source Reverse Transfer Capacitance		3.5		
I_G	Gate Current		100	μA	$V_{GD} = 20\text{V}, I_D = 200\mu\text{A},$ $T_A = 150^\circ\text{C}$
			100	nA	
V_{GS}	Gate Source Voltage	0.2	3.8	V	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$
g_{fs}	Common Source Forward Transconductance	500	1500	μmho	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{KHz}$
g_{os}	Common Source Output Conductance		1		
\bar{e}_n	Equivalent Input Noise Voltage		10	$\text{nV}/\sqrt{\text{Hz}}$	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 10\text{Hz}$ $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{KHz}$
			5		

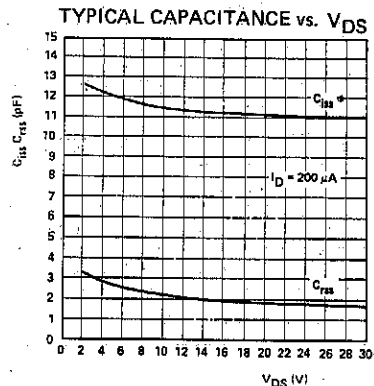
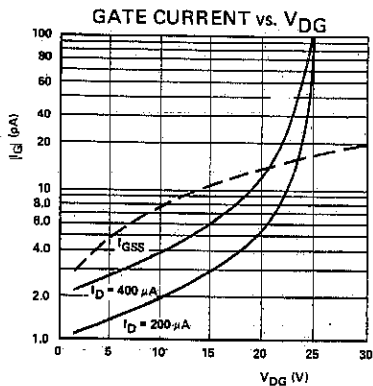
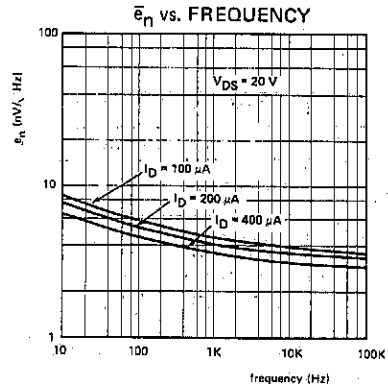
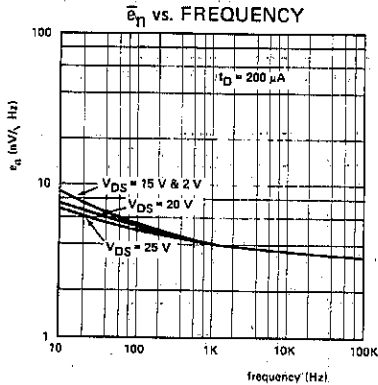
NOTES: 1. Per transistor.
2. Pulse test required; pulse width = 2 ms.

MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	PARAMETER	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1		$V_{DS} = 20\text{ V}, V_{GS} = 0$ (Note 2)
$ I_{G1} - I_{G2} $	Differential Gate Current		10		10		10	nA	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ $T_A = +125^\circ\text{C}$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1		$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A},$ $f = 1\text{ KHz}$ (Note 2)
$ g_{os1} - g_{os2} $	Differential Output Conductance		0.1		0.1		0.1	μmho	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A},$ $f = 1\text{ KHz}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		5		10		15	mV	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$
$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	100		100		90		dB	$V_{DD} = 10$ to $20\text{ V},$ $I_D = 200\ \mu\text{A}$ (Note 3)

- NOTES:**
1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
 2. Pulse duration of 2 ms used during test.
 3. $\text{CMRR} = 20\text{Log}_{10} \Delta V_{DD} / \Delta V_{GS1} - V_{GS2}$, ($\Delta V_{DD} = 10\text{ V}$), not included in JEDEC registration

TYPICAL OPERATING CHARACTERISTICS





IMF6485 Monolithic Low Noise Dual N-Channel JFET

FEATURES

- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking

1

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V	
Gate-Gate Voltage	$\pm 50\text{V}$	
Gate Current (Note 1)	50 mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	+300°C	
	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/°C	7.7 mW/°C

GENERAL DESCRIPTION

This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.

PIN CONFIGURATION
TO-71

CHIP TOPOGRAPHY
6019

0035 X 0090
0026 X 0070
TYP 2 PLACES
0037 X 0037
0027 X 0027
TYP 2 PLACES
0035 X 0035
0025 X 0025
TYP 2 PLACES

ORDERING INFORMATION*

TO-71	WAFER	DICE
IMF6485	IMF6485/W	IMF6485/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200	pA	$V_{GS} = -30\text{V}, V_{DS} = 0.$
		$T_A = 150^\circ\text{C}$	-200	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = -1\mu\text{A}, V_{DS} = 0$
V_p	Gate-Source Pinch-Off Voltage	-0.7	-4.0		$V_{DS} = 20\text{V}, I_D = 1\text{nA}$
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	$V_{DS} = 20\text{V}, V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	μmho	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{KHz}$
g_{oss}	Common-Source Output Conductance		10		$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{KHz}$
C_{iss}	Common-Source Input Capacitance		20	pF	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{MHz}$
I_G	Gate Current		-100	pA	$V_{GS} = 20\text{V}, I_D = 200\mu\text{A}$
		$T_A = 150^\circ\text{C}$	-100	nA	
V_{GS}	Gate-Source Voltage	0.2	-3.8	V	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$
g_{fs}	Common-Source Forward Transconductance	500	1500	μmho	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{KHz}$
g_{os}	Common-Source Output Conductance		1		$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$
e_n	Equivalent Input Noise Voltage		15	$\text{nV}/\sqrt{\text{Hz}}$	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 10\text{Hz}$
			10		$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{KHz}$

NOTES:

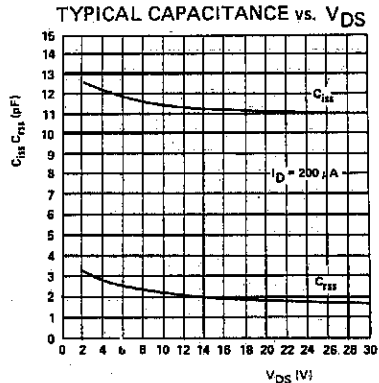
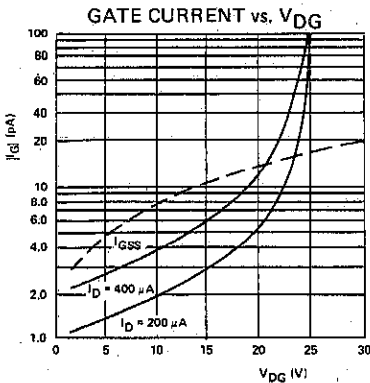
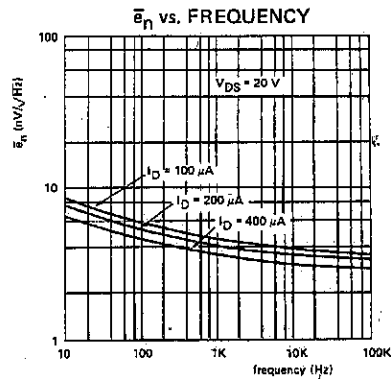
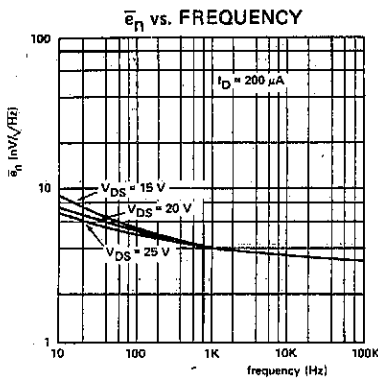
1. Per transistor.
2. Pulse test required; pulse width = 2 ms.

MATCHING CHARACTERISTICS (@ 25° C unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1		$V_{DS} = 20 \text{ V}, V_{GS} = 0$ (Note 2)
$ I_{G1} - I_{G2} $	Differential Gate Current		10	nA	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$ $T_A = +125^\circ \text{C}$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1		$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A},$ $f = 1 \text{ KHz}$ (Note 2)
$ g_{os1} - g_{os2} $	Differential Output Conductance		0.1	μmho	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A},$ $f = 1 \text{ KHz}$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		25	mV	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift		40	$\mu\text{V}/^\circ\text{C}$	$V_{CG} = 20 \text{ V}, I_D = 200 \mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	90		dB	$V_{DD} = 10$ to $20 \text{ V},$ $I_D = 200 \mu\text{A}$ (Note 3)

- NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
 2. Pulse duration of 2 ms used during test.
 3. $\text{CMRR} = 20 \log_{10} \Delta V_{DD} / \Delta |V_{GS1} - V_{GS2}|$, ($\Delta V_{DD} = 10 \text{ V}$)

TYPICAL OPERATING CHARACTERISTICS



1

Diode Protected P-Channel Enhancement Mode MOSFET

FEATURES

- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate from Damage due to Overvoltage

1

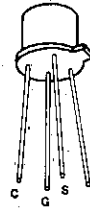
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

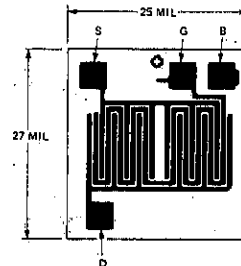
Drain-Source or Drain-Gate Voltage	40V
Drain Current	50 mA
Gate Forward Current	10 μA
Gate Reverse Current	1 mA
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	375 mW
Derate above 25°C	3.0 mW/ $^\circ\text{C}$

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY 1507



ORDERING INFORMATION*

TO-72	WAFER	DICE
3N161	3N161/W	3N161/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{GSSF} Forward Gate-Terminal Current		-100		pA	$V_{GS} = -25\text{ V}, V_{DS} = 0$
	$T_A = +100^\circ\text{C}$		-1	nA	
BV_{GSS} Forward Gate-Source Break-down Voltage	-25			V	$I_G = 0.1\text{ mA}, V_{DS} = 0$
I_{DSS} Zero-Gate-Voltage Drain Current			-10	nA	$V_{DS} = -15\text{ V}, V_{GS} = 0$
			-10	μA	$V_{DS} = -25\text{ V}, V_{GS} = 0$
$V_{GS(th)}$ Gate-Source Threshold Voltage	-1.5		-5	V	$V_{DS} = -15\text{ V}, I_D = -10\text{ }\mu\text{A}$
V_{GS} Gate-Source Voltage	-4.5		-8		$V_{DS} = -15\text{ V}, I_D = -8\text{ mA}$
$I_{D(on)}$ On-State Drain Current	-40		-120	mA	$V_{DS} = -15\text{ V}, V_{GS} = -15\text{ V}$
$ y_{fs} $ Small-Signal Common-Source Forward Transfer Admittance	3500		6500	μmho	$V_{DS} = -15\text{ V}, I_D = -8\text{ mA}$
$ y_{os} $ Small-Signal Common-Source Output Admittance			250		
C_{iss} Common-Source Short-Circuit Input Capacitance			10	pF	$f = 1\text{ MHz}$
C_{rss} Common-Source Short-Circuit Reverse Transfer Capacitance			4		

3N163, 3N164 P-Channel Enhancement Mode MOS FET

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

ABSOLUTE MAXIMUM RATINGS (Note 1)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage

3N163 40V

3N164 30V

Static Gate-Source Voltage

3N163 $\pm 40\text{V}$

3N164 $\pm 30\text{V}$

Transient Gate-Source Voltage (Note 2) $\pm 125\text{V}$

Drain Current 50 mA

Storage Temperature -65°C to $+200^\circ\text{C}$

Operating Temperature -55°C to $+150^\circ\text{C}$

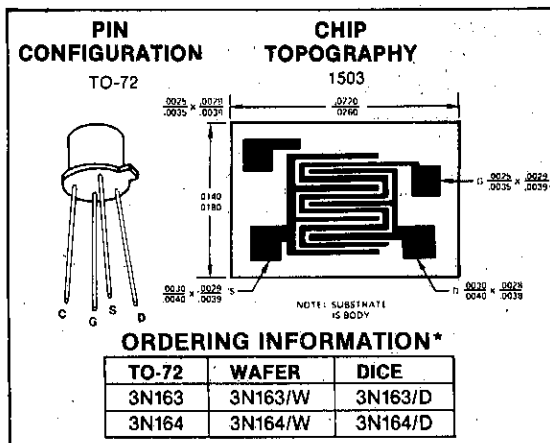
Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$

Power Dissipation 375 mW

Derate above $+25^\circ\text{C}$ $3.0 \text{ mW}/^\circ\text{C}$

NOTES:

1. See handling precautions on 3N170 data sheet.
2. Devices must not be tested at $\pm 125\text{V}$ more than once, nor for longer than 300 ms.



1

*When ordering wafer/dice refer to Appendix B-23.

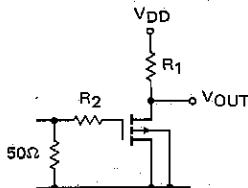
ELECTRICAL CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted)

Symbol	Parameter	3N163		3N164		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSSR}	Gate Reverse Leakage Current		10		10	pA	$V_{GS} = -40\text{V}$ (3N163) $V_{GS} = -30\text{V}$ (3N164)
I_{GSSF}	Gate Forward Current		-10		-10		
		$T_A = +125^\circ\text{C}$					
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	$I_D = -10 \mu\text{A}$, $V_{GS} = 0$
BV_{SDS}	Source Drain Breakdown Voltage	-40		-30			$I_S = -10 \mu\text{A}$, $V_{GD} = 0$, $V_{DS} = 0$
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	$V_{DS} = V_{GS}$, $I_D = -10 \mu\text{A}$
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		$V_{DS} = -15\text{V}$, $I_D = -10 \mu\text{A}$
V_{GS}	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	pA	$V_{DS} = -15\text{V}$, $I_D = -0.5 \text{ mA}$
I_{DSS}	Zero Gate Voltage Drain Current	200		400			$V_{DS} = -15\text{V}$, $V_{GS} = 0$
I_{SDS}	Source Drain Current	400		800		ohms	$V_{GS} = 15\text{V}$, $V_{DS} = V_{DS} = 0$
$r_{DS(on)}$	Drain-Source on Resistance		250		300		$V_{GS} = -20\text{V}$, $I_D = -100 \mu\text{A}$
$I_{D(on)}$	On Drain Current	-5.0	-30.0	-3.0	-30.0	mA	$V_{DS} = -15\text{V}$, $V_{GS} = -10\text{V}$
g_{fs}	Forward Transconductance	2000	4000	1000	4000		$V_{DS} = -15\text{V}$, $I_D = -10 \text{ mA}$, $f = 1 \text{ KHz}$
g_{os}	Output Admittance		250		250	pF	$V_{DS} = -15\text{V}$, $I_D = -10 \text{ mA}$, $f = 1 \text{ MHz}$
C_{iss}	Input Capacitance - Output Shorted		2.5		2.5		
C_{rss}	Reverse Transfer Capacitance		0.7		0.7		
C_{oss}	Output Capacitance Input Shorted		3.0		3.0		

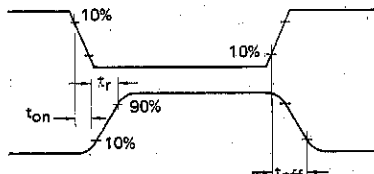
SWITCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$)

t_{on}	Turn-On Delay Time		12		12	ns	$V_{DD} = -15\text{V}$ $I_{D(on)} = -10 \text{ mA}$ $R_C = R_L = 1.4 \text{ k}\Omega$
t_r	Rise Time		24		24		
t_{off}	Turn-Off Time		50		50		

SWITCHING TIME CIRCUIT



SWITCHING WAVEFORM





3N165, 3N166 Dual P-Channel Enhancement Mode MOS FET

FEATURES

- Very High Impedance
- High Gate Breakdown
- Low Capacitance

1

ABSOLUTE MAXIMUM RATINGS (Note 1)

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain-Source or Drain-Gate Voltage (Note 2)

3N165 40V

3N166 30V

Transient Gate-Source Voltage (Note 3) ± 125

Gate-Gate Voltage $\pm 80\text{V}$

Drain Current (Note 2) 50 mA

Storage Temperature -65°C to $+200^\circ\text{C}$

Operating Temperature -55°C to $+150^\circ\text{C}$

Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$

Power Dissipation

One Side 300 mW

Both Sides 525 mW

Total Derating above 25°C 4.2 mW/ $^\circ\text{C}$

PIN CONFIGURATION
TO-99

DEVICE SCHEMATIC

CHIP TOPOGRAPHY

NOTE: SURSTRATE IS BODY.

ORDERING INFORMATION*

TO-99	WAFER	DICE
3N165	3N165/W	3N165/D
3N166	3N166/W	3N166/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C and $V_{GS} = 0$ unless notes)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current		10	pA	$V_{GS} = 40\text{V}$
I_{GSSF}	Gate Forward Leakage Current		-10		$V_{GS} = -40\text{V}$
	$T_A = +125^\circ\text{C}$		-25		
I_{DSS}	Drain to Source Leakage Current		-200	mA	$V_{DS} = -20\text{V}$
I_{SDS}	Source to Drain Leakage Current		-400		$V_{SD} = -20, V_{DB} = 0$
$I_{D(on)}$	On Drain Current	-5	-30		$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	V	$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5		$V_{DS} = V_{GS}, I_D = -10\mu\text{A}$
$r_{DS(on)}$	Drain Source ON Resistance		300	ohms	$V_{GS} = -20\text{V}, I_D = -100\mu\text{A}$
g_{fs}	Forward Transconductance	1500	3000	μmhos	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 1\text{kHz}$
g_{os}	Output Admittance		300	pF	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 1\text{MHz}$
C_{iss}	Input Capacitance		3.0		
C_{rss}	Reverse Transfer Capacitance		0.7		
C_{oss}	Output Capacitance		3.0	μmhos	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 100\text{MHz}$
$R_E(Y_{fs})$	Common Source Forward Transconductance	1200			

MATCHING CHARACTERISTICS 3N165

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		$V_{DS} = -15\text{V}, I_D = -1500\mu\text{A}, f = 1\text{KHz}$
V_{GS1-2}	Gate-Source Threshold Voltage Differential		100	mV	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$
ΔV_{GS1-2}	Gate Source Threshold Voltage Differential Change with Temperature		100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+25^\circ\text{C}$
ΔT			100		

Note 1: See handling precautions on 3N170 data sheet.

Note 2: Per transistor.

Note 3: Devices must not be tested at $\pm 125\text{V}$ more than once, nor for longer than 300 ms.

3N170, 3N171 N-Channel Enhancement Mode MOS FET

FEATURES

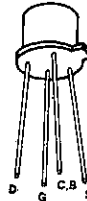
- Low Switching Voltages
- Fast Switching Times
- Low Drain-Source Resistance
- Low Reverse Transfer Capacitance

ABSOLUTE MAXIMUM RATINGS

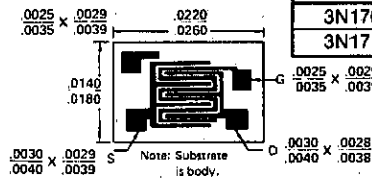
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	$\pm 35\text{V}$
Drain-Source Voltage	25V
Gate-Source Voltage	$\pm 35\text{V}$
Drain Current	30 mA
Storage Temperature	
Range	-65°C to $+200^\circ\text{C}$
Operating Temperature	
Range	-55°C to $+150^\circ\text{C}$
Lead Temperature	
(Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

PIN CONFIGURATION TO-72



CHIP TOPOGRAPHY 1003



HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.

ORDERING INFORMATION*

TO-72	WAFER	DICE
3N170	3N170/W	3N170/D
3N171	3N170/W	3N170/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS		
BV_{DSS}	25		V	$I_D = 10\ \mu\text{A}$, $V_{GS} = 0$		
I_{GSS}		10	pA	$V_{GS} = -35\ \text{V}$, $V_{DS} = 0$		
		$T_A = 125^\circ\text{C}$			100	
I_{DSS}	Zero-Gate-Voltage Drain Current	10	nA	$V_{DS} = 10\ \text{V}$, $V_{GS} = 0$		
		$T_A = 125^\circ\text{C}$			1.0	
$V_{GS(th)}$	Gate-Source Threshold Voltage	3N170	1.0	2.0	V	$V_{DS} = 10\ \text{V}$, $I_D = 10\ \mu\text{A}$
		3N171	1.5			
$I_{D(on)}$	"ON" Drain Current	10		mA	$V_{GS} = 10\ \text{V}$, $V_{DS} = 10\ \text{V}$	
$V_{DS(on)}$	Drain-Source "ON" Voltage		2.0	V	$I_D = 10\ \text{mA}$, $V_{GS} = 10\ \text{V}$	
$r_{ds(on)}$	Drain-Source ON Resistance		200	Ω	$V_{GS} = 10\ \text{V}$, $I_D = 0$, $f = 1.0\ \text{kHz}$	
$ Y_{fs} $	Forward Transfer Admittance	1000		μmhos	$V_{DS} = 10\ \text{V}$, $I_D = 2.0\ \text{mA}$, $f = 1.0\ \text{kHz}$	
C_{rss}	Reverse Transfer Capacitance		1.3	pF	$V_{DS} = 0$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$	
C_{iss}	Input Capacitance		5.0		$V_{DS} = 10\ \text{V}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$	
$C_{d(sub)}$	Drain-Substrate Capacitance		5.0		$V_{D(SUB)} = 10\ \text{V}$, $f = 1.0\ \text{MHz}$	
$t_{d(on)}$	Turn-On Delay Time		3.0	ns	$V_{DD} = 10\ \text{V}$, $I_{D(on)} = 10\ \text{mA}$, $V_{GS(on)} = 10\ \text{V}$, $V_{GS(off)} = 0$, $R_G = 50\ \Omega$	
t_r	Rise Time		10			
$t_{d(off)}$	Turn-Off Delay Time		3.0			
t_f	Fall Time		15			



3N172, 3N173 Diode Protected P-Channel Enhancement Mode MOS FET

FEATURES

- High Input Impedance
- Diode Protected Gate

1

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage	
3N172	40V
3N173	30V
Drain Current	50 mA
Gate Forward Current	10 μA
Gate Reverse Current	1 mA
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	375 mW
Derate above 25°C	3.0 mW/ $^\circ\text{C}$

PIN CONFIGURATION
TO-72

DEVICE SCHEMATIC

CHIP TOPOGRAPHY 1503Z

NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION*

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted)

PARAMETER		3N172		3N173		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSSR}	Gate Reverse Current		-200		-500	pA	$V_{GS} = -20\text{V}$
		$T_A = +125^\circ\text{C}$	-0.5		-1.0		
BV_{GSS}	Gate Breakdown Voltage	-40	-125	-30	-125	V	$I_D = -10 \mu\text{A}$
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30			$I_D = -10 \mu\text{A}$
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			$I_S = -10 \mu\text{A}, V_{GS} = 0$
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		$V_{DS} = V_{GS}, I_D = -10 \mu\text{A}$
V_{GS}	Gate Source Voltage	-2.0	-5.0	-2.0	-5.0	nA	$V_{DS} = -15\text{V}, I_D = -10 \mu\text{A}$
		-3.0	-6.5	-2.5	-6.5		$V_{DS} = -15\text{V}, I_D = -500 \mu\text{A}$
I_{DSS}	Zero Gate Voltage Drain Current		-0.4		-10		$V_{DS} = -15\text{V}, V_{GS} = 0$
I_{SDS}	Zero Gate Voltage Source Current		-0.4		-10		$V_{SD} = -15\text{V}, V_{DB} = 0, V_{GD} = 0$
$r_{DS(on)}$	Drain-Source On Resistance		250		350	ohms	$V_{GS} = -20\text{V}, I_D = -100 \mu\text{A}$
$I_{D(on)}$	On Drain Current	-5.0	-30	-5.0	-30	mA	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$

3N188-3N191 Dual P-Channel Enhancement Mode MOSFET

FEATURES

- Very High Input Impedance
- High Gate Breakdown 3N190-3N191
- Zener Protected gate 3N188-3N189
- Low Capacitance

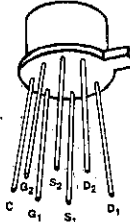
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage (Note 1)	
3N188, 3N189	40V
3N190, 3N191	30V
Transient Gate-Source Voltage (Notes 1 and 2)	$\pm 125\text{V}$
Gate-Gate Voltage	$\pm 80\text{V}$
Drain Current (Note 1)	50 mA
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	
One Side	300 mW
Both Sides	525 mW
Total Derating above 25°C	4.2 mW/ $^\circ\text{C}$

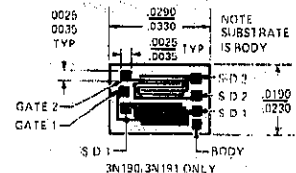
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

2506



NOTE: Body is connected to case.

ORDERING INFORMATION*

	TO-99	WAFER	DICE
3N188	—	—	—
3N189	—	—	—
3N190	3N190/W	—	3N190/D
3N191	3N191/W	—	3N191/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C and $V_{BS} = 0$ unless otherwise noted)

PARAMETER	3N188 3N189		3N190 3N191		UNITS	TEST CONDITIONS
	MIN	MAX	MIN	MAX		
I_{GSSR} Gate Reverse Current				10	μA	$V_{GS} = 40\text{V}$
I_{GSSF} Gate Forward Current		-200		-10	μA	$V_{GS} = -40\text{V}$
BV_{DSS} Drain-Source Breakdown Voltage	-40	-200	-40	-25	V	$I_D = -10\mu\text{A}$
BV_{SDS} Source-Drain Breakdown Voltage	-40		-40		V	$I_S = -10\mu\text{A}, V_{BD} = 0$
$V_{GS(th)}$ Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$
V_{GS} Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	V	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$
I_{DSS} Zero Gate Voltage Drain Current		-200		-200	μA	$V_{DS} = -15\text{V}$
I_{SDS} Source Drain Current		-400		-400	μA	$V_{SD} = -15\text{V}, V_{DB} = 0$
$r_{DS(on)}$ Drain-Source on Resistance		300		300	ohms	$V_{DS} = -20\text{V}, I_D = -100\mu\text{A}$
$I_{D(on)}$ On Drain Current	-5.0	-30.0	-5.0	-30.0	mA	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$
g_{fs} Forward Transconductance (Note 3)	1500	4000	1500	4000	μmhos	
Y_{os} Output Admittance		300		300	μmhos	
C_{iss} Input Capacitance Output Shorted		4.5		4.5	pF	$V_{DS} = -15\text{V}, I_D = -5\text{mA}$
C_{rss} Reverse Transfer Capacitance		1.5		1.0	pF	
C_{oss} Output Capacitance Input Shorted		3.0		3.0	pF	$f = 1\text{MHz}$

SWITCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted)

Parameter	Description	MIN	MAX	UNITS	TEST CONDITIONS
$t_{d(on)}$	Turn On Delay Time		15	ns	$V_{DD} = -15\text{V}, I_D = -5\text{mA}$
t_r	Rise Time		30	ns	$R_G = R_L = 1.4\text{k}\Omega$
t_{off}	Turn Off Time		50	ns	

MATCHING CHARACTERISTICS (@ 25°C and $V_{BS} = 0$ unless noted) 3N188 and 3N190

Parameter	Description	MIN	MAX	UNITS	TEST CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.85	1.0		$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}, f = 1\text{kHz}$
V_{GS1-2}	Gate Source Threshold Voltage Differential		100	mV	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)		100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$ $T = -85^\circ\text{C}$ to $+25^\circ\text{C}$
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)		100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$ $T = +25^\circ\text{C}$ to $+125^\circ\text{C}$

NOTES:

1. Per transistor
2. Approximately doubles for every 10°C increase in T_A .

3. Pulse test duration = 300 μsec ; duty cycle $\leq 3\%$.
4. Measured at end points, T_A and T_B .

FEATURES

- $I_R = 0.1 \text{ pA}$ (typical)
- $BV_R > 30 \text{ V}$
- $C_{RSS} = 0.75 \text{ pF}$ (typical)

1

GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Diode Reverse Voltage	30V
Diode to Diode Voltage	$\pm 50\text{V}$
Forward Current	20 mA
Reverse Current	100 μA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

PIN CONFIGURATIONS
TO-71
TO-78

*These leads must not be tied together nor connected to the circuit in any way.

CHIP TOPOGRAPHY

ORDERING INFORMATION*

TO78	TO71	WAFER	CHIP
ID100	ID101	ID100/W	ID100/D

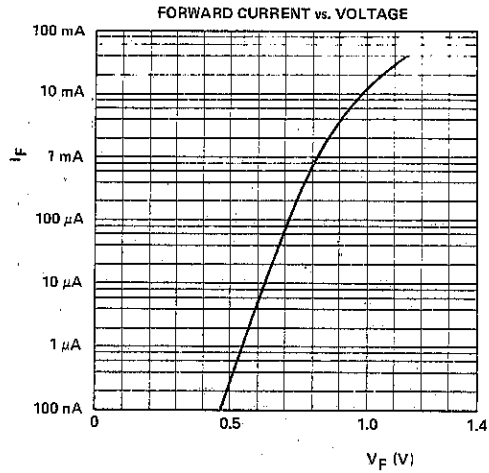
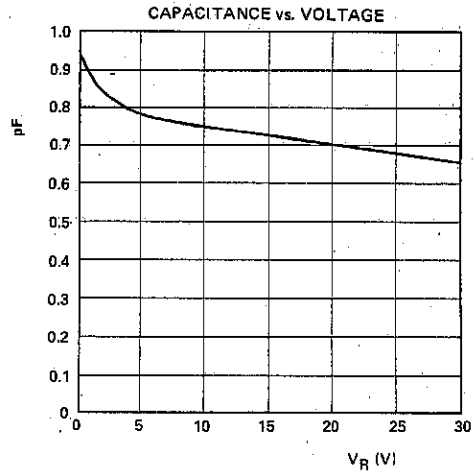
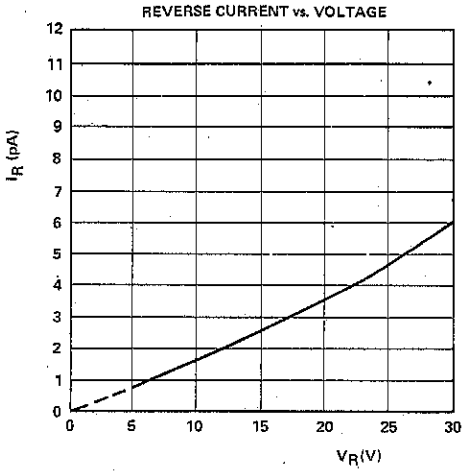
*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER	ID100, ID101			UNITS	TEST CONDITIONS
	MIN.	TYP.	MAX.		
V_F	Forward Voltage Drop			V	$I_F = 10 \text{ mA}$
BV_R	Reverse Breakdown Voltage			V	$I_R = 1 \mu\text{A}$
I_R	Reverse Leakage Current			μA	$V_R = 1 \text{ V}$
		0.1	10		
$ I_{R1} - I_{R2} $	Differential Leakage Current			μA	$V_R = 10 \text{ V}$
		2.0	3		
C_{RSS}	Total Reverse Capacitance			pF	$V_R = 10 \text{ V}, f = 1 \text{ MHz}$

TYPICAL CHARACTERISTICS OF ID100/ID101

1



1

FEATURES

- Interfaces Directly w/T²L Logic Elements
- $r_{DS(on)} < 75\Omega$ for 5V Logic Drive
- $I_{D(off)} < 100 \text{ pA}$

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with T²L logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of $\pm 15 \text{ V}$ can be switched. The FET is OFF for hi level inputs ($+5 \text{ V}$ or $+15 \text{ V}$) and ON for low level inputs ($< 0.5 \text{ V}$ for IT100; $< 1.5 \text{ V}$ for IT101).

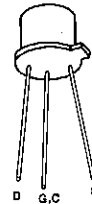
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ \text{ C}$ unless otherwise noted)

Gate-Source Voltage	35V
Gate-Drain Voltage	35V
Gate Current	50mA
Storage Temperature Range	-65° C to $+200^\circ \text{ C}$
Operating Temperature Range	-55° C to $+150^\circ \text{ C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ \text{ C}$
Power Dissipation	300 mW
Derate above 25° C	1.7 mW/ $^\circ \text{ C}$

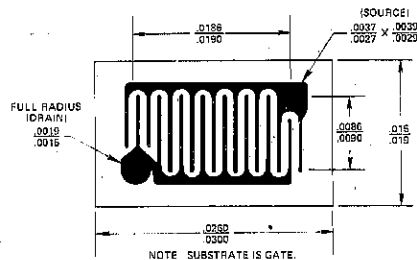
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5514



ORDERING INFORMATION*

TO-18	WAFER	DICE
IT100	IT100/W	IT100/D
IT101	IT101/W	IT101/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted)

PARAMETER		IT100		IT101		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{DSS}	Drain Current	-10		-20		mA	$V_{GS} = 0, V_{DS} = -15 \text{ V}$
V_p	Pinch Off Voltage	2	4.5	4	10	V	$I_D = 1 \text{ nA}, V_{DS} = -15 \text{ V}$
BV_{GSS}	Gate-Source Breakdown Voltage	35		35			$I_G = 1 \mu\text{A}, V_{DS} = 0$
I_{GSSR}	Gate Reverse Current		200		200	pA	$V_{GS} = 20 \text{ V}, V_{DS} = 0$
g_{fs}	Transconductance	8		8		mmho	$V_{GS} = 0, V_{DS} = -15 \text{ V}$
g_{os}	Output Conductance		1		1		
$I_{D(off)}$	Drain (OFF) Leakage		-100		-100	pA	$V_{DS} = -10 \text{ V}, V_{GS} = 15 \text{ V}$
$r_{DS(on)}$	Drain-Source "ON" Resistance		75		60	Ω	$V_{GS} = 0, V_{DS} = -0.1 \text{ V}$
C_{iss}	Input Capacitance		35		35	pF	$V_{DG} = -20 \text{ V}, V_{GS} = 0$
C_{rss}	Reverse Transfer Capacitance		12		12		$V_{DG} = -10 \text{ V}, I_S = 0$

IT120-IT122 Monolithic Dual NPN Transistor

FEATURES

- High h_{FE} at Low Current
- Low Output Capacitance
- Good Matching
- Tight V_{BE} Tracking

ABSOLUTE MAXIMUM RATINGS

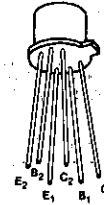
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	50 mA
Collector-Collector Voltage	60V
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

Power	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Dissipation ...	400 mW	750 mW	300 mW	500 mW
Derate Above				
25°C	1.7 mW/ $^\circ\text{C}$	2.9 mW/ $^\circ\text{C}$	2.3 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$

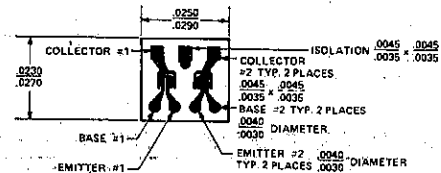
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4003



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT120	IT120-TO71	IT120/W	IT120/D
IT121	IT121-TO71	IT121/W	IT121/D
IT122	IT122-TO71	IT122/W	IT122/D

ELECTRICAL CHARACTERISTICS

(25°C unless otherwise noted)

*When ordering wafer/dice refer to Appendix B-23.

PARAMETER		IT120A		IT120		IT121		IT122		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
		225		225		100		100			$I_C = 1.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$
		75		75		30		30			$T_A = -55^\circ\text{C}$
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$V_{CE(SAT)}$	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	$I_C = 0.5 \text{ mA}, I_B = 0.05 \text{ mA}$
I_{CBO}	Collector Cutoff Current	1.0		1.0		1.0		1.0		nA	$I_E = 0, V_{CB} = 45 \text{ V}$
		10		10		10		10		μA	$T_A = +150^\circ\text{C}$
I_{EBO}	Emitter Cutoff Current	1.0		1.0		1.0		1.0		nA	$I_C = 0, V_{EB} = 5.0 \text{ V}$
C_{ob0}	Output Capacitance	2.0		2.0		2.0		2.0		pF	$I_E = 0, V_{CB} = 5.0 \text{ V}$
C_{te}	Emitter Transition Capacitance	2.5		2.5		2.5		2.5		pF	$I_C = 0, V_{EB} = 0.5 \text{ V}$
$C_{C1, C2}$	Collector to Collector Capacitance	4.0		4.0		4.0		4.0		pF	$f = 1 \text{ MHz}$
$I_{C1, C2}$	Collector to Collector Leakage Current	10		10		10		10		nA	$V_{CC} = 0$
$V_{CE0(SUST)}$	Collector to Emitter Sustaining Voltage	45		45		45		45		V	$V_{CC} = \pm 60 \text{ V}$
GBW	Current Gain Bandwidth Product	10		10		7		7		MHz	$I_C = 10 \mu\text{A}, V_{CE} = 5 \text{ V}$
		220		220		180		180		MHz	$I_C = 1 \text{ mA}, V_{CE} = 5 \text{ V}$
$ V_{BE1} - V_{BE2} $	Base-Emitter Voltage Differential		1		2		3		5	mV	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$ I_{B1} - I_{B2} $	Base Current Differential		2.5		5		25		25	nA	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$\Delta(V_{BE1} - V_{BE2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu\text{V}/^\circ\text{C}$	$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA .

IT124 Monolithic Dual Super-Beta NPN Transistor

1

FEATURES

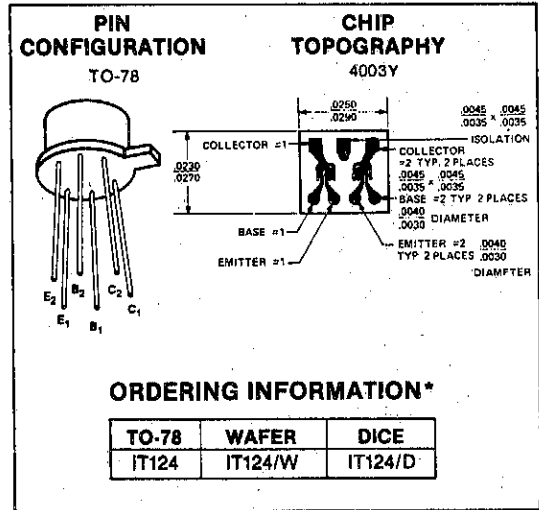
- Very High Gain
- Low Output Capacitance
- Tight V_{BE} Matching
- High GBW

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base Voltage (Note 1)	2V
Collector-Emitter Voltage (Note 1)	2V
Emitter-Base Voltage (Notes 1 and 2)	7V
Collector-Current (Note 1)	10 mA
Collector-Collector Voltage	100V
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

	TO-78	
	ONE	BOTH
	SIDE	SIDES
Power Dissipation	300 mW	500 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$



*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1500			$I_C = 1\mu\text{A}, V_{CE} = 1\text{V}$
		$T_A = -55^\circ\text{C}$	600		
$V_{BE(ON)}$	Emitter-Base "ON" Voltage		0.7	V	$I_C = 1\text{mA}, I_B = 0.1\text{mA}$
$V_{CE(SAT)}$	Collector Saturation Voltage		0.5		
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0, V_{CB} = 1\text{V}$
		$T_A = +150^\circ\text{C}$		100	
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0, V_{EB} = 5\text{V}$
C_{ob0}	Output Capacitance		0.8	pF	$I_E = 0, V_{CB} = 1\text{V}$
C_{te}	Emitter Transition Capacitance		1.0		$I_C = 0, V_{EB} = 0.5\text{V}$
C_{C1C2}	Collector to Collector Capacitance		0.8		$V_{CC} = 0$
I_{C1C2}	Collector to Collector Leakage Current		250	pA	$V_{CC} = \pm 50\text{V}$
GBW	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$
		100			$I_C = 100\mu\text{A}, V_{CE} = 1\text{V}$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu\text{A}, V_{CE} = 3\text{V},$ $f = 1\text{KHz}, R_G = 10\text{Kohms},$ $BW = 200\text{Hz}$
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu\text{A}, I_E = 0$
BV_{EBO} (Note 2)	Emitter-Base Breakdown Voltage	7			$I_E = 10\mu\text{A}, I_C = 0$
$V_{CE0(SUST)}$	Collector-Emitter Sustaining Voltage	2			$I_C = 1\text{mA}, I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TYP	MAX	UNITS	CONDITIONS
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential	2	5	mV	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$
$\Delta(V_{BE1} - V_{BE2})/\Delta T$	Base Emitter Voltage Differential Change with Temperature	5	15	$\mu\text{V}/^\circ\text{C}$	$I_C = 10\mu\text{A}, V_{CE} = 1\text{V}$ $T = -55^\circ\text{C}$ to $+125^\circ\text{C}$
$ I_{B1} - I_{B2} $	Base Current Differential		.6	nA	$T_C = 10\mu\text{A}, V_{CE} = 1\text{V}$

NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed $10\mu\text{A}$.

IT126-IT129 Monolithic Dual NPN Transistor

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectric Isolated Matched Pairs for Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Collector-Base Voltage (Note 1)

IT126, IT127	60V
IT128	55V
IT129	45V

Collector-Emitter Voltage (Note 1)

IT126, IT127	60V
IT128	55V
IT129	45V

Emitter-Base Voltage (Notes 1 and 2)

	7.0V
--	------

Collector Current (Note 1)

	100 mA
--	--------

Collector-Collector Voltage

	70V
--	-----

Storage Temperature Range

	-65°C to $+200^\circ\text{C}$
--	---

Operating Temperature Range

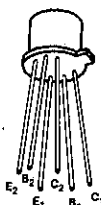
	-55°C to $+150^\circ\text{C}$
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Lead Temperature (Soldering, 10 sec.)

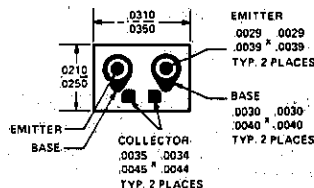
	$+300^\circ\text{C}$
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	TO71		TO78	
	One Side	Both Sides	One Side	Both Sides
Power Dissipation	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Total Dissipation at 25°C	1.7 mW/ $^\circ\text{C}$	2.9 mW/ $^\circ\text{C}$	2.5 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$
Cast Temperature				
Derating Factor				

PIN CONFIGURATION
TO-71 TO-78



CHIP TOPOGRAPHY
4001



ORDERING INFORMATION*

TO78	TO-71	WAFER	DICE
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-TO71	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT128/W	IT128/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	IT126		IT127		IT128		IT129		UNITS	CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE} DC Current Gain		150		150		100		70		$I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$
		200	800	200	800	150	800	100		$I_C = 1.0 \text{ mA}, V_{CE} = 5\text{V}$
		230		230		170		115		$I_C = 10 \text{ mA}, V_{CE} = 5\text{V}$
		100		100		75		50		$I_C = 50 \text{ mA}, V_{CE} = 5\text{V}$
	$T_A = -55^\circ\text{C}$	75		75		60		40		$I_C = 1 \text{ mA}, V_{CE} = 5\text{V}$
$V_{BE(on)}$ Emitter-Base On Voltage		.9		.9		.9		.9	V	$I_C = 10 \text{ mA}, V_{CE} = 5\text{V}$
		1.0		1.0		1.0		1.0		$I_C = 50 \text{ mA}, V_{CE} = 5\text{V}$
$V_{CE(sat)}$ Collector Saturation Voltage		.3		.3		.3		.3		$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$
		1.0		1.0		1.0		1.0		$I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$
I_{CBO} Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	$I_E = 0, V_{CB} = 45\text{V}, 30\text{V}^*$
	$T_A = +150^\circ\text{C}$	0.1		0.1		0.1		0.1*	μA	
I_{EBO} Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5\text{V}$
C_{obo} Output Capacitance		3		3		3		3	pF	$I_E = 0, V_{CB} = 20\text{V}$
$BV_{C_1C_2}$ Collector-to Collector Breakdown Voltage	± 100		± 100		± 100		± 100		V	$I_C = \pm 1 \mu\text{A}$
$V_{CEO(sust)}$ Collector to Emitter Sustaining Voltage	60		60		55		45			$I_C = 1 \text{ mA}, I_B = 0$
BV_{CBO} Collector Base Breakdown Voltage	60		60		55		45			$I_C = 10 \mu\text{A}, I_E = 0$
BV_{EBO} Emitter Base Breakdown Voltage	7		7		7		7			$I_E = 10 \mu\text{A}, I_C = 0$
MATCHING CHARACTERISTICS										
$ V_{BE_1} - V_{BE_2} $ Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 1 \text{ mA}, V_{CE} = 5\text{V}$
$\Delta(V_{BE_1} - V_{BE_2})/\Delta T$ Base Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu\text{V}/^\circ\text{C}$	$I_C = 1 \text{ mA}, V_{CE} = 5\text{V}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
$ I_{B_1} - I_{B_2} $ Base Current Differential		2.5		5		10		20	nA	$I_C = 10 \mu\text{A}, V_{CE} = 5\text{V}$
		.25		.5		1.0		2.0	μA	$I_C = 1 \text{ mA}, V_{CE} = 5\text{V}$

NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA .



IT130-IT132 Monolithic Dual PNP Transistor

FEATURES

- High h_{FE} at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking

ABSOLUTE MAXIMUM RATINGS

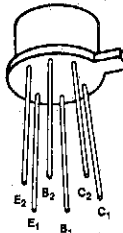
($T_A = 25^\circ\text{C}$ unless otherwise specified)

Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	50 mA
Collector-Collector Voltage	60V
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

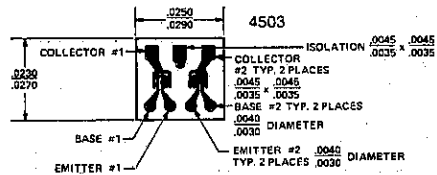
Power Dissipation	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
	400 mW	750 mW	300 mW	500 mW
	2.3 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$	1.7 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$

PIN CONFIGURATIONS

TO-71
TO-78



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER	IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain		200	200	80	80	100	100		$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
			225	225	100	100	100	100		$I_C = 1.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$
			75	75	30	30	30	30		$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7	0.7	0.7	0.7	0.7	0.7	V	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$V_{CE(SAT)}$	Collector Saturation Voltage		0.5	0.5	0.5	0.5	0.5	0.5		$I_C = 0.5 \text{ mA}, I_B = 0.05 \text{ mA}$
I_{CBO}	Collector Cutoff Current		-1.0	-1.0	-1.0	-1.0	-1.0	-1.0	nA	$I_E = 0, V_{CB} = 45 \text{ V}$
			-10	-10	-10	-10	-10	-10	μA	$T_A = +150^\circ\text{C}$
I_{EBO}	Emitter Cutoff Current		-1.0	-1.0	-1.0	-1.0	-1.0	-1.0	nA	$I_C = 0, V_{EB} = 5.0 \text{ V}$
C_{ob}	Output Capacitance		2.0	2.0	2.0	2.0	2.0	2.0	pF	$I_C = 0, V_{CB} = 5.0 \text{ V}$
C_{te}	Emitter Transition Capacitance		2.5	2.5	2.5	2.5	2.5	2.5		$I_C = 0, V_{EB} = 0.5 \text{ V}$
C_{C1-C2}	Collector to Collector Capacitance		4.0	4.0	4.0	4.0	4.0	4.0		$V_{CC} = 0$
I_{C1-C2}	Collector to Collector Leakage Current		10	10	10	10	10	10	nA	$V_{CC} = \pm 60 \text{ V}$
$V_{CEO(SUST)}$	Collector to Emitter Sustaining Voltage		-45	-45	-45	-45	-45	-45	V	$I_C = 1.0 \text{ mA}, I_B = 0$
			5	5	4	4	4	4	MHz	$I_C = 10 \mu\text{A}, V_{CE} = 5 \text{ V}$
GBW	Current Gain Bandwidth Product		110	110	90	90	90	90		$I_C = 1 \text{ mA}, V_{CE} = 5 \text{ V}$
			110	110	90	90	90	90		$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential		1	1	2	2	3	3	mV	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$ I_{B1} - I_{B2} $	Base Current Differential		2.5	2.5	5	5	25	25	nA	$I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$
$\Delta(V_{BE1} - V_{BE2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature		3	3	5	5	10	10	$\mu\text{V}/^\circ\text{C}$	$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$

NOTES:

1. Per transistor.
2. The reverse base-to-emitter voltage must never exceed 7.0V, and the reverse base-to-emitter current must never exceed 10 μA .

IT136-IT139 Monolithic Dual PNP Transistor

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base Voltage (Note 1)	
IT136, IT137	60V
IT138	55V
IT139	45V
Collector-Emitter Voltage (Note 1)	
IT136, IT137	60V
IT138	55V
IT139	45V
Emitter-Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	100 mA
Collector-Collector Voltage	70V
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10-sec.)	$+300^\circ\text{C}$

TO78

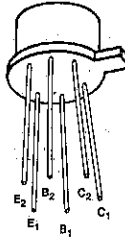
	ONE SIDE	BOTH SIDES
Power Dissipation	0.4 Watt	0.75 Watt
Derate above 25°C	2.3 mW/ $^\circ\text{C}$	4.3 mW/ $^\circ\text{C}$

TO71

	ONE SIDE	BOTH SIDES
Power Dissipation	0.3 Watt	0.5 Watt
Derate above 25°C	1.7 mW/ $^\circ\text{C}$	2.9 mW/ $^\circ\text{C}$

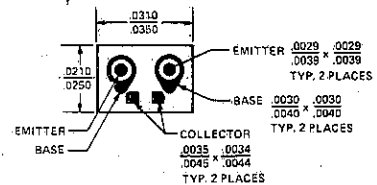
PIN CONFIGURATION

TO-71
TO-78



4501

CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-78	TO-71	WAFER	DICE
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

*When ordering wafer/dice refer to Appendix B-23.

1

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

1

PARAMETER		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h _{FE}	DC Current Gain	150		150		100		70			I _C = 10 μA, V _{CE} = 5V
		150	800	150	800	100	800	70	800		I _C = 1.0 mA, V _{CE} = 5V
		125		125		80		50			I _C = 10 mA, V _{CE} = 5V
		65		60		40		25			I _C = 50 mA, V _{CE} = 5V
		75		75		60		40			I _C = 1 mA, V _{CE} = 5V T _A = 55°C
V _{BE(on)}	Emitter - Base On Voltage		.9		.9		.9		.9	V	I _C = 1 mA, V _{CE} = 5V
V _{CE(sat)}	Collector Saturation Voltage		1.0		1.0		1.0		1.0		I _C = 50 mA, V _{CE} = 5V
			.3		.3		.3		.3		I _C = 1 mA, I _B = .1 mA
			.6		.6		.6		.6		I _C = 10 mA, I _B = 1 mA
I _{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	I _E = 0, V _{CB} = 45V, 30V*
			0.1		0.1		0.1		0.1*	μA	T _A = +150°C
I _{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	I _C = 0, V _{EB} = 5V
C _{obo}	Output Capacitance		3		3		3		3	pF	I _E = 0, V _{CB} = 20V, f = 1 MHz
PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
BV _{C₁C₂}	Collector to Collector Breakdown Voltage	± 100		± 100		± 100		± 100		V	I _C = ±1 μA
V _{CEO(sust)}	Collector to Emitter Sustaining Voltage	60		60		55		45			I _C = 1 mA, I _B = 0
BV _{CB0}	Collector Base Breakdown Voltage	60		60		55		45			I _C = 10 μA, I _E = 0
BV _{EBO}	Emitter Base Breakdown Voltage	7		7		7		7			I _E = 10 μA, I _C = 0
PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V _{BE₁} - V _{BE₂}	Base Emitter Voltage Differential		1		2		3		5	mV	I _C = 1 mA, V _{CE} = 5V
Δ V _{BE₁} - V _{BE₂} ΔT	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	I _C = 1 mA, V _{CE} = 5V T _A = -55°C to +125°C
I _{B₁} - I _{B₂}	Base Current Differential		2.5		5		10		20	nA	I _C = 10 μA, V _{CE} = 5V
			.25		.5		1.0		2.0	μA	I _C = 1 mA, V _{CE} = 5V

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA

IT500-IT505 Monolithic Dual Cascode N-Channel JFET

FEATURES

- CMRR > 120 dB
- $I_G < 5\text{pA}$ @ 50V_{DG}
- $C_{rss} < 0.5\text{pF}$
- $g_{os} > .025\ \mu\text{mhos}$

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

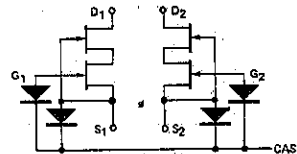
Drain-Source and Drain-Gate	
Voltages (Note 1)	60V
Drain Current (Note 1)	50 mA
Gate-Gate Voltage	$\pm 60\text{V}$
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$

	ONE SIDE	BOTH SIDES
Power Dissipation	250 mW	500 mW
Derate above 25°C	3.8 mW/ $^\circ\text{C}$	7.7 mW/ $^\circ\text{C}$

GENERAL DESCRIPTION

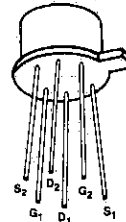
A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common mode rejection ratio.

1

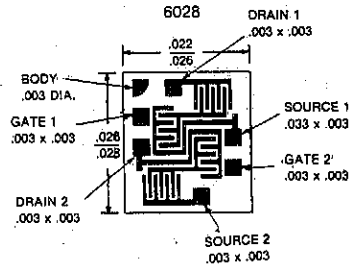


PIN CONFIGURATION

TO-71
low profile



CHIP TOPOGRAPHY (Note 2)



ORDERING INFORMATION*

TO-78	WAFER	DICE
IT500	IT500/W	IT500/D
IT501	IT501/W	IT501/D
IT502	IT502/W	IT502/D
IT503	IT503/W	IT503/D
IT504	IT504/W	IT504/D
IT505	IT505/W	IT505/D

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

Symbol	Characteristics	Min	Max	Unit	Test Conditions
I _{GSSR}	Gate Reverse Current		-100	pA	V _{GS} = -20V, V _{DS} = 0
		T _A = 125°C	-5	nA	
BV _{GSS}	Gate-Source Breakdown Voltage	-60		V	I _G = -1 μA, V _{DS} = 0
V _{GS(off)}	Gate-Source Cutoff Voltage	-0.7	-4		V _{DS} = 20V, I _D = 1 nA
V _{GS}	Gate-Source Voltage	-0.2	-3.8	pA	V _{DG} = 50V, I _D = 200 μA
I _G	Gate Operating Current		-5		
		T _A = 125°C	-5	nA	
I _{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V _{DS} = 20V, V _{GS} = 0
g _{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V _{DS} = 20V, V _{GS} = 0
g _{fs}	Common-Source Forward Transconductance (Note 1)	700	1600		V _{DG} = 20V, I _D = 200 μA
g _{os}	Common-Source Output Conductance		1		V _{DS} = 20V, V _{GS} = 0
g _{os}	Common-Source Output Conductance		0.025		V _{DS} = 20V, I _D = 200 μA
C _{g192}	Gate to Gate Capacitance		3.5	pF	V _{G1} = V _{G2} = 10V
C _{iss}	Common-Source Input Capacitance		7	pF	V _{DS} = 20V, V _{GS} = 0
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 3)		0.5		
NF	Spot Noise Figure		0.5		
e _n	Equivalent Input Noise Voltage		0.035	μV	f = 100 Hz, R _G = 10 MΩ
			0.010	√Hz	f = 10 Hz
					f = 1 kHz

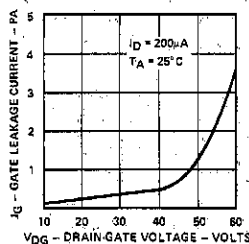
Symbol	Characteristics	IT500		IT501		IT502		IT503		IT504		IT505		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
I _{G1, G2}	Differential Gate Current		5		5		5		5		10		15	nA	V _{DG} = 20V, I _D = 200 μA, +125°C
I _{DSS1}	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1		V _{DS} = 20V, V _{GS} = 0V
I _{DSS2}															f = 1 kHz
g _{fs1} /g _{fs2}	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1		
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage		5		5		10		15		25		50	mV	
ΔV _{GS1} -V _{GS2} / ΔT	Gate-Source Differential Voltage Change with Temp. (Note 2)		5		10		20		40		100		200	μV/°C	V _{DG} = 20V, I _D = 200 μA
C _{MRR} **	Common Mode Rejection Ratio	120		120		120		120		120		120		dB	ΔV _{DD} = 10V, I _D = 200 μA

$$** C_{MRR} = 20 \log_{10} \frac{\Delta V_{DD}}{\Delta (V_{GS1} - V_{GS2})}, \Delta V_{DD} = 10V - 20V$$

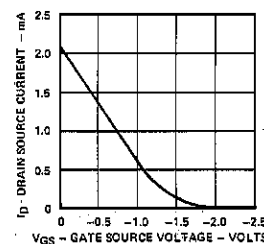
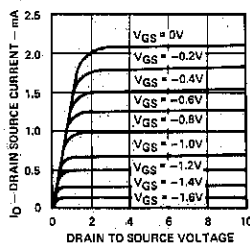
- NOTES: 1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
 2. Measured at end points, T_A and T_B.
 3. With case guarded C_{rss} is typically < 0.15 pF.

TYPICAL PERFORMANCE CURVES

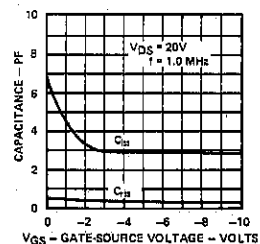
GATE LEAKAGE



OUTPUT CHARACTERISTICS



TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE



A050 Using the IT500 Family to Improve the Input Bias Current of BIFET OPAMPS

1

INTRODUCTION

The LF156 family of BIFET OPAMPS is very popular because of the combination of high slew rate (typically $12V/\mu s$ @ unity gain) and moderate offset voltage (about $2mV$). Input bias current, however, varies directly with input voltage; rising from $30pA$ @ $V_{IN} = -10V$, to $50pA$ @ $V_{IN} = 0V$, and finally to $80pA$ @ $V_{IN} = +10V$. This can be improved markedly by using one of the IT500 series to drive the inputs of the LF156.

The IT500, like the others in its family, is a dual cascoded n-channel JFET pair, featuring a typical input bias current of $<1pA$ with inputs ranging from $-15V$ to $+15V$; actual I_B is guaranteed to be less than $5pA$ @ $V_{DG} = 50V$.

Figure 1 shows an IT500 being used to drive the inputs of an LF156. This greatly reduces the input bias current, and in no way affects the already superior slew rate; the offset voltage is not significantly degraded because of the excellent matching of the IT500.

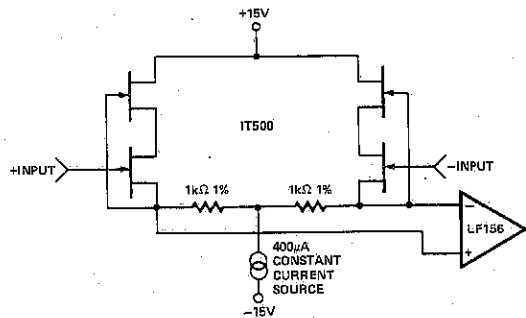


FIGURE 1. INPUT DRIVE CIRCUIT USING IT500

The constant current source can be designed with any transistor pair having a high beta @ $I_C = 400\mu A$. See Figure 2.

An added bonus of the IT500 is its CMRR $> 100dB$, compared to the LF156 CMRR of $85dB$.

This configuration is ideal for electrometer circuits, with good measurement accuracy down to $10pA$ of input current ($< 10\%$ error with $10pA$ of input current). A $10M\Omega$ glass feedback resistor connected between the -INPUT and OPAMP OUTPUT does the trick. Other possible applications include sample and hold amplifiers, instrumentation amplifiers, etc.

Although this application note has dealt solely with the LF156, all present day BIFET OPAMPS exhibit the same I_{BIAS} vs. V_{IN} dependency, and all will benefit from using the IT500 as a preamplifier.

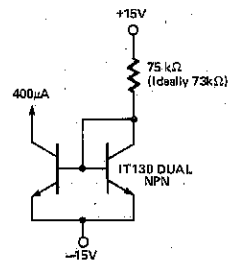


FIGURE 2. CONSTANT CURRENT SOURCE

1

FEATURES

- Specified Matching Characteristics
- High Gain
- Low "ON" Resistance

ABSOLUTE MAXIMUM RATINGS

(25°C Unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-40V
Gate Current	50 mA
Gate-Gate Voltage	±60V
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

	One Side	Both Sides
Power Dissipation	325mW	650mW
Derate above 25°C	2.2mW/°C	3.3mW/°C

PIN CONFIGURATION
TO-71

CHIP TOPOGRAPHY
6033

ORDERING INFORMATION*

TO-71	WAFER	DICE
IT550	IT550/W	IT550/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS (25°C unless otherwise noted)

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT	
I _{GSSR}	Gate-Reverse Current	V _{GS} = -20V, V _{DS} = 0 T _A = 150°C		-100	pA	
				-200	mA	
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-40		V	
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 15V, I _D = 1nA	-0.5	-3		
V _{GS(f)}	Gate-Source Voltage	V _{DS} = 0V, I _G = 2mA		1.0		
I _{DSS}	Saturation Drain Current (Note 1)	V _{DS} = 15V, V _{GS} = 0	5	30	mA	
r _{DS(on)}	Static Drain Source ON Resistance	I _D = 1mA, V _{GS} = 0		100	Ω	
g _{fs}	Common-Source Forward Transconductance (Note 1)	V _{DG} = 15V, I _D = 2mA	f = 1kHz	7500	12,500	μmho
			f = 100MHz	7000		
g _{os}	Common-Source Output Conductance	V _{DG} = 15V, I _D = 2mA	f = 1kHz		45	pF
C _{rss}	Common-Source Reverse Transfer Capacitance		f = 1MHz		3	
C _{iss}	Common-Source Input Capacitance	V _{DG} = 15V, I _D = 2mA			12	dB
NF	Spot Noise Figure		f = 10Hz, R _g = 1M		1.0	
e _n	Equivalent Short Circuit Input Noise Voltage	V _{DG} = 15V, I _D = 2mA	f = 10Hz		50	nV/√Hz

SYMBOL	PARAMETERS	CONDITIONS	IT550		UNIT
			MIN.	MAX.	
I _{DSS1} I _{DSS2}	Saturation Drain Current Ratio (Notes 1 and 2)	V _{DS} = 15V, V _{GS} = 0	0.95	1	—
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage	V _{DS} = 15V, I _D = 2mA		50	mV
Δ V _{GS1} -V _{GS2} ΔT	Gate-Source Voltage Differential Drift (Note 3)	(T _A = -55°C to +125°C)		100	μV/°C
g _{fs1} g _{fs2}	Transconductance Ratio (Notes 1 and 2)	V _{DS} = 15V, I _D = 2mA f = 1kHz	0.90	1	—

NOTES:

1. Pulse test required; pulse width 300μs, duty cycle ≤ 3%.

2. Assumes smaller value in numerator
3. Measured at end points T_A and T_B

IT1700

P-Channel Enhancement Mode MOSFET

1

FEATURES

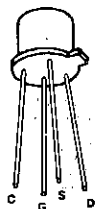
- Low ON-Resistance
- High Gain
- Low Noise Voltage
- High Input Impedance
- Low Leakage

ABSOLUTE MAXIMUM RATINGS

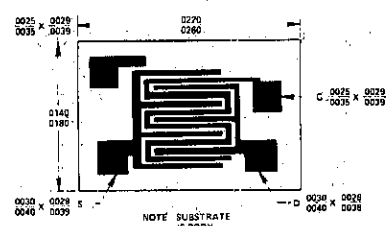
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source and Gate-Source Voltage	-40 V
Peak Gate-Source Voltage (Note 1)	± 125 V
Drain Current	50 mA
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$
Power Dissipation	375 mW
Derate above 25°C	3 mW/ $^\circ\text{C}$

PIN CONFIGURATION
TO-72



CHIP TOPOGRAPHY
1503



NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION*

TO-72	WAFER	DICE
IT1700	IT1700/W	IT1700/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{GS} = 0$ unless otherwise noted.

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS	
BV_{DSS}	Drain to Source Breakdown Voltage	-40		V	$V_{GS} = 0, I_D = -10 \mu\text{A}$
BV_{SDS}	Source to Drain Breakdown Voltage	-40		V	$V_{GS} = 0, I_D = -10 \mu\text{A}$
I_{GSS}	Gate Leakage Current	(See note 2)			
I_{DSS}	Drain to Source Leakage Current		200	μA	$V_{GS} = 0, V_{DS} = -20 \text{ V}$
$I_{DSS} (150^\circ\text{C})$	Drain to Source Leakage Current		0.4	μA	
I_{SDS}	Source to Drain Leakage Current		400	μA	
$I_{SDS} (150^\circ\text{C})$	Source to Drain Leakage Current		0.8	μA	
$V_{GS(th)}$	Gate Threshold Voltage	-2	-5	V	$V_{GS} = V_{DS}, I_D = -10 \mu\text{A}$
$r_{DS(on)}$	Static Drain to Source "on" Resistance		400	ohms	$V_{GS} = -10 \text{ V}, V_{DS} = 0$
$I_{DS(on)}$	Drain to Source "on" Current	2		mA	$V_{GS} = -10 \text{ V}, V_{DS} = -15 \text{ V}$
g_{fs}	Forward Transconductance Common Source	2000	4000	μmhos	$V_{DS} = -15 \text{ V}, I_D = -10 \text{ mA}$ $f = 1 \text{ kHz}$
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance		5	pF	$V_{DS} = -15 \text{ V}, I_D = -10 \text{ mA}$ $f = 1 \text{ MHz}$
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance		1.2	pF	$V_{DG} = -15 \text{ V}, I_D = 0$ $f = 1 \text{ MHz}$
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance		3.5	pF	$V_{DS} = -15 \text{ V}, I_D = -10 \text{ mA}$ $f = 1 \text{ MHz}$

NOTES: 1. Device must not be tested at $\pm 125\text{V}$ more than once nor longer than 300 ms.

2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of $< 10 \mu\text{A}$. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

IT1750 N-Channel Enhancement Mode MOSFET

FEATURES

- Low ON Resistance
- Low C_{dg}
- High Gain
- Low Threshold Voltage

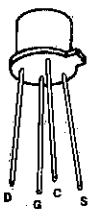
1
ABSOLUTE MAXIMUM RATINGS

 ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source and Gate-Source Voltage	25V
Peak Gate-Source Voltage (Note 1)	$\pm 125\text{V}$
Drain Current	100 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	375 mW
Derate above 25°C	3 mW/ $^\circ\text{C}$

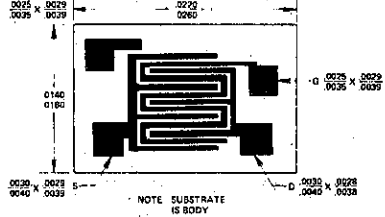
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1003



NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION*

TO-72	WAFER	DICE
IT1750	IT1750/W	IT1750/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Body connected to Source and $V_{BS} = 0$ unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GS(th)}$ Gate to Source Threshold Voltage	0.50	1.5	3.0	V	$V_{DS} = V_{GS}$, $I_D = 10 \mu\text{A}$
I_{DSS} Drain Leakage Current		0.1	10	nA	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$
I_{GSS} Gate Leakage Current		See note 2.			
BV_{DSS} Drain Breakdown Voltage	25			V	$I_D = 10 \mu\text{A}$, $V_{GS} = 0$
$r_{DS(on)}$ Drain To Source on Resistance		25	50	ohms	$V_{GS} = 20 \text{ V}$
$I_{D(on)}$ Drain Current	10	50		mA	$V_{DS} = V_{GS} = 10 \text{ V}$
Y_{fs} Forward Transadmittance	3,000			μmhos	$V_{DS} = 10 \text{ V}$, $I_D = 10 \text{ mA}$, $f = 1 \text{ KHz}$
C_{iss} Total Gate Input Capacitance		5.0	6.0	pF	$I_D = 10 \text{ mA}$, $V_{DS} = 10 \text{ V}$, $f = 1 \text{ MHz}$
C_{dg} Gate to Drain Capacitance		1.3	1.6	pF	$V_{DG} = 10 \text{ V}$, $f = 1 \text{ MHz}$

NOTES:

1. Devices must not be tested at $\pm 125\text{V}$ more than once nor longer than 300 ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of $< 10\text{pA}$. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

FEATURES

- Low $r_{DS(on)}$

APPLICATIONS

- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage -25V
 Gate Current 50 mA
 Storage Temperature Range .. -65°C to +200°C
 Operating Temperature Range -55°C to +150°C
 Lead Temperature (Soldering, 10 sec.)...+300°C
 Power Dissipation 360 mW
 Derate above 25°C 3.3 mW/°C

**PIN
CONFIGURATION
TO-92**


ORDERING INFORMATION*

J105	TO-92 only
J106	TO-92 only
J107	TO-92 only

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted *When ordering wafer/dice refer to Appendix B-23.

PARAMETER	J105			J106			J107			UNIT	TEST CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
I_{GSS}			-3			-3			-3	nA	$V_{DS}=0V, V_{GS}=-15V$
$V_{GS(off)}$	-4.5		-10	-2		-6	-0.5		-4.5	V	$V_{DS}=5V, I_D=1\mu A$
BV_{GSS}	-25			-25			-25			V	$V_{DS}=0V, I_G=-1\mu A$
I_{DSS}	500			200			100			mA	$V_{DS}=15V, V_{GS}=0V$
$I_{D(off)}$			3			3			3	nA	$V_{DS}=5V, V_{GS}=-10V$
$r_{DS(on)}$			3			6			8	Ω	$V_{DS}\leq 0.1V, V_{GS}=0V$
$C_{dg(off)}$			35			35			35	pF	$V_{DS}=0V, V_{GS}=-10V$ $V_{DS}=V_{GS}=0V$ $f=1\text{ MHz}$
$C_{sg(off)}$			35			35			35		
$C_{dg(on)}$ + $C_{sg(on)}$			160			160			160		
$t_{d(on)}$		15		15			15			ns	Switching Time Test Conditions J105 J106 J107 V_{DD} 1.5V 1.5V 1.5V $V_{GS(off)}$ -12V -7V -5V R_L 50 Ω 50 Ω 50 Ω
t_r		20		20			20				
$t_{d(off)}$		15		15			15				
t_f		20		20			20				

NOTES: 1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse test duration = 300 μs ; duty cycle $\leq 3\%$.

1

FEATURES

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltage Generated by Closed Switch
- Purely Resistive
- High Isolation Resistance from Driver
- Fast Switching
- Short Sample and Hold Aperture Time

APPLICATIONS

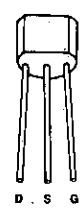
- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-35V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	310 mW
Derate Above 25°C	2.8 mW/°C

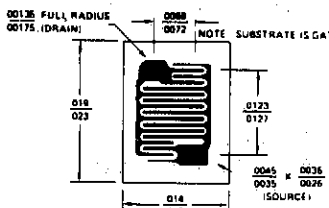
PIN CONFIGURATION



TO-92

D S G

CHIP TOPOGRAPHY



5001

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO-92	WAFER	DICE
J111	J111/W	J111/D
J112	J112/W	J112/D
J113	J113/W	J113/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS		J111			J112			J113			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
I _{GSSR}	Gate Reverse Current (Note 1)			-1			-1			-1	nA	V _{DS} = 0V, V _{GS} = -15V
V _{GS(off)}	Gate Source Cutoff Voltage	-3		-10	-1		-5	-0.5		-3	V	V _{DS} = 5V, I _D = 1μA
BV _{GSS}	Gate Source Breakdown Voltage	-35		-35			-35					V _{DS} = 0V, I _G = -1μA
I _{DSS}	Drain Saturation Current (Note 2)	20		5			2				mA	V _{DS} = 15V, V _{GS} = 0V
I _{D(off)}	Drain Cutoff Current (Note 1)			1			1			1	nA	V _{DS} = 5V, V _{GS} = -10V
r _{DS(on)}	Drain Source ON Resistance			30			50			100	Ω	V _{DS} = 0.1V, V _{GS} = 0V
C _{DG(off)}	Drain Gate OFF Capacitance			5			5			5	pF	V _{DS} = 0V, V _{GS} = -10V V _{DS} = V _{GS} = 0 f = 1 MHz
C _{SG(off)}	Source Gate OFF Capacitance			5			5			5		
C _{DG(on)} C _{SG(on)}	Drain Gate Plus Source Gate ON Capacitance			28			28			28		
t _{d(on)}	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions J111 J112 J113 V _{DD} 10V 10V 10V V _{GS(off)} -12V -7V -5V R _L 0.8kΩ 1.6kΩ 3.2kΩ
t _r	Rise Time		6			6			6			
t _{d(off)}	Turn Off Delay Time		20			20			20			
t _f	Fall Time		15			15			15			

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300μs; duty cycle ≤ 3%.

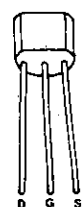
FEATURES

- Low Insertion Loss
- No Offset or Error Generated by Closed Switch
 - Purely Resistive
 - High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
- Fast Switching

APPLICATIONS

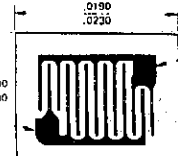
- Analog Switches
- Choppers
- Commutators

PIN CONFIGURATION
TO-92



D G S

CHIP TOPOGRAPHY (Note 1)
5508



NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO-92	WAFER	DICE
J17X	J17X/W	J17X/D

1

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1)	30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	350 mW
Derate above 25°C	3.5 mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS		J174			J175			J176			J177			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I _{GSSR}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V _{DS} = 0, V _{GS} = 20V	
V _{GS(off)}	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V _{DS} = -15V, I _D = -10nA	
BV _{GSS}	Gate-Source Breakdown Voltage	30		30			30			30					V _{DS} = 0, I _G = 1μA	
I _{DSS}	Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V _{DS} = -15V, V _{GS} = 0	
I _{D(off)}	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V _{DS} = -15V, V _{GS} = 10V	
r _{DS(on)}	Drain-Source ON Resistance			85			125			250			300	Ω	V _{GS} = 0, V _{DS} = -0.1V	
C _{dg(off)}	Drain-Gate OFF Capacitance			5.5			5.5			5.5			5.5	pF	V _{DS} = 0, V _{GS} = 10V	
C _{sg(off)}	Source-Gate OFF Capacitance			5.5			5.5			5.5			5.5		f = 1 MHz	V _{DS} = V _{GS} = 0
C _{dg(on)} + C _{sg(on)}	Drain-Gate Plus Source Gate ON Capacitance			40			40			40			40			
t _{o(on)}	Turn On Delay Time			2			5			15			20	ns	Switching Time Test Conditions	
t _r	Rise Time			5			10			20			25		J174 J175 J176 J177	
t _{d(off)}	Turn Off Delay Time			5			10			15			20		V _{DD} -10V -8V -6V -6V	
t _f	Fall Time			10			20			20			25		V _{GS(off)} 12V 8V 6V 3V	
															R _L 560Ω 12KΩ 5.6KΩ 10KΩ	
														V _{GS(on)} 0V 0V 0V 0V		

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration -300μs; duty cycle ≤ 3%.

1

FEATURES

- High Input Impedance
- Low I_{GSS}

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	360 mW
Derate above 25°C	3.3mW/°C

PIN CONFIGURATION
TO-92

CHIP TOPOGRAPHY
5010*

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO-92	WAFER	DICE
J201	J201/W	J201/D
J202	J202/W	J202/D
J203	J203/W	J203/D
J204	J204/W	J204/D

*DICE WITH 4 MIL BONDING PADS AVAILABLE. CONSULT FACTORY FOR DETAILS.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS	J201			J202			J203			J204			UNIT	TEST CONDITIONS	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS} Gate Reverse Current (Note 2)			-100			-100			-100			-100	pA	$V_{DS} = 0, V_{GS} = -20V$	
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	-0.5		-2.0	V	$V_{DS} = 20V, I_D = 10\mu A$	
BV_{GSS} Gate-Source Breakdown Voltage	-40			-40			-40			-25			V	$V_{DS} = 0, I_G = -1\mu A$	
I_{DSS} Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20			1.2	mA	$V_{DS} = 20V, V_{GS} = 0$	
I_G Gate Current (Note 1)		-3.5			-3.5			-3.5			-3.5		pA	$V_{DG} = 20V, I_D = 200\mu A$	
g_{fs} Common-Source Forward Transconductance (Note 2)	500			1,000			1,500					1,500			
g_{os} Common Source Output Conductance		1			3.5			10				2.5	μmho	$V_{DS} = 20V, V_{GS} = 0$	$f = 1\text{ kHz}$
C_{iss} Common-Source Input Capacitance		4			4			4				4	pF		
C_{ras} Common-Source Reverse Transfer Capacitance		1			1			1				1			
\bar{e}_n Equivalent Short-Circuit Input Noise Voltage		5			5			5				10	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10V, V_{GS} = 0$	$f = 1\text{ kHz}$

NOTES: 1. Approximately doubles for every 10°C increase in T_A .
2. Pulse test duration = 2ms.

1

PARAMETERS		J204			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX			
S T A T I C	I_{GSS}	Gate Reverse Current (Note 2)		-100	pA	$V_{DS} = 0, V_{GS} = -20V$	
	$V_{GS(off)}$	-0.5	Gate-Source Cutoff Voltage		V	$V_{DS} = 20V, I_D = 10nA$	
	BV_{GSS}	-25	Gate-Source Breakdown Voltage			$V_{DS} = 0, I_G = -\mu A$	
	I_{DSS}	Saturation Drain Current (Note 3)		1.2	mA	$V_{DS} = 20V, V_{GS} = 0$	
	I_G	Gate Current (Note 1)		-3.5	pA	$V_{DG} = 20V, I_D 200\mu A$	
D Y N A M I C	g_{fs}	Common-Source Forward Transconductance (Note 2)		1500	μmho	$V_{DS} = 20V, V_{GS} = 0$	f = 1kHz
	g_{os}	Common Source Output Conductance		2.5			f = 1MHz
	C_{iss}	Common-Source Input Capacitance		4	pF		f = 1MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		1			f = 1kHz
	e_n	Equivalent Short-Circuit Input Noise Voltage		10	$\frac{nV}{Hz}$		$V_{DS} = 10V, V_{GS} = 0$

FEATURES

- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater than 100 dB
- Easily Matched to 75Ω Input

1

APPLICATIONS

- VHF/UHF Amplifiers
- Oscillators
- Mixers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering; 10 sec.)	+300°C
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

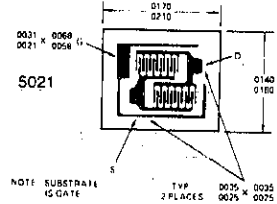
PARAMETER	J308			J309			J310			UNIT	TEST CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage									V	$I_G = -1\mu\text{A}, V_{DS} = 0$
I_{GSSR}	Gate Reverse Current									nA	$V_{GS} = -15\text{V}, V_{DS} = 0$
$V_{GS(off)}$	Gate-Source Cutoff Voltage									μA	$V_{DS} = 10\text{V}, I_D = 1\text{nA}$
I_{DSS}	Saturation Drain Current (Note 1)									mA	$V_{DS} = 10\text{V}, V_{GS} = 0$
$V_{GS(f)}$	Gate-Source Forward Voltage									V	$V_{DS} = 0, I_G = 1\text{mA}$
g_{fs}	Common-Source Forward Transconductance										
g_{os}	Common-Source Output Conductance										
g_{fg}	Common-Gate Forward Transconductance									μmhos	$V_{DS} = 10\text{V}, I_D = 10\text{mA}$
g_{og}	Common-Gate Output Conductance										
C_{gd}	Gate-Drain Capacitance										
C_{gs}	Gate-Source Capacitance									pF	$V_{DS} = 0, V_{GS} = -10\text{V}$
e_n	Equivalent Short-Circuit Input Noise Voltage									$\frac{nV}{\sqrt{\text{Hz}}}$	$V_{DS} = 10\text{V}, I_D = 10\text{mA}$
$Re(v_{is})$	Common-Source Forward Transconductance										
$Re(v_{fg})$	Common-Gate Input Conductance										
$Re(v_{is})$	Common-Source Input Conductance									mmho	
$Re(v_{os})$	Common-Source Output Conductance										$V_{DS} = 10\text{V}, I_D = 10\text{mA}$
G_{pg}	Common-Gate Power Gain at Noise Match										
NF	Noise Figure									dB	$f = 105\text{MHz}$
G_{pg}	Common-Gate Power Gain at Noise Match										
NF	Noise Figure										$f = 450\text{MHz}$

NOTE: 1. Pulse test PW 300 μs , duty cycle $\leq 3\%$.

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION*

TO-92	WAFER	DICE
J30X	J30X/W	J30X/D

*When ordering wafer/dice refer to Appendix B-23.



LM114/H, LM114A/AH Monolithic Dual NPN Transistor

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10 μ A collector current. Typical collector-base capacitance is only 1.6 pF at 5V.

ABSOLUTE MAXIMUM RATINGS

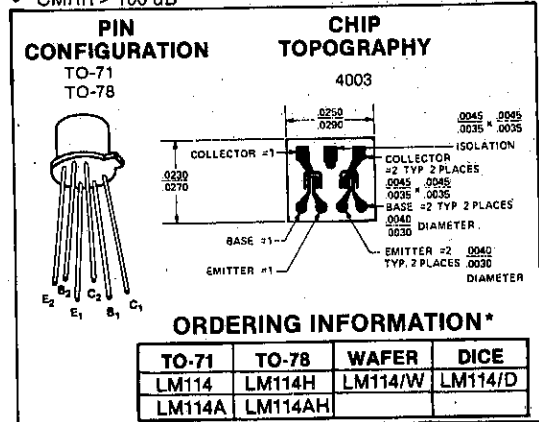
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base Voltage (1)	45V
Collector-Emitter Voltage (1)	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (1)	6V
Collector Current (1)	20mA
Storage Temperature Range	-65 $^\circ\text{C}$ to +200 $^\circ\text{C}$
Operating Temperature Range	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	+300 $^\circ\text{C}$
Power Dissipation	800mW
Derate above 25 $^\circ\text{C}$	14mW/ $^\circ\text{C}$

FEATURES

- Low offset voltage
- Low drift
- High current gain
- Tight beta match
- High breakdown voltage
- Matching guaranteed over a 0V to 45V collector-base voltage range
- CMRR > 100 dB

1



ELECTRICAL CHARACTERISTICS (Note 2)

*When ordering wafer/dice refer to Appendix B-23.

PARAMETER	MAXIMUM LIMITS		UNITS	CONDITIONS
	LM114A, AH	LM114, H		
Offset Voltage	0.5	2.0	mV	$1\mu\text{A} \leq I_C \leq 100\mu\text{A}$
Offset Current	2.0	10	nA	$I_C = 10\mu\text{A}$
	0.5			$I_C = 1\mu\text{A}$
Bias Current	20	40	nA	$I_C = 10\mu\text{A}$
	3.0			$I_C = 1\mu\text{A}$
Offset Voltage Change	0.2	1.5	mV	$0\text{V} \leq V_{CB} \leq V_{MAX}, I_C = 10\mu\text{A}$
Offset Current Change	1.0	4.0	nA	
Offset Voltage Drift	2.0	10	$\mu\text{V}/^\circ\text{C}$	
Offset Current	12	50	nA	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}, I_C = 10\mu\text{A}$
Bias Current	60	150	nA	
Collector-Base Leakage Current	10	50	pA	$V_{CB} = V_{MAX}$
	$T_A = 125^\circ\text{C}$	10	50	nA
Collector-Emitter Leakage Current	50	200	pA	$V_{CE} = V_{MAX}, V_{EB} = 0\text{V}$
	$T_A = 125^\circ\text{C}$	50	200	nA
Collector-Collector Leakage Current	100	300	pA	$V_{CC} = V_{MAX}$
	$T_A = 125^\circ\text{C}$	100	300	nA

Note 1: Per transistor.

Note 2: These specifications apply for $T_A = +25^\circ\text{C}$ and $0\text{V} \leq V_{CB} \leq V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, $V_{MAX} = 30\text{V}$.

M116

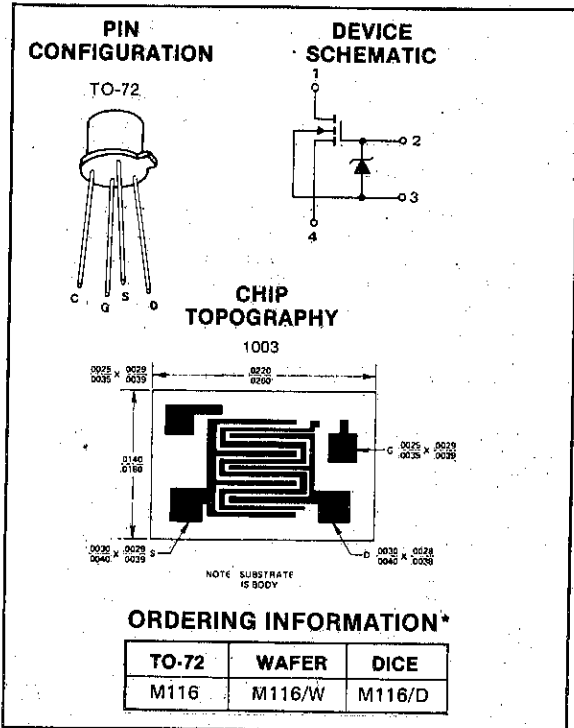
Diode Protected N-Channel Enhancement Mode MOSFET

FEATURES

- Low I_{GSS}
- Integrated Zener Clamp for Gate Protection

1
ABSOLUTE MAXIMUM RATINGS
 $(T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain to Source Voltage	30V
Gate to Drain Voltage	30V
Drain Current	50 mA
Gate Zener Current	± 0.1 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	2.2 mW/ $^\circ\text{C}$



*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		M116		UNITS	TEST CONDITIONS
		MIN	MAX		
$r_{DS(on)}$	Drain Source ON Resistance		100 200	Ω	$V_{GS} = 20\text{ V}, I_D = 100\ \mu\text{A}, V_{BS} = 0$ $V_{GS} = 10\text{ V}, I_D = 100\ \mu\text{A}, V_{BS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	1	5	V	$V_{GS} = V_{DS}, I_D = 10\ \mu\text{A}, V_{BS} = 0$ $I_D = 1\ \mu\text{A}, V_{GS} = V_{BS} = 0$
BV_{DSS}	Drain-Source Breakdown Voltage	30			$I_S = 1\ \mu\text{A}, V_{GD} = V_{BD} = 0$
BV_{SDS}	Source-Drain Breakdown Voltage	30		nA	$I_G = 10\ \mu\text{A}, V_{SB} = V_{DB} = 0$ $V_{DS} = 20\text{ V}, V_{GS} = V_{BS} = 0$
BV_{GBS}	Gate-Body Breakdown Voltage	30	60		$V_{SD} = 20\text{ V}, V_{GD} = V_{BD} = 0$
$I_{D(OFF)}$	Drain Cutoff Current		10	pA	$V_{GS} = 20\text{ V}, V_{DS} = V_{BS} = 0$
$I_{S(OFF)}$	Source Cutoff Current		10		$V_{GB} = 0, V_{DB} = 10\text{ V}, f = 1\text{ MHz}$ Body Guarded
I_{GSS}	Gate-Body Leakage		100	pF	$V_{GB} = 0, V_{DB} = 10\text{ V}, f = 1\text{ MHz}$ $V_{GB} = 0, V_{DB} = 10\text{ V}, V_{BS} = 0$ $f = 1\text{ MHz}$
C_{gs}	Gate-Source		2.5		
C_{gd}	Gate-Drain Capacitance		2.5		
C_{db}	Drain-Body Capacitance		7		
C_{iss}	Input Capacitance		10		

U200-U202 N-Channel JFET

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FEATURES

- Low Insertion Loss
- Good OFF Isolation

APPLICATIONS

- Analog Switches
- Commutators
- Choppers

PIN CONFIGURATION

TO-18

CHIP TOPOGRAPHY

ORDERING INFORMATION*

TO-18	WAFER	DICE
U200	U200/W	U200/D
U201	U201/W	U201/D
U202	U202/W	U202/D

*When ordering wafer/dice refer to Appendix B-23.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Total Device Dissipation	1.8W
Derate above 25°C	10 mW/°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Parameter		U200		U201		U202		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	$V_{GS} = 20\text{ V}, V_{DS} = 0$
		$T_A = 150^\circ\text{C}$	-1	-1	-1	-1	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	$I_G = 1\ \mu\text{A}, V_{DS} = 0$
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		$V_{DS} = 20\text{ V}, I_D = 10\text{ nA}$
$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	$V_{DS} = 10\text{ V}, V_{GS} = -12\text{ V}$
		$T_A = 150^\circ\text{C}$	1	1	1	μA			
I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	$V_{DS} = 20\text{ V}, V_{GS} = 0$
$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	$V_{GS} = 0, I_D = 0$
C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	$V_{DS} = 20\text{ V}, V_{GS} = 0$
C_{rss}	Common Source Reverse Transfer Capacitance		8		8		8		$V_{DS} = 0, V_{GS} = -12\text{ V}$

NOTE 1: Pulse test required, pulsewidth = 300 μsec , duty cycle $\leq 3\%$.

U231-U235 Monolithic Dual N-Channel JFET

FEATURES

- Good Matching Characteristics

APPLICATIONS

- Differential Amplifiers
- Low and Maximum Frequency Amplifiers

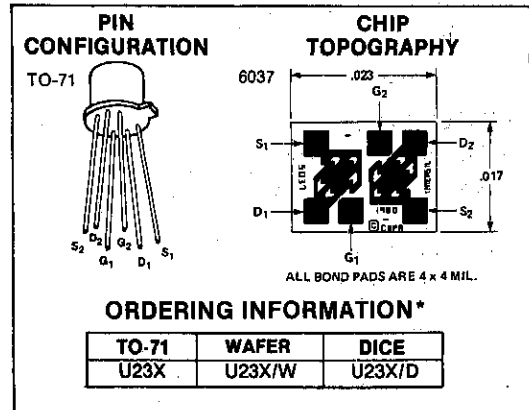
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate Current (Note 1)	50 mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Load Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$
Power Dissipation	300 mW
Derate above 25°C	1.7 mW/ $^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.



*When ordering wafer/dice refer to Appendix B-23.

Parameter		Min	Max	Unit	Test Conditions
I_{GSSR}	Gate Reverse Current		-100	pA	$V_{GS} = -30V, V_{DS} = 0$
			-500	nA	$T_A = 150^\circ\text{C}$
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = 1\mu\text{A}, V_{DS} = 0$
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		$V_{DS} = 20V, I_D = 1\text{ nA}$
V_{GS}	Gate-Source Voltage	-0.3	-4.0		
I_G	Gate Operating Current		-50	pA	$V_{DG} = 20V, I_D = 200\mu\text{A}$
			-250	nA	$T_A = 125^\circ\text{C}$
I_{DSS}	Saturation Drain Current (Note 2)	0.5	5.0	mA	$V_{DS} = 20V, V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000		$V_{DS} = 20V, V_{GS} = 0$
		1000		μmho	$f = 1\text{ kHz}$
g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		$V_{DS} = 20V, I_D = 200\mu\text{A}$
g_{os}	Common-Source Output Capacitance		35		$V_{DS} = 20V, V_{GS} = 0$
g_{os}	Common-Source Output Conductance		10		$V_{DG} = 20V, I_D = 200\mu\text{A}$
C_{iss}	Common-Source Input Capacitance		6	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance		2		$V_{DS} = 20V, V_{GS} = 0$
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$	$f = 100\text{ Hz}$

Matching Characteristics		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions
$ I_{G1} - I_{G2} $	Differential Gate Current	10	10	10	10	10	nA	$V_{DG} = 20V, I_D = 200\mu\text{A}, 125^\circ\text{C}$
$(I_{DSS1} - I_{DSS2}) / I_{DSS1}$	Saturation Drain Current Match (Note 2)	5	5	5	10	15	%	$V_{DS} = 20V, V_{GS} = 0$
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	5	10	15	20	25	mV	
$\Delta V_{GS1} - V_{GS2} $	Gate-Source Voltage Differential Drift (Note 3)	10	25	50	75	100	$\mu\text{V}/^\circ\text{C}$	$T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$
$(g_{fs1} - g_{fs2}) / g_{fs1}$	Transconductance Match (Note 2)	3	5	5	10	15	%	$V_{DG} = 20V, I_D = 200\mu\text{A}$
$ g_{os1} - g_{os2} $	Differential Output Conductance	5	5	5	5	5	μmho	$f = 1\text{ kHz}$

NOTES:

1. Per transistor.
2. Pulse test required, pulse width = 300 μs , duty cycle $\leq 3\%$.
3. Measured at end points, T_A and T_B .



U257 Monolithic Dual N-Channel JFET

FEATURES

- $g_{fs} > 5000 \mu\text{mho}$ from DC to 100 MHz
- Matched V_{GS} , g_{fs} and g_{os}

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) -25V	
Gate Current (Note 1) 50 mA	
Storage Temperature Range -65°C to $+200^\circ\text{C}$	
Operating Temperature Range -55°C to $+150^\circ\text{C}$	
Lead Temperature (Soldering, 10 sec.) $+300^\circ\text{C}$	
	ONE SIDE	BOTH SIDES
Power Dissipation 250 mW 500 mW
Derate above 25°C 3.8 mW/ $^\circ\text{C}$ 7.7 mW/ $^\circ\text{C}$

PIN CONFIGURATION

TO-99

CHIP TOPOGRAPHY

6022

ORDERING INFORMATION*

TO-99	WAFER	DICE
U257	U257/W	U257/D

*When ordering wafer/dice refer to Appendix B-23.

1

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
I_{GSSR}	Gate Reverse Current		-100	pA	$V_{GS} = 15\text{ V}, V_{DS} = 0$
		$T_A = 150^\circ\text{C}$	-250	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	-1	-5		$V_{DS} = 10\text{ V}, I_D = 1\text{ nA}$
I_{DSS}	Saturation Drain Current (Note 2)	5	40	mA	$V_{DS} = 10\text{ V}, V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	$V_{DS} = 10\text{ V}, I_D = 5\text{ mA}, f = 1\text{ kHz}$
g_{fs}	Common-Source Forward Transconductance	5000	10,000		$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}, f = 100\text{ MHz}$
g_{os}	Common-Source Output Conductance		150		$V_{DS} = 10\text{ V}, I_D = 5\text{ mA}, f = 1\text{ kHz}$
g_{oss}	Common-Source Output Conductance		150		$f = 100\text{ MHz}$
C_{iss}	Common-Source Input Capacitance		5	pF	$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}$
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		
\bar{e}_n	Equivalent Input Noise Voltage		30	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$f = 10\text{ kHz}$
I_{DSS1}	Drain Current Ratio at Zero Gate Voltage (Note 2)	0.85	1		$V_{DS} = 10\text{ V}, V_{GS} = 0$
I_{DSS2}					
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		100	mV	$V_{DG} = 10\text{ V}, I_D = 5\text{ mA}, f = 1\text{ kHz}$
g_{fs1}	Transconductance Ratio	0.85	1		
g_{fs2}					
$ g_{os1} - g_{os2} $	Differential Output Conductance		20	μmho	

NOTES:

1. Per transistor.
2. Pulse test required, pulse width = $300 \mu\text{s}$, duty cycle $\leq 3\%$.

U304-U306 P-Channel JFET

FEATURES

- Low ON Resistance
- $I_{D(off)} < 500 \text{ pA}$
- Switches directly from T²L Logic (U306)

1

APPLICATIONS

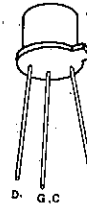
- Analog Switches
- Commutators
- Choppers

ABSOLUTE MAXIMUM RATINGS

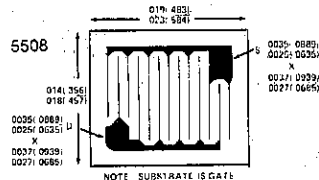
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1)	30V
Gate Current	50 mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	350 mW
Derate above 25°C	2.8 mW/°C

PIN CONFIGURATION TO-18



CHIP TOPOGRAPHY (Note 1)



ORDERING INFORMATION*

TO-18	WAFER	DICE
U304	U304/W	U304/D
U305	U305/W	U305/D
U306	U306/W	U306/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.

*When ordering wafer/dice refer to Appendix B-23.

Parameter	U304		U305		U306		Unit	Test Conditions																								
	Min	Max	Min	Max	Min	Max																										
I_{GSSR} Gate Reverse Current		500		500		500	pA	$V_{GS} = 20V, V_{DS} = 0$																								
	$T_A = 150^\circ\text{C}$	1.0	1.0	1.0	1.0	μA																										
BV_{GSS} Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1 \mu\text{A}, V_{DS} = 0$ $V_{DS} = -15V, I_D = -1 \mu\text{A}$																								
$V_{GS(off)}$ Gate-Source Cutoff Voltage	5	10	3	6	1	4																										
$V_{DS(on)}$ Drain-Source ON Voltage		-1.3		-0.8		-0.6	mV	$V_{GS} = 0, I_D = -15\text{mA (U304)},$ $I_D = -7\text{mA (U305)},$ $I_D = -3\text{mA (U306)}$																								
I_{DSS} Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25			$V_{DS} = -15V, V_{GS} = 0$																							
$I_{D(off)}$ Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15V, V_{GS} = 12V \text{ (U304)}$ $V_{GS} = 7V \text{ (U305)}$ $V_{GS} = 5V \text{ (U306)}$																								
	$T_A = 150^\circ\text{C}$	-1.0	-1.0	-1.0	μA																											
$r_{DS(on)}$ Static Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0V, I_D = 0$ $V_{DS} = -15V, V_{GS} = 0$																								
$r_{DS(on)}$ Drain-Source ON Resistance		85		110		175																										
C_{iss} Common-Source Input Capacitance		27		27		27	pF	$V_{DS} = 0, V_{GS} = 12V \text{ (U304)}$ $V_{GS} = 7V \text{ (U305)},$ $V_{GS} = 5V \text{ (U306)}$																								
C_{rss} Common-Source Reverse Transfer Capacitance		7		7		7																										
$t_{d(on)}$ Turn-ON Delay Time		20		25		25	ns	<table border="1"> <thead> <tr> <th></th> <th>U304</th> <th>U305</th> <th>U306</th> </tr> </thead> <tbody> <tr> <td>V_{DD}</td> <td>-10V</td> <td>-6V</td> <td>-6V</td> </tr> <tr> <td>$V_{GS(off)}$</td> <td>12V</td> <td>7V</td> <td>5V</td> </tr> <tr> <td>R_L</td> <td>580Ω</td> <td>743Ω</td> <td>1800Ω</td> </tr> <tr> <td>$V_{GS(on)}$</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>$I_{D(on)}$</td> <td>-15mA</td> <td>-7mA</td> <td>-3mA</td> </tr> </tbody> </table>		U304	U305	U306	V_{DD}	-10V	-6V	-6V	$V_{GS(off)}$	12V	7V	5V	R_L	580 Ω	743 Ω	1800 Ω	$V_{GS(on)}$	0	0	0	$I_{D(on)}$	-15mA	-7mA	-3mA
	U304	U305	U306																													
V_{DD}	-10V	-6V	-6V																													
$V_{GS(off)}$	12V	7V	5V																													
R_L	580 Ω	743 Ω	1800 Ω																													
$V_{GS(on)}$	0	0	0																													
$I_{D(on)}$	-15mA	-7mA	-3mA																													
t_r Rise Time		15		25		35																										
$t_{d(off)}$ Turn-OFF Delay Time		10		15		20																										
t_f Fall Time		25		40		60																										

NOTES:

1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 μs , duty cycle $\leq 3\%$.

FEATURES

- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater than 100 dB
- Easily Matched to 75Ω Input


ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	20 mA
Storage Temperature	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Led Temperature (Soldering, 10 sec.)	+300°C
Power Dissipation	500 mW
Derate above 25°C	4mW/°C

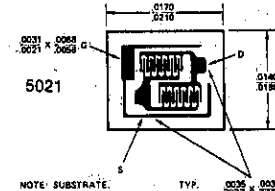
PIN CONFIGURATIONS

TO-52



G, C
D
S

CHIP TOPOGRAPHY



NOTE: SUBSTRATE IS GATE.
TYP. 2 PLACES

ORDERING INFORMATION*

TO-52	WAFER	DICE
U308	U308/W	U308/D
U309	U309/W	U309/D
U310	U310/W	U310/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	U308			U309			U310			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSSR}	Gate Reverse Current $T_A = 125^\circ\text{C}$			-150			-150			-150	PA	$V_{GS} = -15\text{ V}$	
				-150			-150			-150	nA	$V_{GS} = 0$	
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0		$V_{DS} = 10\text{ V}, I_D = 1\ \text{nA}^*$	
I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10\text{ V}, V_{GS} = 0$	
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$I_G = 10\ \text{mA}, V_{DS} = 0$	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	$V_{DS} = 10\text{ V}, I_D = 10\ \text{mA}$	$f = 1\ \text{kHz}$
g_{ogs}	Common-Gate Output Conductance			150			150			150	μmho		
C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	$V_{GS} = -10\text{ V}, V_{DS} = 10\text{ V}$	$f = 1\ \text{MHz}$
C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{\text{Hz}}}$	$V_{DS} = 10\text{ V}, I_D = 10\ \text{mA}$	$f = 100\ \text{Hz}$
g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	$V_{DS} = 10\text{ V}, I_D = 10\ \text{mA}$	$f = 100\ \text{MHz}$
			14			14		14	$f = 450\ \text{MHz}$				
g_{ogs}	Common-Gate Output Conductance		0.18			0.18			0.18		$f = 100\ \text{MHz}$		
			0.32			0.32		0.32	$f = 450\ \text{MHz}$				
G_{pg}	Common-Gate Power Gain		16			16			16		$f = 100\ \text{MHz}$		
			11			11		11	$f = 450\ \text{MHz}$				
NF	Noise Figure		1.5			1.5			1.5		dB		$f = 100\ \text{MHz}$
			2.7			2.7		2.7	$f = 450\ \text{MHz}$				

NOTE: Pulse test duration = 2 ms.

U401-U406 Monolithic Dual N-Channel JFET

FEATURES

- Minimum System Error and Calibration
- Low Drift with Temperature
- Operates from Low Power Supply Voltages
- High Output Impedance

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Drain or Gate-Source Voltage (Note 1) 50V
 Gate Current (Note 1) 10 mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec) $+300^\circ\text{C}$

	ONE SIDE	BOTH SIDES
Power Dissipation	300 mW	500 mW
Derate above 25°C ..	2.6 mW/ $^\circ\text{C}$	5 mW/ $^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25° unless otherwise noted.

Parameters		U401		U402		U403		U404		U405		U406		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
BV _{GS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		V	$V_{DS} = 0, I_G = -1\mu\text{A}$
I _{GS}	Gate Reverse Current (Note 2)		-25		-25		-25		-25		-25		-25	pA	$V_{DS} = 0, V_{GS} = -30\text{V}$
V _{GS(off)}	Gate-Source Cutoff Voltage	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	V	$V_{DS} = 15\text{V}, I_D = 1\text{nA}$
V _{GS(on)}	Gate-Source Voltage (on)		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3	V	$V_{DG} = 15\text{V}, I_D = 200\mu\text{A}$
I _{DSS}	Saturation Drain Current (Note 3)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	$V_{DS} = 10\text{V}, V_{GS} = 0$
I _G	Operating Gate Current (Note 2) $T_A = 125^\circ\text{C}$		-15		-15		-15		-15		-15		-15	pA	$V_{DG} = 15\text{V}, I_D = 200\mu\text{A}$
BV _{G1-G2}	Gate-Gate Breakdown Voltage	± 50		± 50		± 50		± 50		± 50		± 50		V	$V_{DS} = 0, V_{GS} = 0, I_G = \pm 1\mu\text{A}$
g _{fs}	Common-Source Forward Transconductance (Note 3)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	$V_{DS} = 10\text{V}, V_{GS} = 0$ $f = 1\text{kHz}$
g _{os}	Common-Source Output Conductance		20		20		20		20		20		20		
g _{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	pF	$V_{DG} = 15\text{V}, I_D = 200\mu\text{A}$ $f = 1\text{MHz}$
g _{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0		
C _{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 10\text{Hz}$
C _{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0		
e _n	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	nV/√Hz	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 10\text{Hz}$
CMRR	Common-Mode Rejection Ratio (Note 4)	95		95		95		95		90				dB	$V_{DG} = 10\text{ to }20\text{V}, I_D = 200\mu\text{A}$
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	$V_{DG} = 10\text{V}, I_D = 200\mu\text{A}$
$\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Note 5)		10		10		25		25		40		80	μV/ $^\circ\text{C}$	$V_{DG} = 10\text{V}, I_D = 200\mu\text{A}$ $T_A = -55^\circ\text{C}, T_B = +25^\circ\text{C}, I_D = 200\mu\text{A}, T_C = +125^\circ\text{C}$

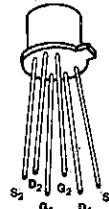
NOTES:

1. Per transistor.
2. Approximately doubles for every 10°C increase in T_A .
3. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
4. Measured at end points, T_A and T_B .

$$5. \text{CMRR} = 20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right], \Delta V_{DD} = 10 \text{ V.}$$

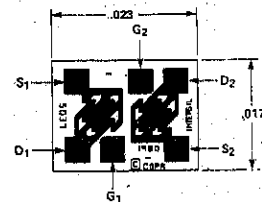
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6037



ORDERING INFORMATION*

TO-71	WAFER	DICE
U40X	U40X/W	U40X/D

*When ordering wafer/dice refer to Appendix B-23.

FEATURES

- Low Insertion Loss
- No Error or Offset Voltage Generated by Closed Switch

APPLICATIONS

Analog Switches, Choppers

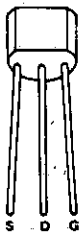
ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Drain or Gate-Source Voltage -40V
 Forward Gate Current 10 mA
 Storage Temperature Range .. -65°C to +200°C
 Operating Temperature Range.. -55°C to +150°C
 Lead Temperature (Soldering, 10 sec)... +300°C
 Power Dissipation 350 mW
 Derate above 25°C 3.5 mW/°C

ELECTRICAL CHARACTERISTICS

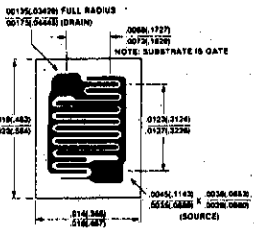
TEST CONDITIONS: 25°C unless otherwise noted

**PIN CONFIGURATION
TO-92**



S D G

**CHIP TOPOGRAPHY
5001**



NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION*

TO-92	TO-92-18	WAFER	DICE
U1897	U1897-18	U1897/W	U1897/D
U1898	U1898-18	U1898/W	U1898/D
U1899	U1899-18	U1899/W	U1899/D

*When ordering wafer/dice refer to Appendix B-23.

PARAMETERS		U1897		U1898		U1899		UNIT	TEST CONDITIONS																								
		MIN	MAX	MIN	MAX	MIN	MAX																										
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\mu\text{A}, V_{DS} = 0$																								
I_{GSSR}	Gate Reverse Current		-400		-400		-400		$V_{GS} = -20\text{V}, V_{DS} = 0$																								
I_{DGO}	Drain-Gate Leakage Current		200		200		200		$V_{DG} = 20\text{V}, I_S = 0$																								
I_{SGO}	Source-Gate Leakage Current		200		200		200		$V_{SG} = 20\text{V}, I_D = 0$																								
$I_{D(off)}$	Drain Cutoff Current		200		200		200		$V_{DS} = 20\text{V}, V_{GS} = -12\text{V}$ (U1897)																								
								nA	$V_{GS} = -8\text{V}$ (U1898) $V_{GS} = -6\text{V}$ (U1899)																								
			10		10		10		$T_A = 85^\circ\text{C}$																								
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5.0	-10	-2.0	-7.0	-1.0	-5.0	V	$V_{DS} = 20\text{V}, I_D = 1\text{na}$																								
I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	$V_{DS} = 20\text{V}, V_{GS} = 0$																								
$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0, I_D = 6.6\text{mA}$ (U1897) $I_D = 4.0\text{mA}$ (U1898) $I_D = 2.5\text{mA}$ (U1899)																								
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1\text{mA}, V_{GS} = 0$																								
C_{dg}	Drain-Gate Capacitance		5		5		5		$V_{DG} = 20\text{V}, I_S = 0$																								
C_{sg}	Source-Gate Capacitance		5		5		5		$V_{SG} = 20\text{V}, I_D = 0$																								
C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20\text{V}, V_{GS} = 0$																								
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5		$f = 1\text{MHz}$																								
$t_{d(on)}$	Turn ON Delay Time		15		15		20		Switching Time Test Conditions																								
t_r	Rise Time		10		20		40	ns																									
t_{off}	Turn OFF Time		40		60		80		<table border="1" style="width: 100%;"> <tr> <td>V_{DD}</td> <td>U1897</td> <td>U1898</td> <td>U1899</td> </tr> <tr> <td>$V_{GS(on)}$</td> <td>3V</td> <td>3V</td> <td>3V</td> </tr> <tr> <td>$V_{GS(off)}$</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>$V_{GS(off)}$</td> <td>-12V</td> <td>-8V</td> <td>-6V</td> </tr> <tr> <td>R_L</td> <td>425Ω</td> <td>770Ω</td> <td>1120Ω</td> </tr> <tr> <td>$I_{D(on)}$</td> <td>6.6mA</td> <td>4mA</td> <td>2.5mA</td> </tr> </table>	V_{DD}	U1897	U1898	U1899	$V_{GS(on)}$	3V	3V	3V	$V_{GS(off)}$	0	0	0	$V_{GS(off)}$	-12V	-8V	-6V	R_L	425 Ω	770 Ω	1120 Ω	$I_{D(on)}$	6.6mA	4mA	2.5mA
V_{DD}	U1897	U1898	U1899																														
$V_{GS(on)}$	3V	3V	3V																														
$V_{GS(off)}$	0	0	0																														
$V_{GS(off)}$	-12V	-8V	-6V																														
R_L	425 Ω	770 Ω	1120 Ω																														
$I_{D(on)}$	6.6mA	4mA	2.5mA																														

NOTE: 1. Pulse test pulsewidth = 300 μs ; duty cycle < 3%

VCR2N/3P/4N/7N Voltage Controlled Resistors

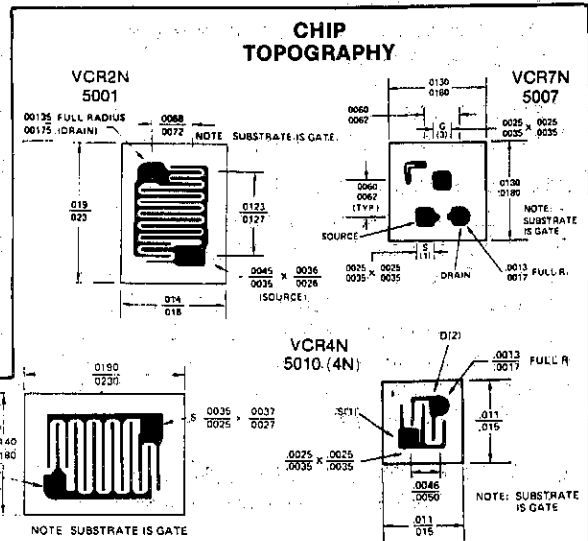
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APPLICATIONS

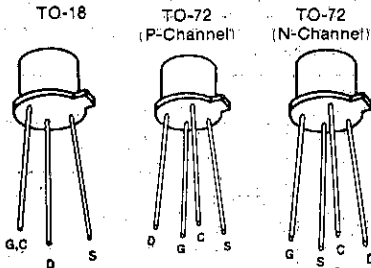
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Drain or Gate-Source Voltage 15V
 Gate Current 10 mA
 Storage Temperature Range ... -65°C to $+200^\circ\text{C}$
 Operating Temperature Range... -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec.)... $+300^\circ\text{C}$
 Power Dissipation 300 mW
 Derate above 25°C 2 mW/ $^\circ\text{C}$



PIN CONFIGURATIONS



ORDERING INFORMATION*

TO-18	TO-72	WAFER	DICE
VCR2N	—	VCR2N/W	VCR2N/D
VCR4N	—	VCR4N/W	VCR4N/D
—	VCR3P	VCR3P/W	VCR3P/D
—	VCR7N	VCR7N/W	VCR7N/D

*When ordering wafer/dice refer to Appendix B-23.

ELECTRICAL CHARACTERISTICS (25° C. unless otherwise noted)

N-Channel VCR FETs

Parameter	VCR2N		VCR4N		VCR7N		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
I_{gss} Gate Reverse Current		-5	-0.2	-0.1			nA	$V_{GS} = -15V, V_{DS} = 0$
BV_{GSS} Gate-Source Breakdown Voltage	-15		-15		-15		V	$I_G = -1\mu A, V_{DS} = 0$
$V_{GS(off)}$ Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5		$I_D = 1\mu A, V_{DS} = 10V$
$r_{ds(on)}$ Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	$V_{GS} = 0, I_D = 0$ f = 1 kHz
C_{dgo} Drain-Gate Capacitance		7.5		3		1.5	pF	$V_{GD} = -10V, I_S = 0$ f = 1 MHz
C_{sgo} Source-Gate Capacitance		7.5		3		1.5	pF	$V_{GS} = -10V, I_D = 0$

P-Channel VCR FETs

Parameter	VCR3P		Unit	Test Conditions
	Min	Max		
I_{gss} Gate Reverse Current		20	nA	$V_{GS} = 15V, V_{DS} = 0$
BV_{GSS} Gate-Source Breakdown Voltage	15		V	$I_G = 1\mu A, V_{DS} = 0$
$V_{GS(off)}$ Gate-Source Cutoff Voltage	3.5	7		$I_D = -1\mu A, V_{DS} = -10V$
$r_{ds(on)}$ Drain-Source ON Resistance	70	200	Ω	$V_{GS} = 0, I_D = 0$ f = 1 kHz
C_{dgo} Drain-Gate Capacitance		6	pF	$V_{GD} = 10V, I_S = 0$ f = 1 MHz
C_{sgo} Source-Gate Capacitance		6	pF	$V_{GS} = 10V, I_D = 0$

JFETS AS VOLTAGE CONTROLLED RESISTORS

The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of $V_{DS} = 0$ for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about 100k Ω .

Best gate control voltage for best linearity is up to about 0.8V P_{PK} ; ON resistance increases rapidly beyond this point.

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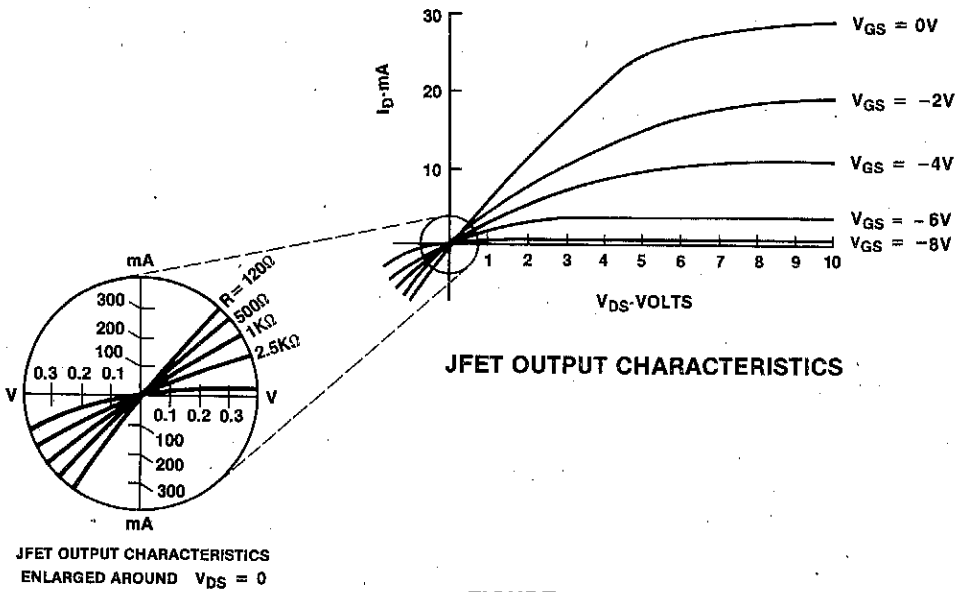


FIGURE 1

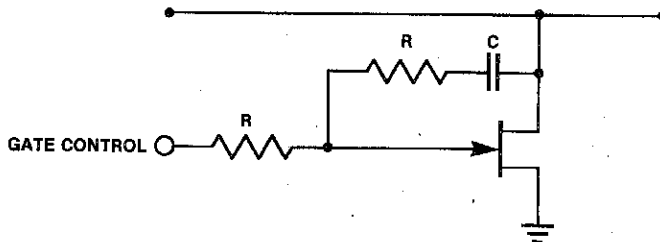


FIGURE 2

