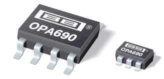
Burr-Brown Products from Texas Instruments

OPA690



SBOS223A—DECEMBER 2001 – REVISED JULY 2002

Wideband, Voltage Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  +5V to +12V Single Supply
  ±2.5V to ±5V Dual Supply
- **UNITY-GAIN STABLE: 500MHz (G = 1)**
- **HIGH OUTPUT CURRENT: 190mA**
- **OUTPUT VOLTAGE SWING: ±4.0V**
- **HIGH SLEW RATE: 1800V/μs**
- **LOW SUPPLY CURRENT: 5.5mA**
- **LOW DISABLED CURRENT: 100μA**
- **WIDEBAND +5V OPERATION: 220MHz (G = 2)**

APPLICATIONS

- **VIDEO LINE DRIVER**
- **xDSL LINE DRIVER/RECEIVER**
- **HIGH SPEED IMAGING CHANNELS**
- **ADC BUFFERS**
- **PORTABLE INSTRUMENTS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **ACTIVE FILTERS**
- **OPA680 UPGRADE**

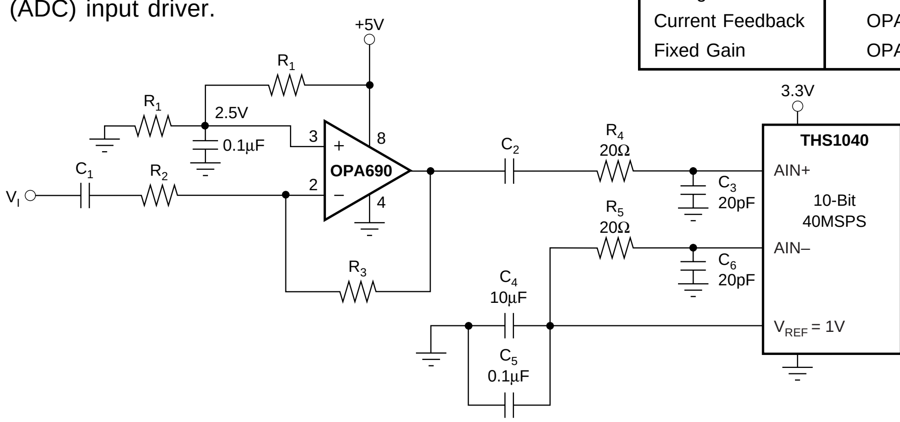
DESCRIPTION

The OPA690 represents a major step forward in unity-gain stable, voltage feedback op amps. A new internal architecture provides slew rate and full-power bandwidth previously found only in wideband current feedback op amps. A new output stage architecture delivers high currents with a minimal headroom requirement. These combine to give exceptional single-supply operation. Using a single +5V supply, the OPA690 can deliver a 1V to 4V output swing with over 150mA drive current and 150MHz bandwidth. This combination of features makes the OPA690 an ideal RGB line driver or single-supply Analog-to-Digital Converter (ADC) input driver.

The OPA690's low 5.5mA supply current is precisely trimmed at 25°C. This trim, along with low temperature drift, gives lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, will operate the OPA690 normally. If pulled LOW, the OPA690 supply current drops to less than 100μA while the output goes to a high impedance state. This feature may be used for power savings.

OPA690 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage Feedback	OPA680	OPA2690	OPA3690
Current Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	OPA2682	OPA3692



Single-Supply ADC Driver

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	$\pm 1.2V$
Input Voltage Range	$\pm V_S$
Storage Temperature Range: D, DBV	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C
ESD Resistance: HBM	2000V
MM	200V
CDM	1500V

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

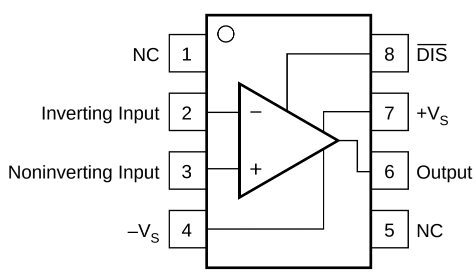
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA690ID	SO-8	D	–40°C to +85°C	OPA690	OPA690ID	Rails, 100
"	"	"	"	"	OPA690IDR	Tape and Reel, 2500
OPA690IDBV	SOT23-6	DBV	–40°C to +85°C	OAEI	OPA690IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA690IDBVR	Tape and Reel, 3000

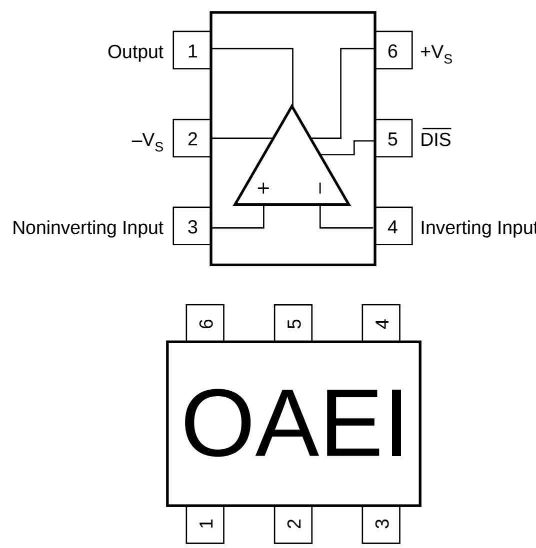
NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS

Top View **SO**



Top View **SOT23**



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C**.

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA690ID, IDBV TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	G = +1, V_O = 0.5Vp-p, R_F = 25Ω	500				MHz	typ	C
	G = +2, V_O = 0.5Vp-p	220	165	160	150	MHz	typ	C
	G = +10, V_O = 0.5Vp-p	30	20	19	18	MHz	typ	C
Gain-Bandwidth Product	G ≥ 10	300	200	190	180	MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	30				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.5Vp-p	4				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 5Vp-p	200				MHz	typ	C
Slew Rate	G = +2, 4V Step	1800	1400	1200	900	V/μs	typ	C
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.4				ns	typ	C
	G = +2, V_O = 5V Step	2.8				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd-Harmonic	R_L = 100Ω	–68	–64	–62	–60	dBc	typ	C
	R_L ≥ 500Ω	–77	–70	–68	–66	dBc	typ	C
3rd-Harmonic	R_L = 100Ω	–70	–68	–66	–64	dBc	typ	C
	R_L ≥ 500Ω	–81	–78	–76	–75	dBc	typ	C
Input Voltage Noise	f > 1MHz	5.5				$nV/\sqrt{Hz}$	typ	C
Input Current Noise	f > 1MHz	3.1				$pA/\sqrt{Hz}$	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, R_L = 150	0.06				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, R_L = 150	0.03				deg	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, R_L = 100Ω	69	**58**	56	54	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±1.0	**±4**	±4.5	±4.7	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±10	±10	μV/°C	max	B
Input Bias Current	V_{CM} = 0V	+3	**±8**	±9	±11	μA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 0V			±20	±40	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.1	**±1.0**	±1.4	±1.6	μA	max	A
Average Offset Current Drift	V_{CM} = 0V			±7	±9	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)(5)		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V	65	**60**	57	56	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0	190 || 0.6				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0	3.2 || 0.9				MΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing	V_O = 0	+190	**+160**	+140	+100	mA	min	A
Current Output, Sinking	V_O = 0	–190	**–160**	–140	–100	mA	min	A
Short-Circuit Current Limit	V_O = 0	±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.04				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–100	**–200**	–240	–260	μA	max	A
Disable Time	V_{IN} = $1V_{DC}$	200				ns	typ	C
Enable Time	V_{IN} = $1V_{DC}$	25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = 0	±50				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($V_{\overline{DIS}}$)	$V_{\overline{DIS}}$ = 0	75	**130**	150	160	μA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6.0**	±6	±6	V	max	A
Max Quiescent Current	V_S = ±5V	5.5	**5.8**	6.0	6.2	mA	max	A
Min Quiescent Current	V_S = ±5V	5.5	**5.3**	5.1	4.7	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	75	**68**	66	64	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range D, DBV Package		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction Temperature = Ambient for 25°C specifications. (2) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +10°C at high temperature limit for over temperature specifications. (3) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum CMRR specification at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C**.

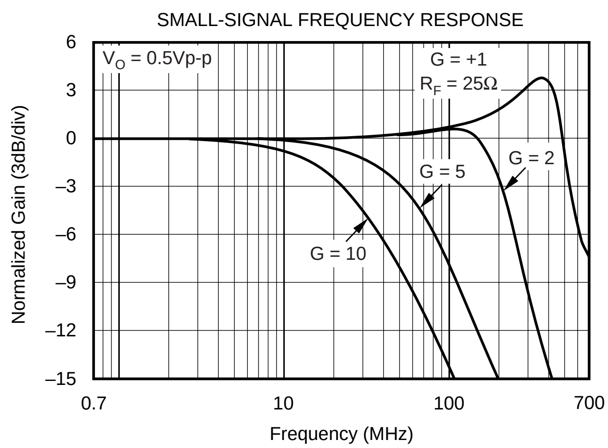
R_F = 402Ω, R_L = 100Ω, and G = +2, (see Figure 2 for AC performance only), unless otherwise noted.

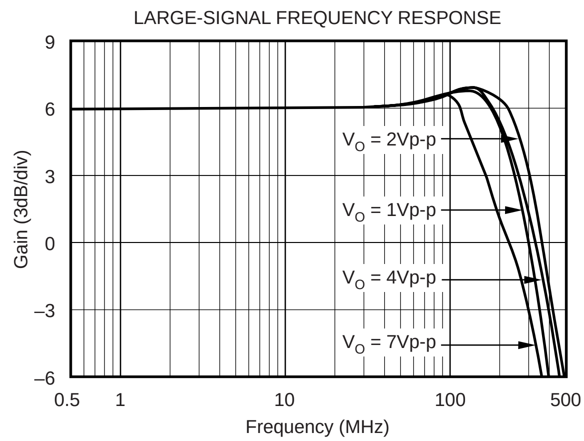
PARAMETER	CONDITIONS	OPA690ID, IDBV TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth	G = +1, V_O < 0.5Vp-p, R_F = ±25Ω	400				MHz	typ	C
	G = +2, V_O < 0.5Vp-p	190	150	145	140	MHz	typ	C
	G = +10, V_O < 0.5Vp-p	25	18	17	16	MHz	typ	C
Gain-Bandwidth Product	G ≥ 10	250	180	170	160	MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	20				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.5Vp-p	5				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2Vp-p	220				MHz	typ	C
Slew Rate	G = +2, 2V Step	1000	700	670	550	V/µs	typ	C
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.6				ns	typ	C
	G = +2, V_O = 2V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd-Harmonic	R_L = 100Ω to V_S/2	–65	–60	–59	–56	dBc	typ	C
	R_L ≥ 500Ω to V_S/2	–75	–70	–68	–66	dBc	typ	C
3rd-Harmonic	R_L = 100Ω to V_S/2	–68	–64	–62	–60	dBc	typ	C
	R_L ≥ 500Ω to V_S/2	–77	–73	–71	–70	dBc	typ	C
Input Voltage Noise	f > 1MHz	5.6				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	3.2				pA/√Hz	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, R_L = 150 to V_S/2	0.06				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, R_L = 150 to V_S/2	0.02				deg	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 2.5V, R_L = 100Ω to 2.5V	63	**56**	54	52	dB	min	A
Input Offset Voltage	V_{CM} = 2.5V	±1.0	**±4**	±4.3	±4.7	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±10	±10	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	+3	**±8**	±9	±11	µA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 2.5V			±20	±40	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±0.3	**±1**	±1.4	±1.6	µA	max	A
Average Offset Current Drift	V_{CM} = 2.5V			±7	±9	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.5	**1.6**	1.7	1.8	V	max	A
Most Positive Input Voltage(5)		3.5	**3.4**	3.3	3.2	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 2.5V ±0.5V	63	**58**	56	54	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 2.5V	92 || 1.4				kΩ || pF	typ	C
Common-Mode	V_{CM} = 2.5V	2.2 || 1.5				MΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4	**3.8**	3.6	3.5	V	min	A
	R_L = 100Ω to 2.5V	3.9	**3.7**	3.5	3.4	V	min	A
Least Positive Output Voltage	No Load	1	**1.2**	1.4	1.5	V	min	A
	R_L = 100Ω to 2.5V	1.1	**1.3**	1.5	1.7	V	max	A
Current Output, Sourcing		+160	**+120**	+100	+80	mA	max	A
Current Output, Sinking		–160	**–120**	–100	–80	mA	min	A
Short-Circuit Current		±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.04				Ω	typ	C
DISABLE (Disable LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–100	**–200**	–240	–260	µA	max	A
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±50				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($V_{\overline{DIS}}$)	$V_{\overline{DIS}}$ = 0	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			12	12	12	V	max	B
Max Quiescent Current	V_S = +5V	4.9	**5.2**	5.4	5.6	mA	max	A
Min Quiescent Current	V_S = +5V	4.9	**4.7**	4.4	4.0	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	72				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

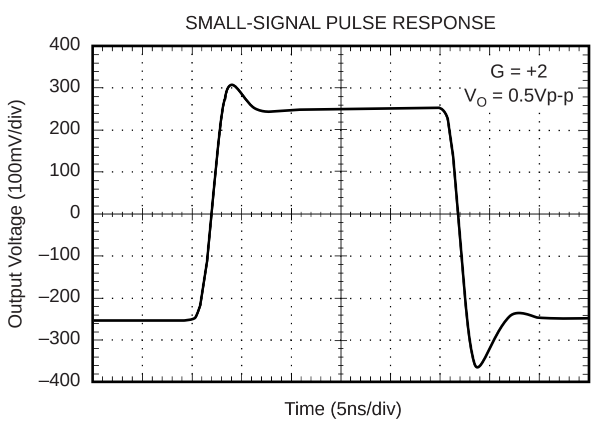
NOTES: (1) Junction Temperature = Ambient for 25°C tested specifications. (2) Junction Temperature = Ambient at low temperature limit: Junction Temperature = Ambient +10°C at high temperature limit for over temperature tested specifications. (3) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum CMRR specification at ±CMIR limits.

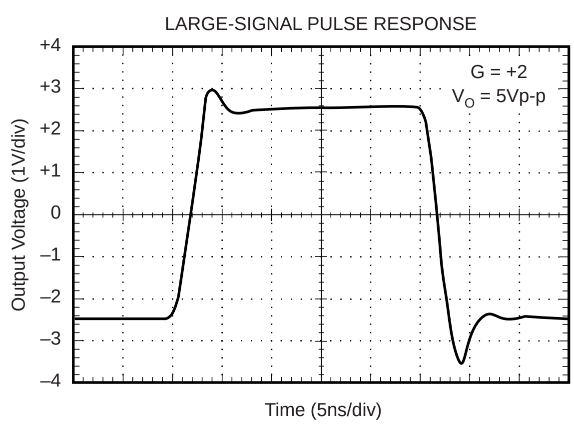
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

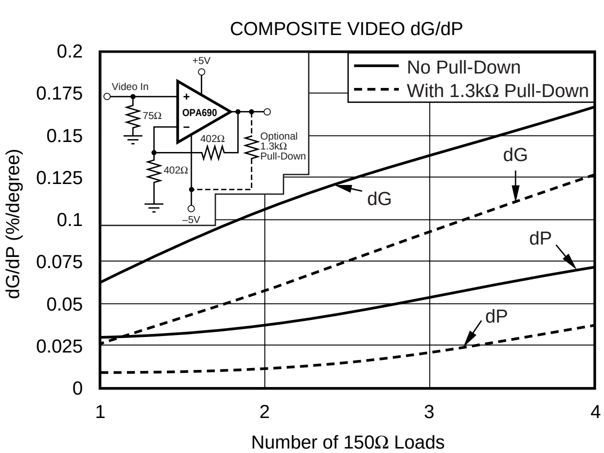
At $T_A = +25°C$, $G = +2$, $R_F = 402\Omega$, and $R_L = 100\Omega$, (see Figure 1 for AC performance only), unless otherwise noted.

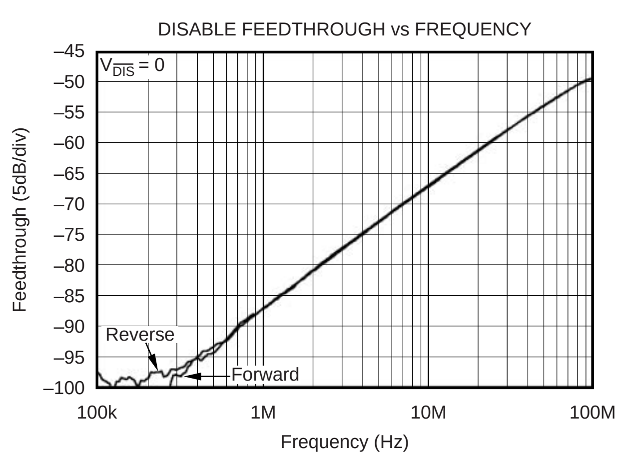




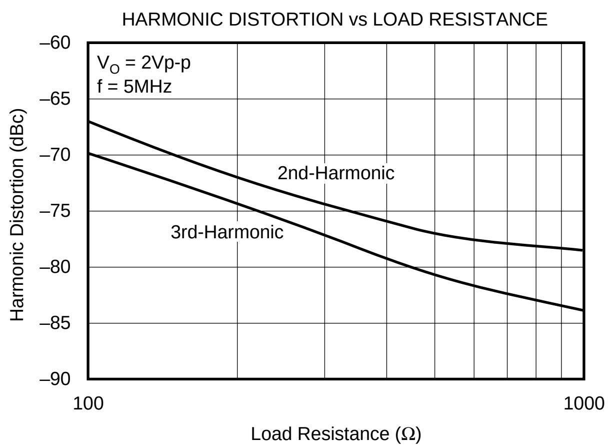


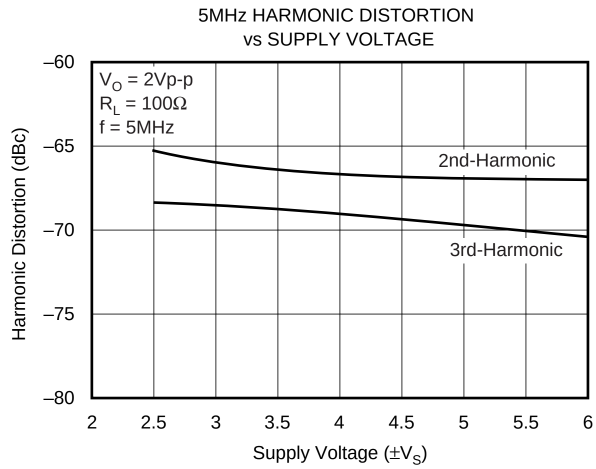


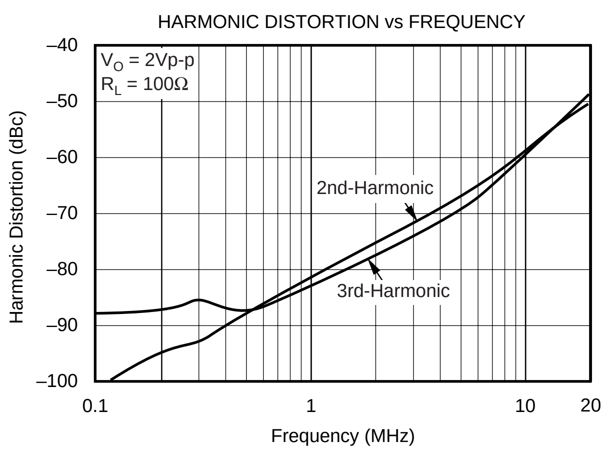


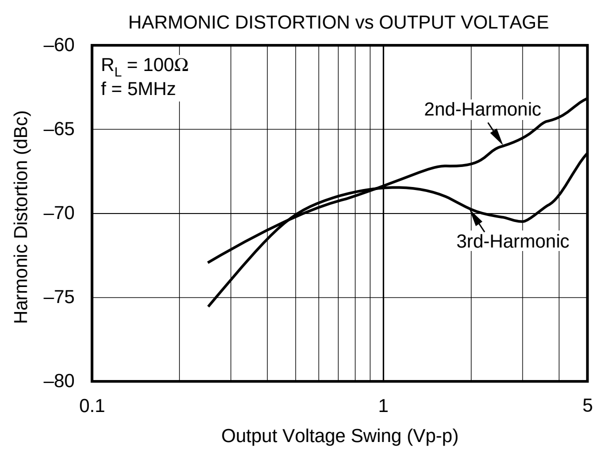


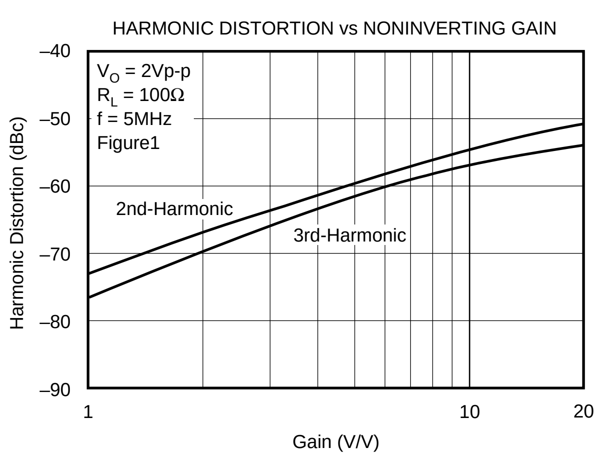
At $T_A = +25°C$, G = +2, $R_F = 402\Omega$, and $R_L = 100\Omega$, (see Figure 1 for AC performance only), unless otherwise noted.

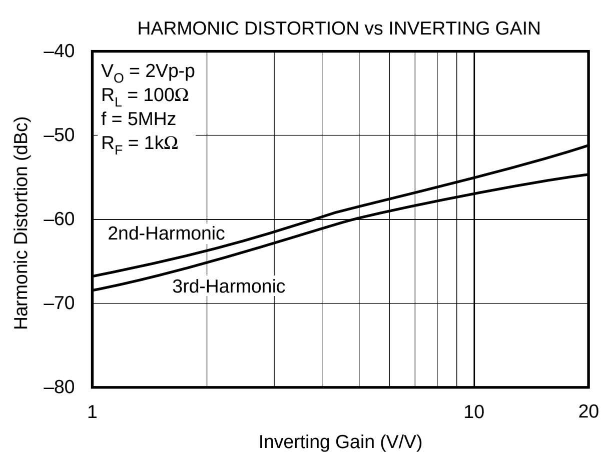






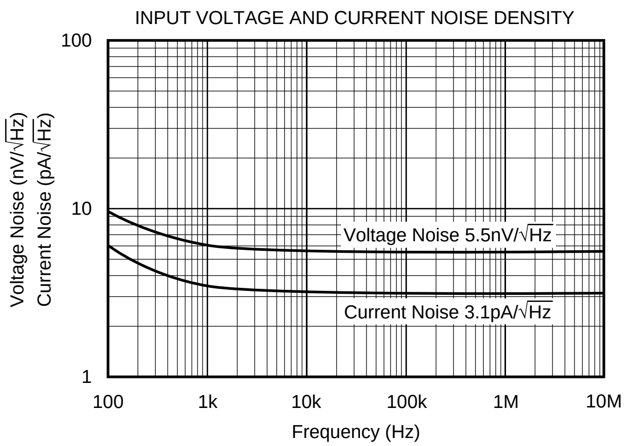


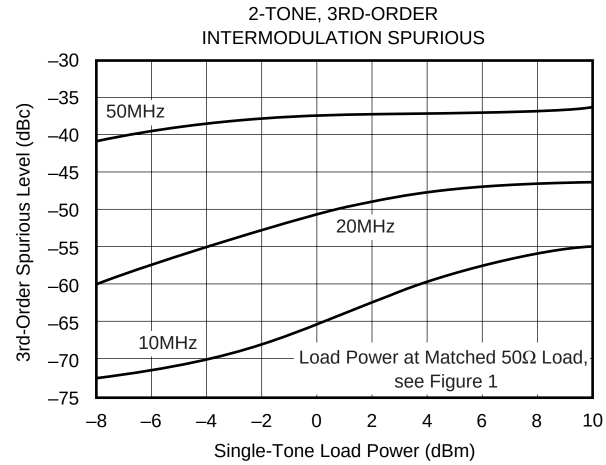


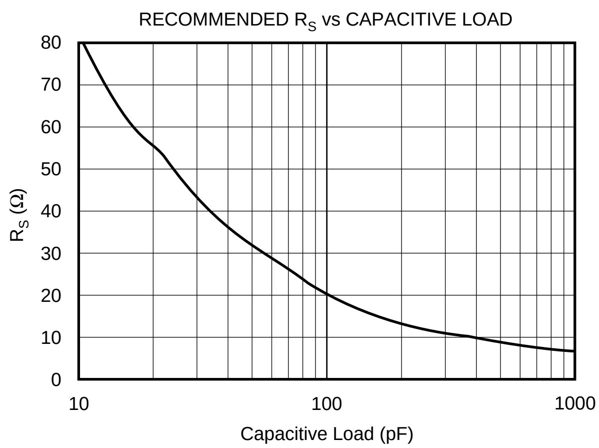


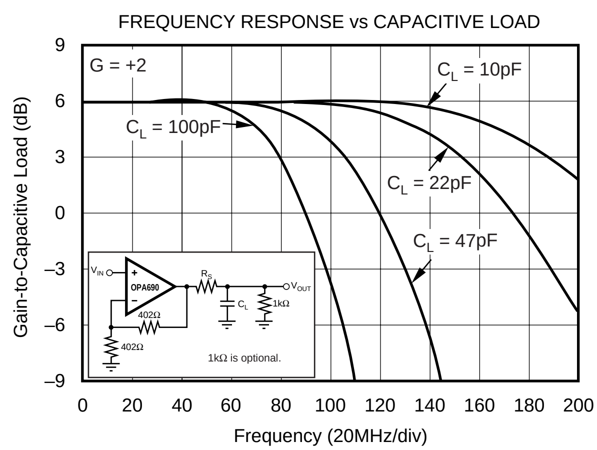
TYPICAL CHARACTERISTICS: $V_S = \pm5V$ (Cont.)

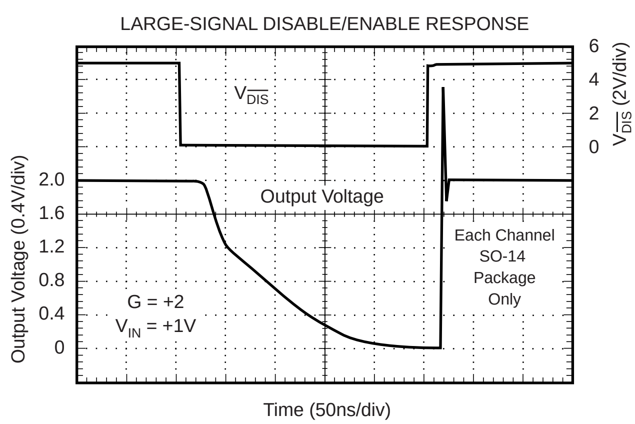
At $T_A = +25°C$, G = +2, $R_F = 402\Omega$, and $R_L = 100\Omega$, (see Figure 1 for AC performance only), unless otherwise noted.

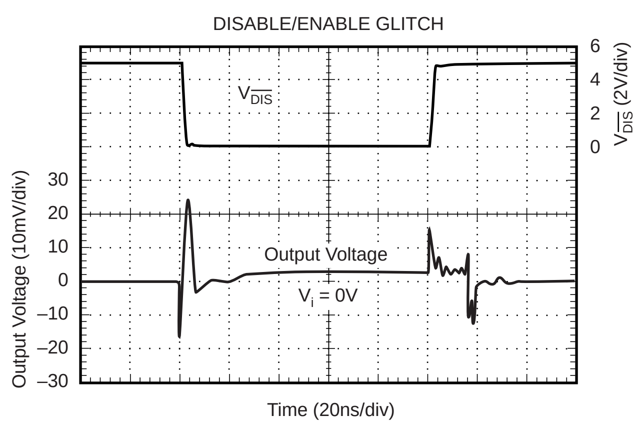






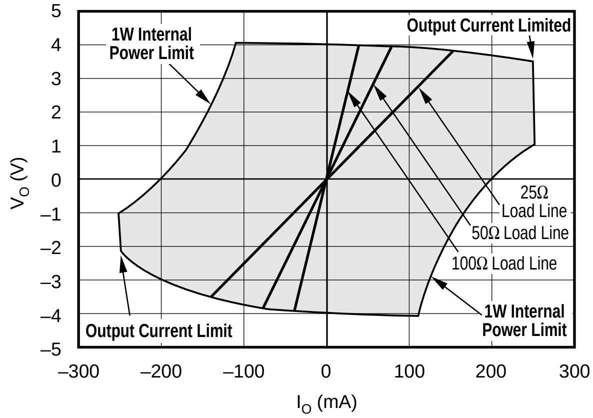




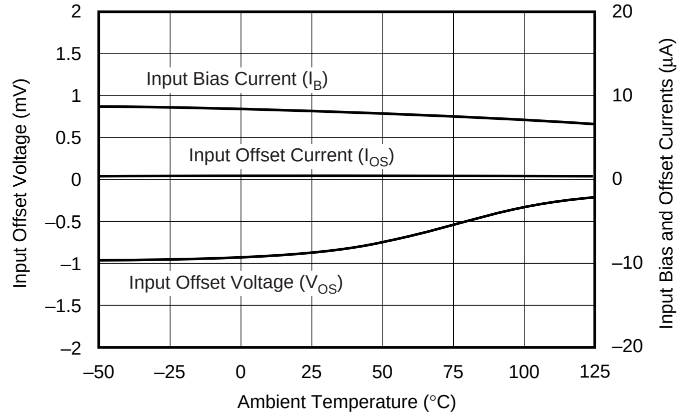


At $T_A = +25°C$, $G = +2$, $R_F = 402\Omega$, and $R_L = 100\Omega$, (see Figure 1 for AC performance only), unless otherwise noted.

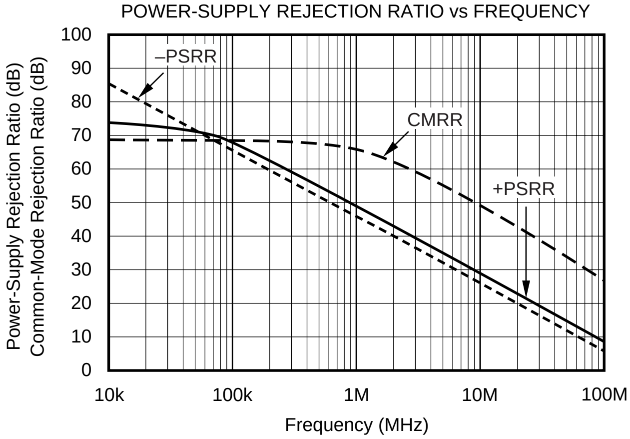
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



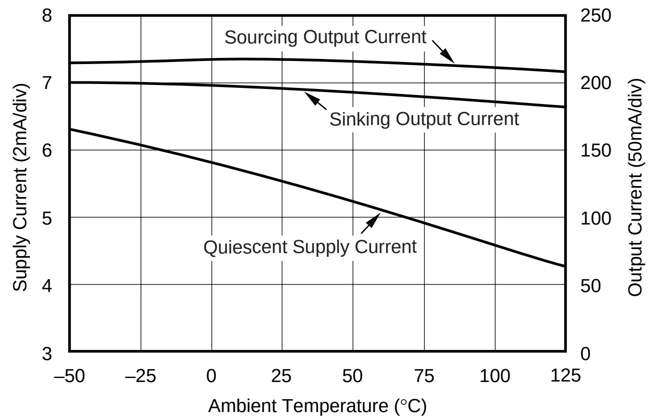
TYPICAL DC DRIFT OVER TEMPERATURE



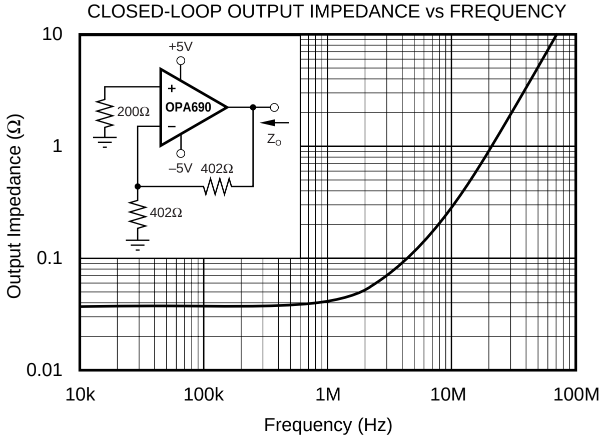
COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY



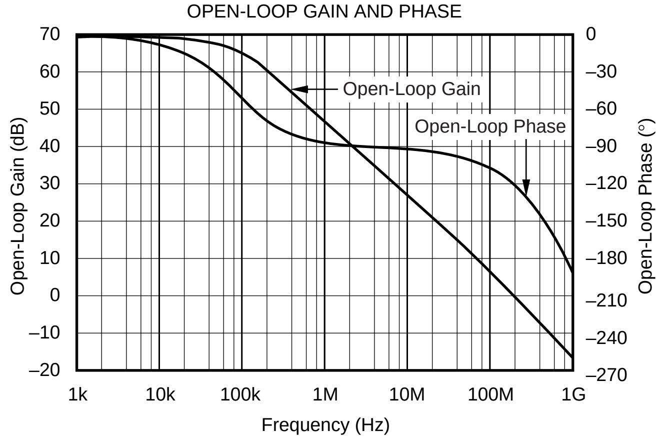
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



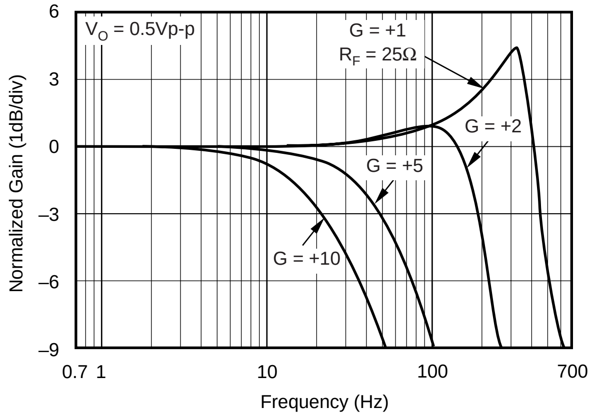
OPEN-LOOP GAIN AND PHASE



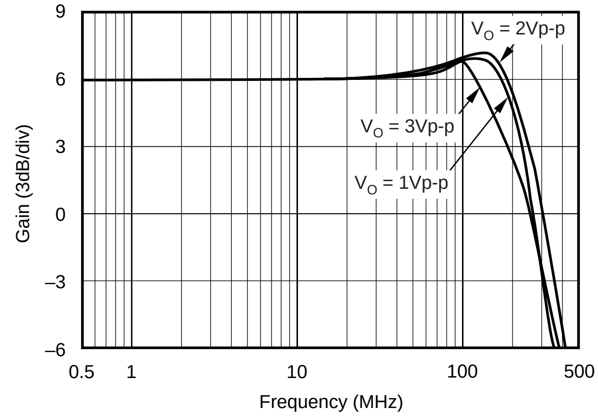
TYPICAL CHARACTERISTICS: $V_S = +5V$

At $T_A = +25°C$, $G = +2$, $R_F = 402\Omega$, and $R_L = 100\Omega$, (see Figure 2 for AC performance only), unless otherwise noted.

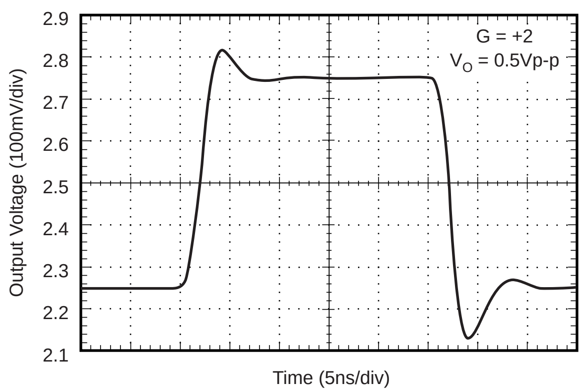
SMALL-SIGNAL FREQUENCY RESPONSE



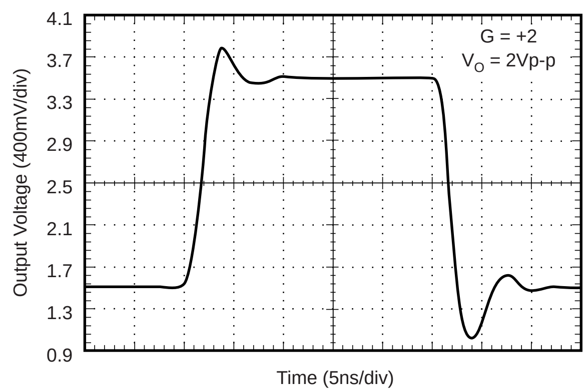
LARGE-SIGNAL FREQUENCY RESPONSE



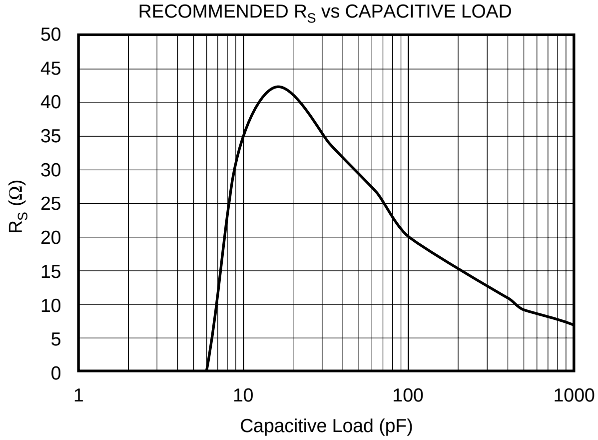
SMALL-SIGNAL PULSE RESPONSE



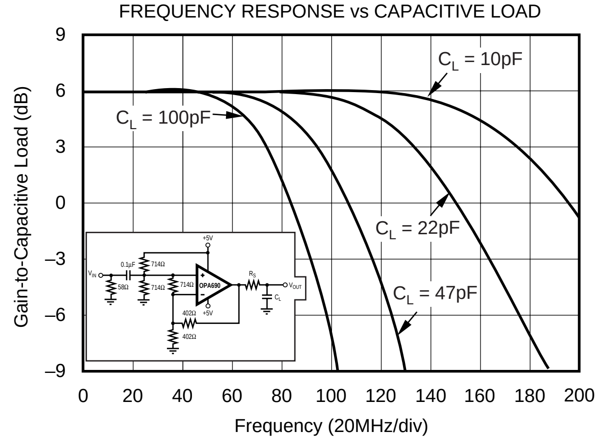
LARGE-SIGNAL PULSE RESPONSE



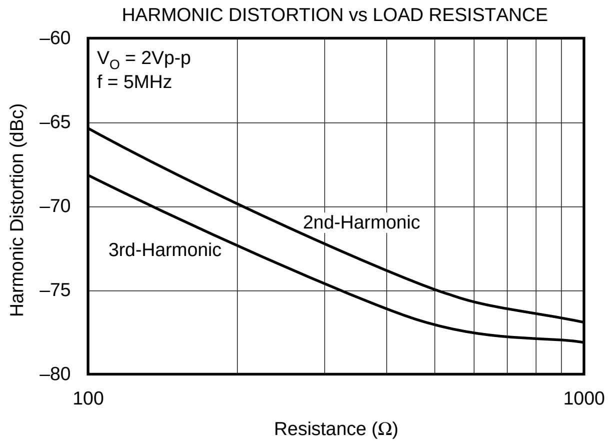
RECOMMENDED R_S vs CAPACITIVE LOAD

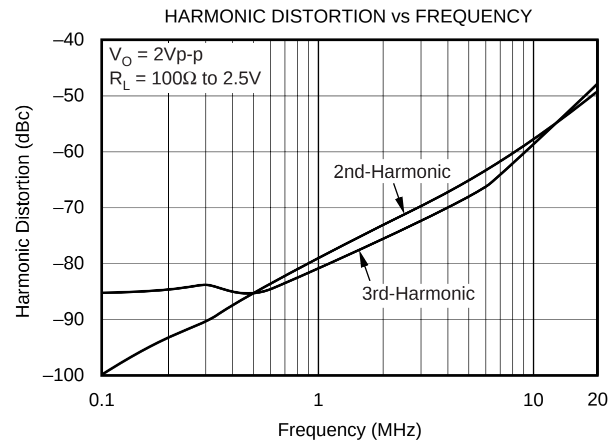


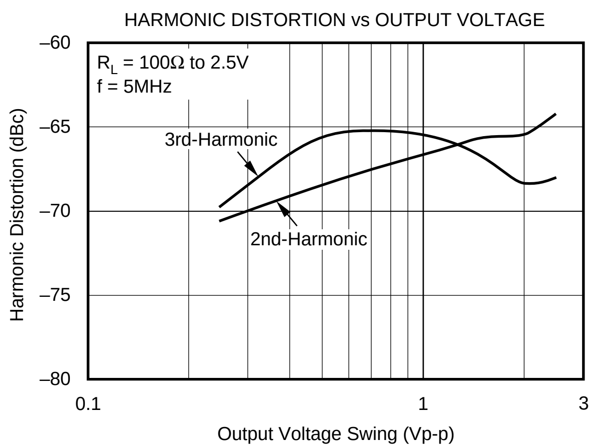
FREQUENCY RESPONSE vs CAPACITIVE LOAD

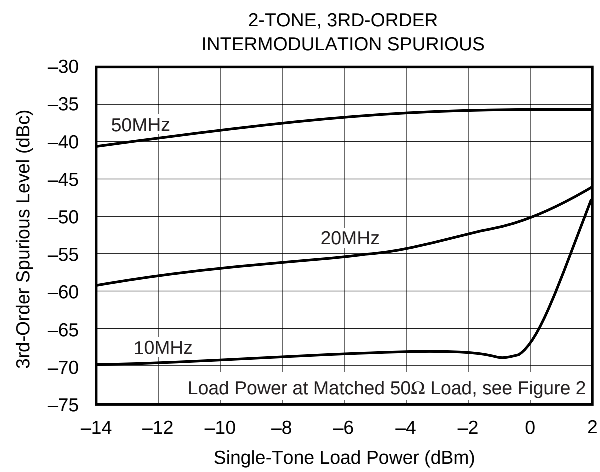


At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, (see Figure 2 for AC performance only), unless otherwise noted.









APPLICATIONS INFORMATION

WIDEBAND VOLTAGE FEEDBACK OPERATION

The OPA690 provides an exceptional combination of high output power capability with a wideband, unity-gain stable voltage feedback op amp using a new high slew rate input stage. Typical differential input stages used for voltage feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA690 uses a new input stage which places the transconductance element between two input buffers, using their output currents as the forward signal. As the error voltage increases across the two inputs, an increasing current is delivered to the compensation capacitor. This provides very high slew rate (1800V/µs) while consuming relatively low quiescent current (5.5mA). This exceptional full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures. The 5.5nV/$\sqrt{Hz}$ input voltage noise for the OPA690 is exceptionally low for this type of input stage.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 804Ω. The disable control line is typically left open to ensure normal amplifier operation. Two optional components are included in Figure 1. An additional resistor (175Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 200Ω source resistance seen at the inverting input (see the DC Accuracy and Offset Control section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1µF capacitor is included between the two power-supply pins. In practical PC board layouts, this optional-added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 2 shows the AC-coupled, gain of +2, single-supply circuit configuration which is the basis of the +5V Specifications and Typical Characteristics. Though not a “rail-to-rail” design, the OPA690 requires minimal input and output voltage headroom compared to other very wideband voltage feedback op amps. It will deliver a 3Vp-p output swing on a single +5V supply with > 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 698Ω resistors). The input signal is then AC-coupled into the midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a 2Vp-p input signal range centered between the supply pins. The input impedance matching resistor (59Ω) used for testing is adjusted to give a 50Ω input load when the parallel combination of the biasing divider network is included. Again, an additional resistor (50Ω in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the DC source resistance matching for the noninverting input bias current. It is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies (> 500MHz) using the input parasitic capacitance to form a bandlimiting pole. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the input DC bias voltage (2.5V) at the output as well. The output voltage can swing to within

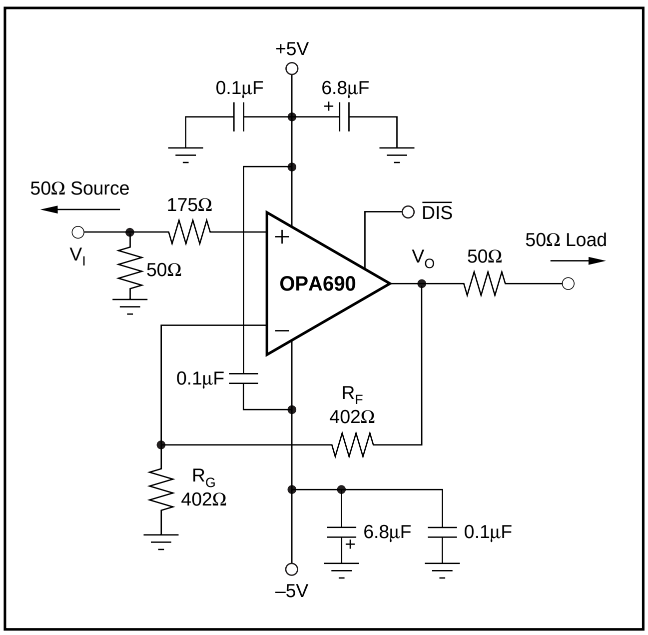


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

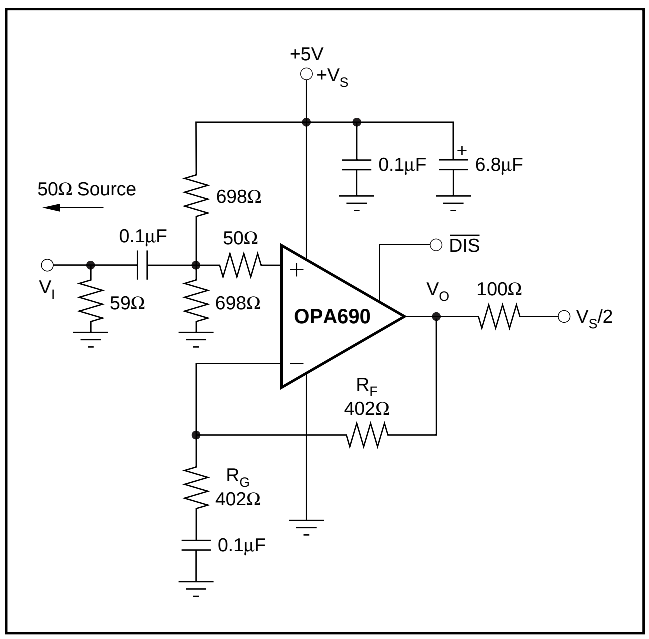


FIGURE 2. AC-Coupled, G = +2, Single-Supply, Specification and Test Circuit.

1V of either supply pin while delivering > 100mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage circuit used in the OPA690 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown in the +5V supply, 3rd-harmonic distortion plots.

SINGLE-SUPPLY ADC INTERFACE

Most modern, high performance ADC (such as the TI ADS8xx and ADS9xx series) operate on a single +5V (or lower) power supply. It has been a considerable challenge for single-supply op amps to deliver a low distortion input signal at the ADC input for signal frequencies exceeding 5MHz. The high slew rate, exceptional output swing, and high linearity of the OPA690 make it an ideal single-supply ADC driver. The circuit on the front page shows one possible (inverting) interface. Figure 3 shows the test circuit of Figure 2 modified for a capacitive (ADC) load and with an optional output pull-down resistor (R_B).

The OPA690 in the circuit of Figure 3 provides > 200MHz bandwidth for a 2Vp-p output swing. Minimal 3rd-harmonic distortion or 2-tone, 3rd-order intermodulation distortion will be observed due to the very low crossover distortion in the OPA690 output stage. The limit of output Spurious-Free Dynamic Range (SFDR) will be set by the 2nd-harmonic distortion. Without R_B, the circuit of Figure 3 measured at 10MHz shows an SFDR of 57dBc. This may be improved by pulling additional DC bias current (I_B) out of the output stage through the optional R_B resistor to ground (the output midpoint is at 2.5V for Figure 3). Adjusting I_B gives the improvement in SFDR shown in Figure 4. SFDR improvement is achieved for I_B values up to 5mA, with worse performance for higher values.

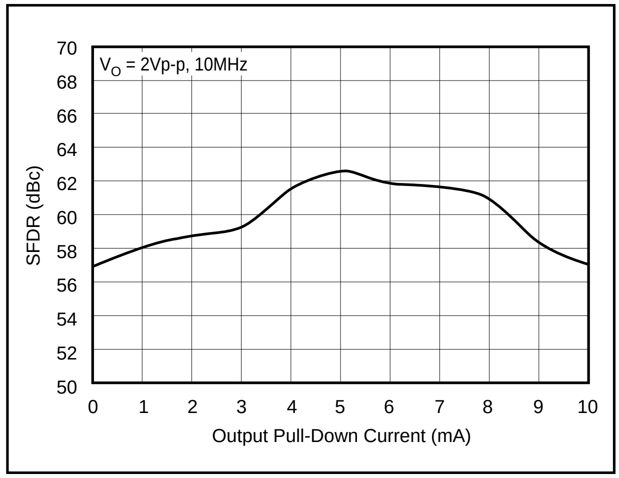


FIGURE 4. SFDR versus I_B.

HIGH-PERFORMANCE DAC TRANSIMPEDANCE AMPLIFIER

High-frequency DDS Digital-to-Analog Converters (DACs) require a low distortion output amplifier to retain their SFDR performance into real-world loads. See Figure 5 for a single-ended output drive implementation. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground summing junction of the OPA690, which is set up as a transimpedance stage or “I-V converter”. The unused current output of the DAC is connected to ground. If the DAC requires its outputs terminated to a compliance voltage other than ground for operation, the appropriate voltage level may be applied to the noninverting input of the OPA690. The

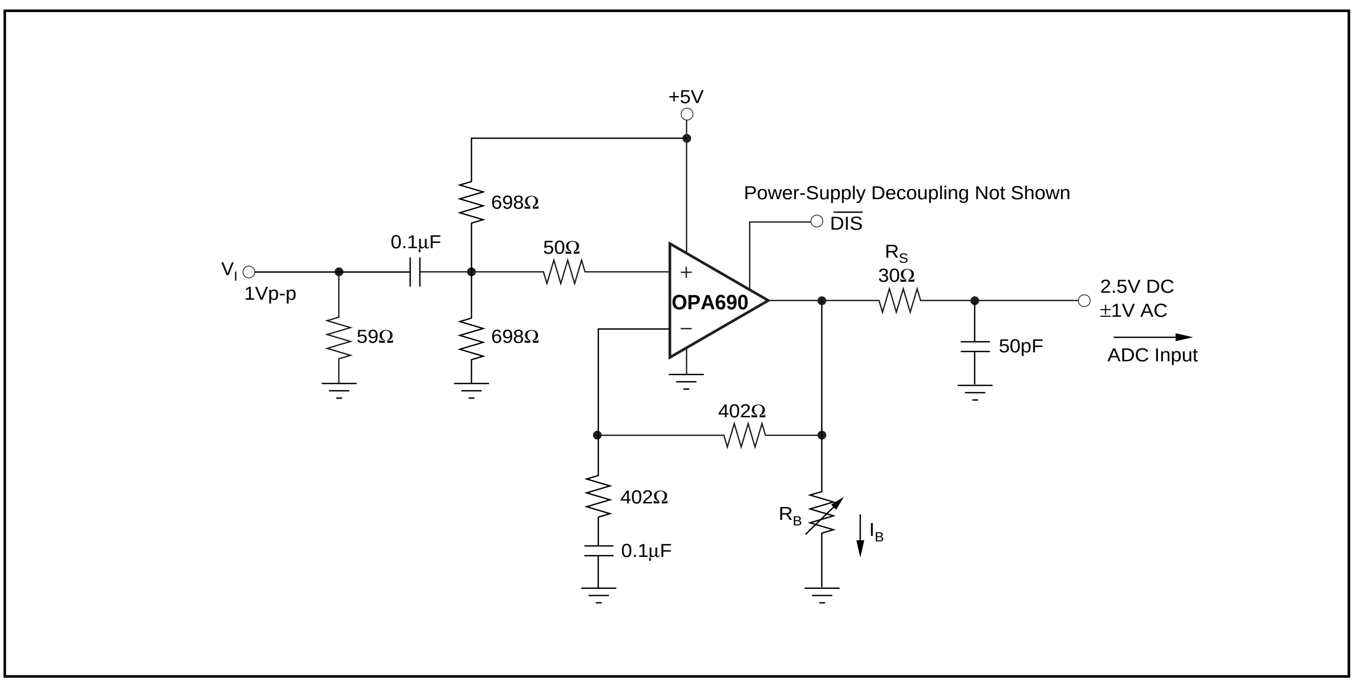


FIGURE 3. Single-Supply ADC Input Driver.

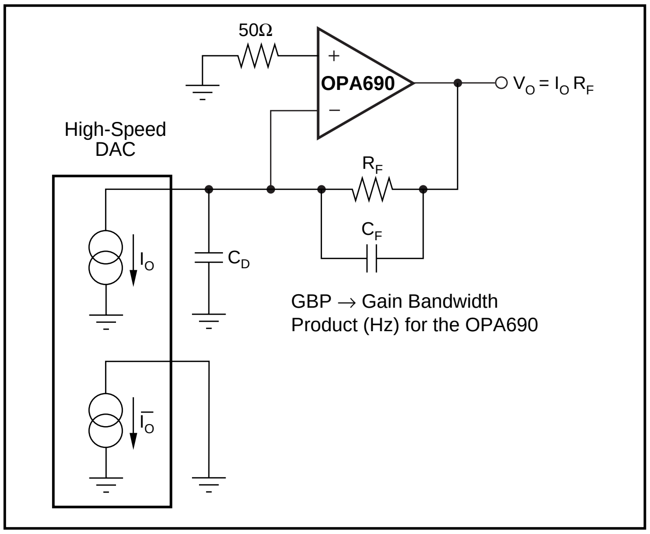


FIGURE 5. DAC Transimpedance Amplifier.

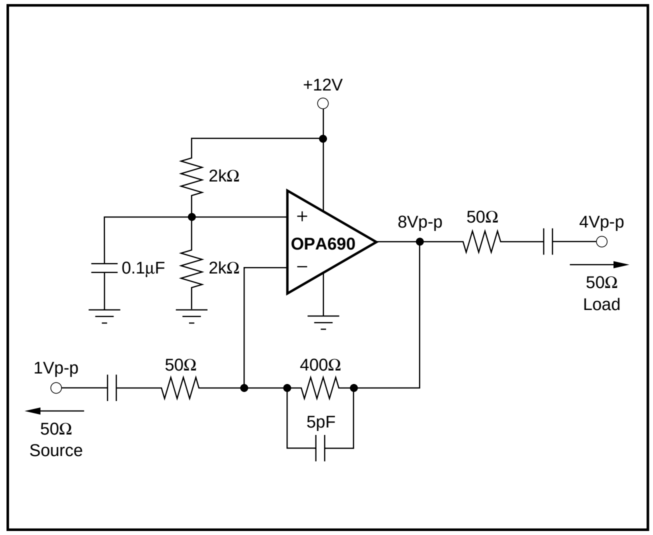


FIGURE 6. High Power Coax Line Driver.

DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance will produce a zero in the noise gain for the OPA690 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in the feedback network should be set to:

$$1/2\pi R_F C_F = \sqrt{GBP/4\pi R_F C_D}$$

which will give a closed-loop transimpedance bandwidth f_{-3dB}, of approximately:

$$f_{-3dB} = \sqrt{GBP/2\pi R_F C_D}$$

HIGH POWER LINE DRIVER

The large output swing capability of the OPA690 and its high current capability allows it to drive a 50Ω line with a peak-to-peak signal up to 4Vp-p at the load, or 8Vp-p at the output of the amplifier using a single 12V supply. Figure 6 shows such a circuit set for a gain of 8 to the output or 4 to the load.

The 5pF capacitor in the feedback loop provides added bandwidth control for the signal path.

SINGLE-SUPPLY ACTIVE FILTERS

The high bandwidth provided by the OPA690, while operating on a single +5V supply, lends itself well to high-frequency active filter designs. Again, the key additional requirement is to establish the DC operating point of the signal near the supply midpoint for highest dynamic range. Figure 7 shows an example design of a 5MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are AC-coupled using 0.1µF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 32kHz for the component values shown). As discussed for Figure 2, this allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The

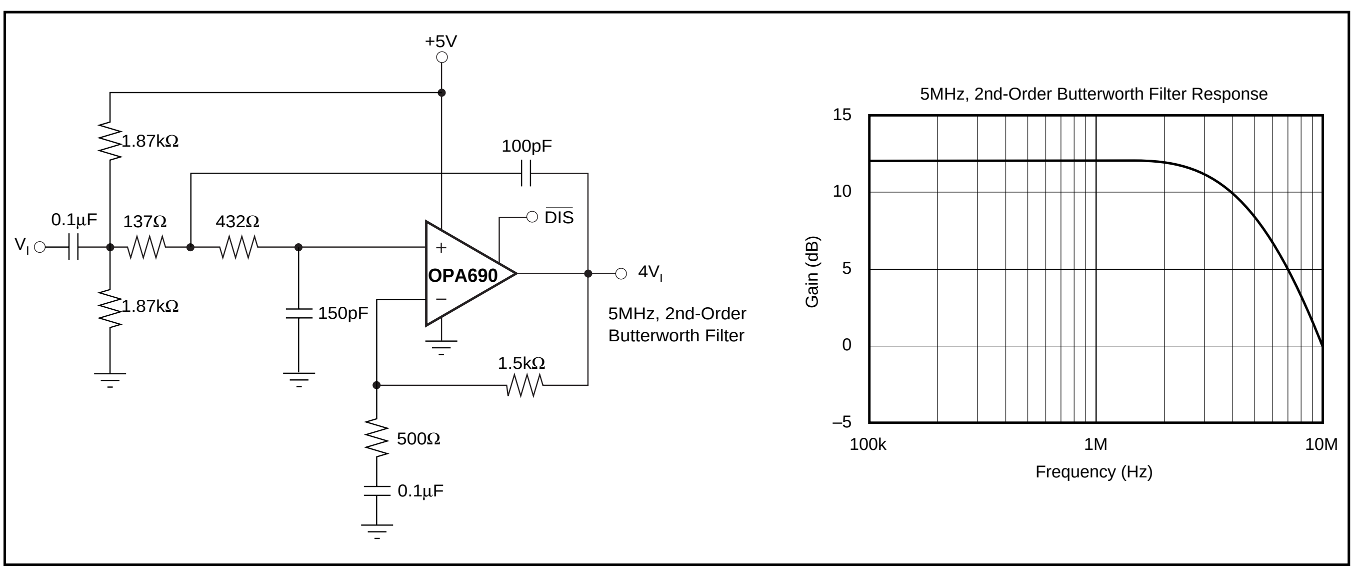


FIGURE 7. Single-Supply, High-Frequency Active Filter.

midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +4, the OPA690 on a single supply will show ~80MHz small- and large-signal bandwidth. The resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 5MHz, –3dB point with a maximally flat passband (above the 32kHz AC-coupling corner), and a maximum stopband attenuation of 36dB at the amplifier's –3dB bandwidth of 80MHz.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Several PC boards are available to assist in the initial evaluation of circuit performance using the OPA690 in its three package styles. All of these are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown below:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA690ID	SO-8	DEM-OPA68xU	SBOU009
OPA690IDBV	SOT23-6	DEM-OPA6xxN	SBOU010

The board can be requested on Texas Instruments' web site (www.ti.com.).

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA690 is available through the Texas Instruments internet web page (http://www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA690 is a unity-gain stable voltage feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short. This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, for G > 1 application, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA690. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 1) to be less than approximately 300Ω. The combined impedance $R_F \| R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus, a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \| R_G < 300\Omega$ will keep this pole above 250MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

BANDWIDTH VERSUS GAIN: NONINVERTING OPERATION

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factors), most amplifiers will exhibit a more complex response with lower phase margin. The OPA690 is compensated to give a slightly peaked response in a noninverting gain of 2 (see Figure 1). This results in a typical gain of +2 bandwidth of 220MHz, far exceeding that predicted by dividing the 300MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 30MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 300MHz.

Frequency response in a gain of +2 may be modified to achieve exceptional flatness simply by increasing the noise gain to 2.5. One way to do this, without affecting the +2 signal gain, is to add an 804Ω resistor across the two inputs in the circuit of Figure 1. A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 402Ω feedback resistor along with a 402Ω resistor across the two op amp inputs, the voltage follower response will be similar to the gain of +2 response of Figure 2. Further reducing the value of the resistor across the op amp inputs will further dampen the frequency response due to increased noise gain.

The OPA690 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

INVERTING AMPLIFIER OPERATION

Since the OPA690 is a general-purpose, wideband voltage feedback op amp, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. Figure 8 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

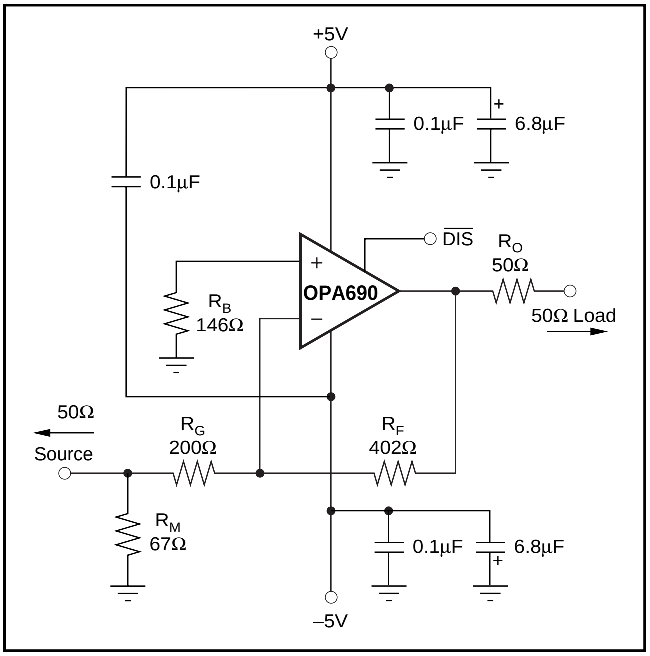


FIGURE 8. Gain of –2 Example Circuit.

In the inverting configuration, three key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PC board trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This has the interesting advantage that the noise gain becomes equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered above. However, the amplifier output will now see the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values, as shown in Figure 8, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For the example in Figure 8, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 67Ω = 28.6Ω. This impedance is added in series with R_G for calculating the noise gain (NG). The resultant NG is 2.8 for Figure 8, as opposed to only 2 if R_M could be eliminated as discussed above. The bandwidth will therefore be slightly lower for the gain of –2 circuit of Figure 8 than for the gain of +2 circuit of Figure 1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC error, due to the input bias currents, will be reduced to (Input Offset Current) • R_F. If the 50Ω source impedance is DC-coupled in Figure 8, the total resistance to ground on the inverting input will be 228Ω. Combining this in parallel with the feedback resistor gives the R_B = 146Ω used in this example. To reduce the additional high frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as R_B < 350Ω, the capacitor is not required since the total noise contribution of all other terms will be less than that of the op amp's input noise voltage. As a minimum, the OPA690 requires an R_B value of 50Ω to damp out parasitic-induced peaking—a direct short to ground on the noninverting input runs the risk of a very high frequency instability in the input stage.

OUTPUT CURRENT AND VOLTAGE

The OPA690 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1V to either supply rail; the tested swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±160mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the "Output Voltage and Current Limitations" plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA690's output drive capabilities, noting that the graph is bounded by a "Safe Operating Area" of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA690 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the typical specifications.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the tested tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}'s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To protect the output stage from accidental shorts to ground and the power supplies, output short-circuit protection is included in the OPA690. The circuit acts to limit the maximum source or sink current to approximately 250mA.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA690 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA690. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA690 output pin (see Board Layout Guidelines).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA690 operating in a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will reduce the peaking as described previously. The circuit of Figure 9 demonstrates this technique, allowing lower values of R_S to be used for a given capacitive load.

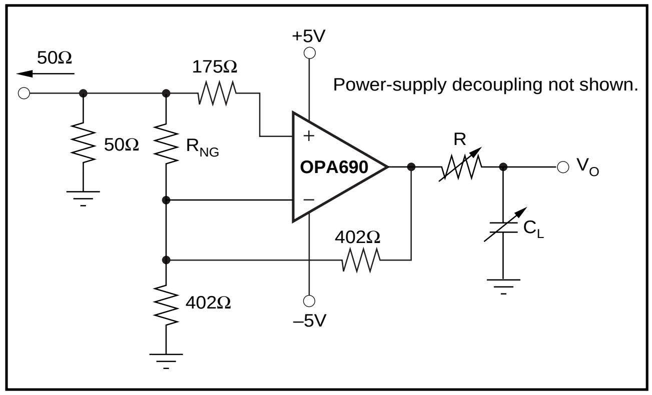


FIGURE 9. Capacitive Load Driving with Noise Gain Tuning.

This gain of +2 circuit includes a noise gain tuning resistor across the two inputs to increase the noise gain, increasing the unloaded phase margin for the op amp. Although this technique will reduce the required R_S resistor for a given capacitive load, it does increase the noise at the output. It also will decrease the loop gain, slightly decreasing the distortion performance. If, however, the dominant distortion mechanism arises from a high R_S value, significant dynamic range improvement can be achieved using this technique. Figure 10 shows the required R_S versus C_{LOAD} parametric on noise gain using this technique. This is the circuit of Figure 9 with R_{NG} adjusted to increase the noise gain (increasing the phase margin) then sweeping C_{LOAD} and finding the required R_S to get a flat frequency response. This plot also gives the required R_S versus C_{LOAD} for the OPA690 operated at higher signal gains.

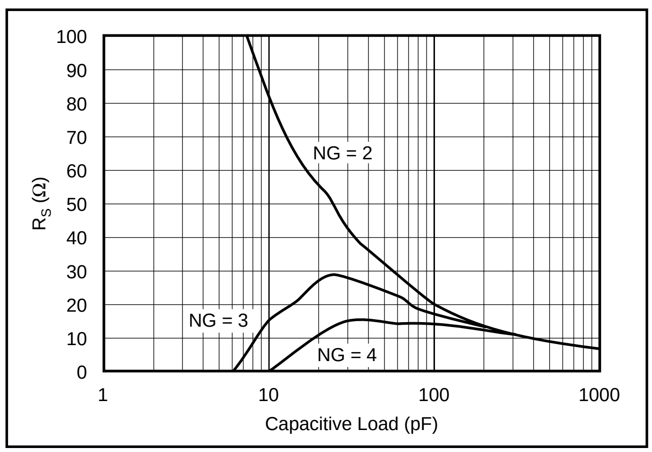


FIGURE 10. Required R_S vs Noise Gain.

DISTORTION PERFORMANCE

The OPA690 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 1) this is sum of R_F + R_G, while in the inverting configuration, it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The new output stage used in the OPA690 actually holds the difference between fundamental power and the 2nd- and 3rd-harmonic powers relatively constant with increasing output power until very large output swings are required (> 4Vp-p). This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are moderately low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (i.e., 2Vp-p for each tone at the load, which requires 8Vp-p for the overall 2-tone envelope at the output pin), the Typical Characteristics show 47dBc difference between the test tone powers and the 3rd-order intermodulation spurious powers. This performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 5.5nV/$\sqrt{Hz}$ input voltage noise for the OPA690 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 11 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

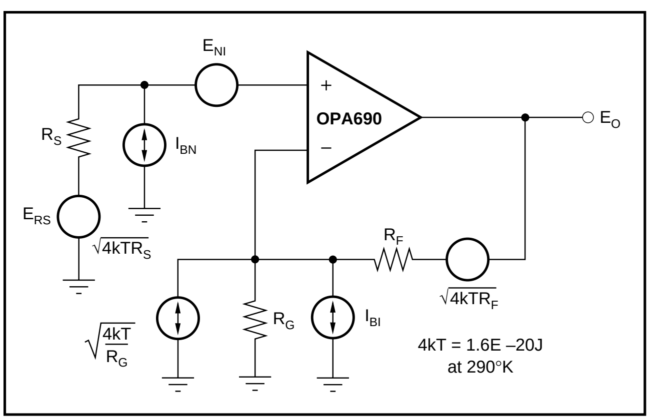


FIGURE 11. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 11.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 2.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating these two equations for the OPA690 circuit and component values (see Figure 1) will give a total output spot noise voltage of 12.3nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 6.1nV/$\sqrt{Hz}$. This is including the noise added by the bias current cancellation resistor (175Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 5.5nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 300Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300Ω will satisfy both noise and frequency response flatness considerations. Since the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 8 is not required.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage feedback op amp allows good output DC accuracy in a wide variety of applications. The power-supply current trim for the OPA690 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically ±8µA at each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. The total output offset voltage may be considerably reduced by matching the DC source resistances appearing at the two inputs. This reduces the output DC error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to: – (NG = noninverting signal gain)

±(NG • $V_{OS(MAX)}$) ± (R_F • $I_{OS(MAX)}$)

= ±(2 • 4mV) ± (402Ω • 1µA)

= ±8.4mV

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques eventually reduce to adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the DC offset voltage on the summing junction will set up a DC current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 12 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the DC offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

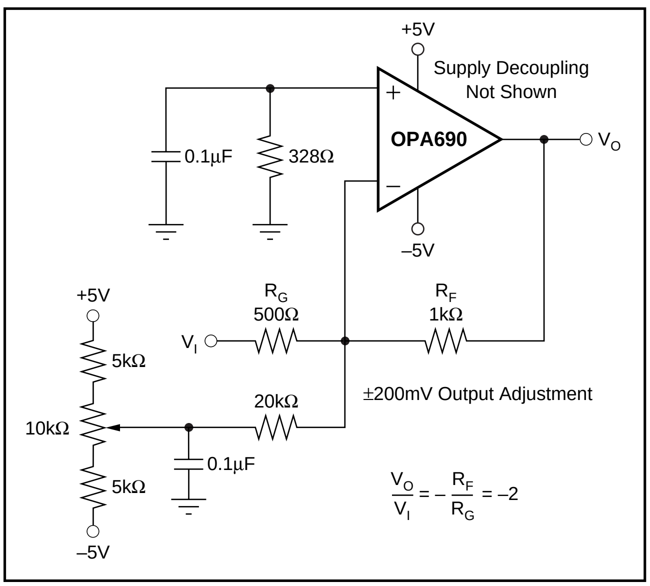


FIGURE 12. DC-Coupled, Inverting Gain of –2, with Offset Adjustment.

DISABLE OPERATION

The OPA690 provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA690 will operate normally. To disable, the control pin must be asserted LOW. Figure 13 shows a simplified internal circuit for the disable control feature.

In normal operation, base current to Q1 is provided through the 110kΩ resistor, while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled

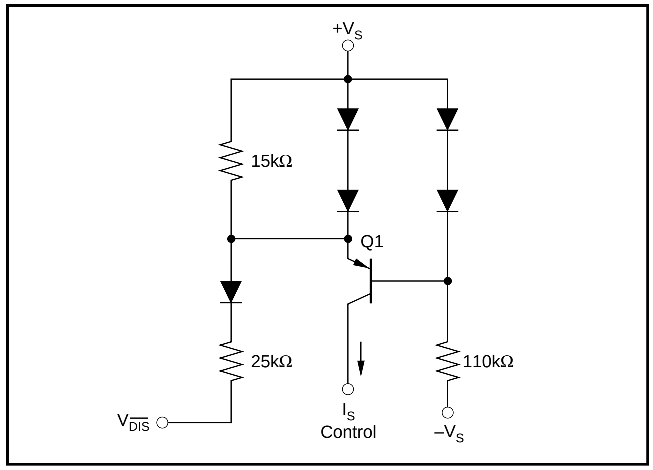


FIGURE 13. Simplified Disable Control Circuit.

LOW, additional current is pulled through the 15kΩ resistor, eventually turning on those two diodes (≈75µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 13. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high impedance state. If the OPA690 is operating in a gain of +1, this will show a very high impedance at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) and the isolation will be very poor as a result.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. Figure 14 shows these glitches for the circuit of Figure 1 with the input signal at 0V. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

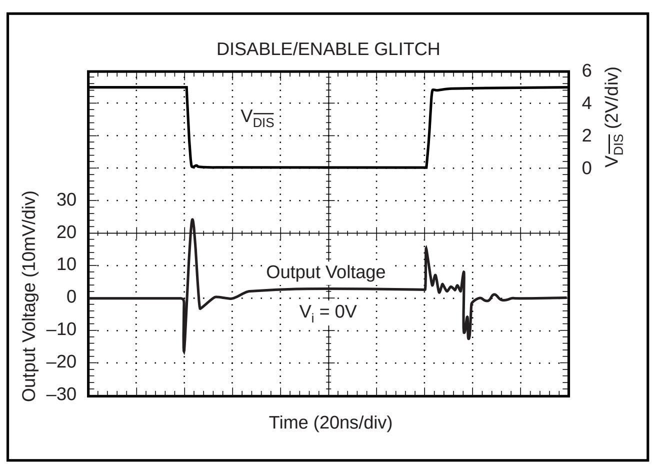


FIGURE 14. Disable/Enable Glitch.

The transition edge rate (dv/dt) of the $\overline{\text{DIS}}$ control line will influence this glitch. For the plot of Figure 14, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate may be achieved by adding a simple RC filter into the $\overline{\text{DIS}}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 1kΩ series resistor between the logic gate and the $\overline{\text{DIS}}$ input pin will provide adequate bandlimiting using just the parasitic input capacitance on the $\overline{\text{DIS}}$ pin while still ensuring adequate logic level swing.

THERMAL ANALYSIS

Due to the high output power capability of the OPA690, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA690IDBV (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load.

$P_D = 10V \bullet 6.2mA + 5^2/(4 \bullet (20\Omega \;||\; 804\Omega)) = 382mW$

Maximum $T_J = +85°C + (0.38W \bullet 150°C/W) = 142°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The output V-I plot shown in the Typical Characteristics include a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA690 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) **Careful selection and placement of external components will preserve the high-frequency performance of the OPA690.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402Ω feedback used in the Electrical Characteristics is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for the unity-gain follower application. This effectively isolates the inverting input capacitance from the output pin that would otherwise cause an additional peaking in the gain of +1 frequency response.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA690 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA690 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA690 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of "Recommended R_S vs Capacitive Load". This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high-speed part like the OPA690 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA690 onto the board.

INPUT AND ESD PROTECTION

The OPA690 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 15.

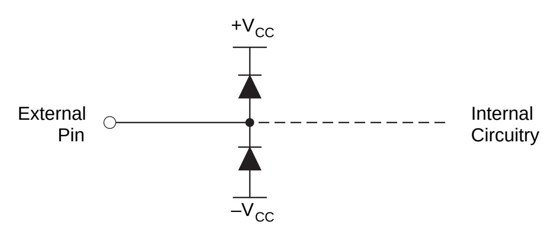
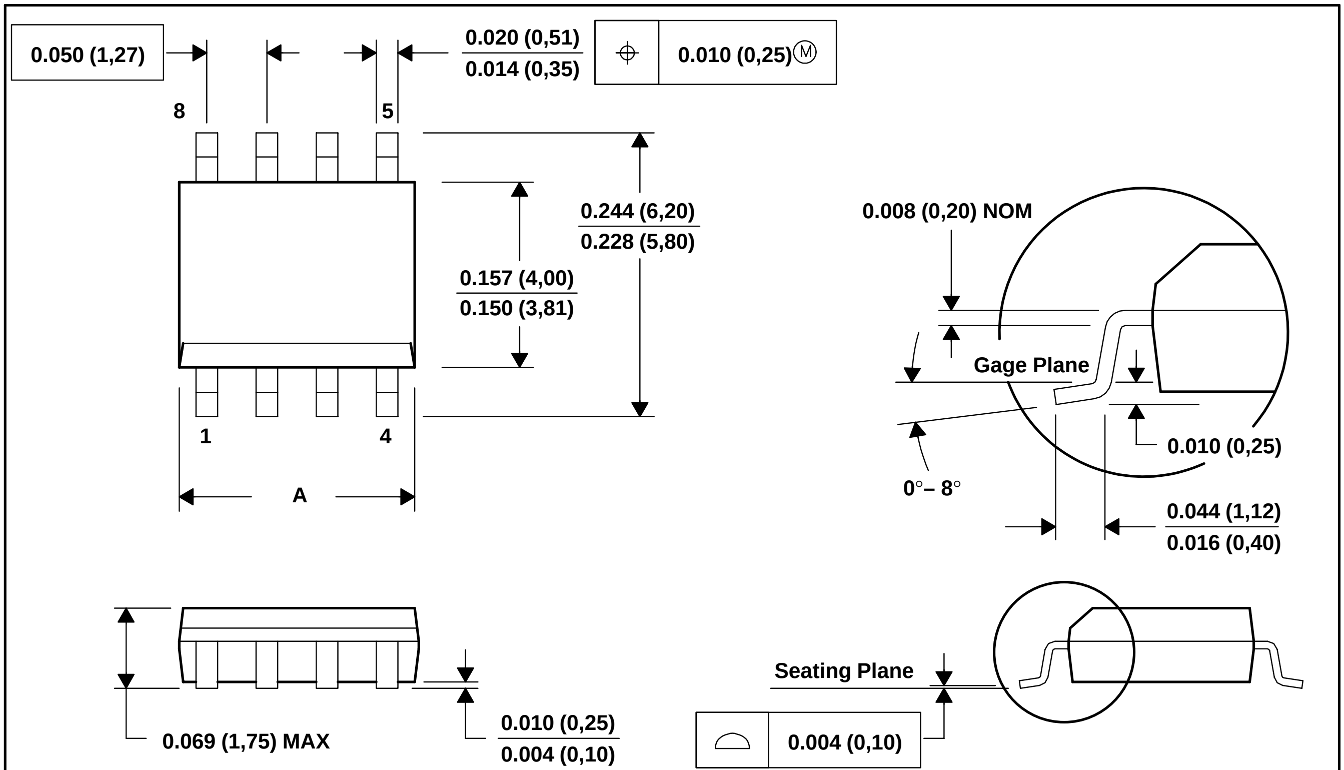


FIGURE 15. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA690), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

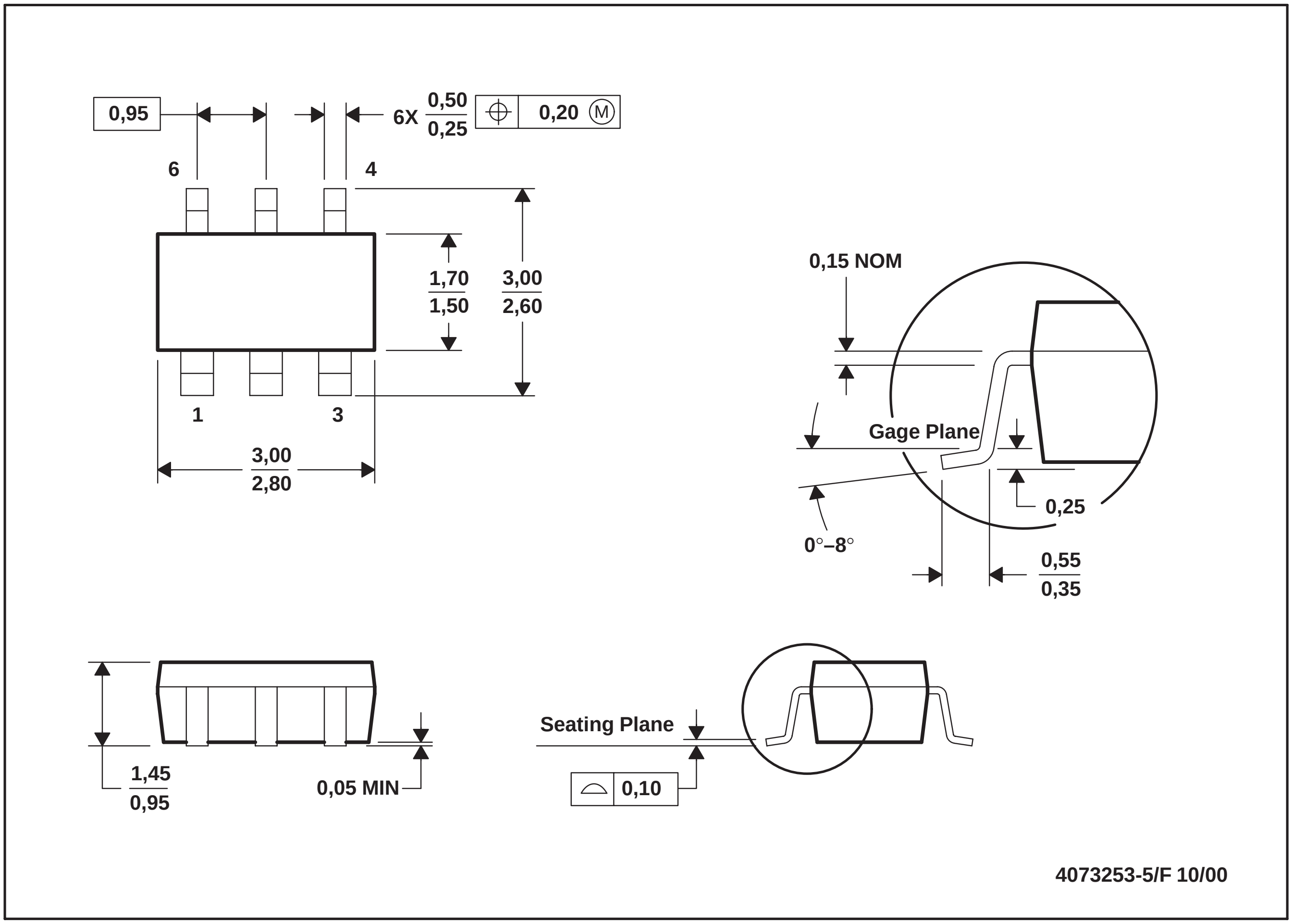


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 are wider than leads 4, 5, 6 for package orientation.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
OPA690ID	ACTIVE	SOIC	D	8	100
OPA690IDBVR	ACTIVE	SOP	DBV	6	3000
OPA690IDBVT	ACTIVE	SOP	DBV	6	250
OPA690IDR	ACTIVE	SOIC	D	8	2500

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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