

HD74HCT374/HD74HCT534

Octal D-type Flip-Flops (with 3-state outputs)/
Octal D-type Flip-Flops (with inverted 3-state outputs)

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Description

These devices are positive edge triggered flip-flops. The difference between HD74HCT374 and HD74HCT534 is only that the former is a true outputs and the latter is a false outputs. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the clock (CK) input. When a high logic level is applied to the output control (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Clock to Q) = 15 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Output Control	Clock	D	HD74HCT374 Q	HD74HCT534 \overline{Q}
L		H	H	L
L		L	L	H
L	L	X	No change	No change
H	X	X	Z	Z

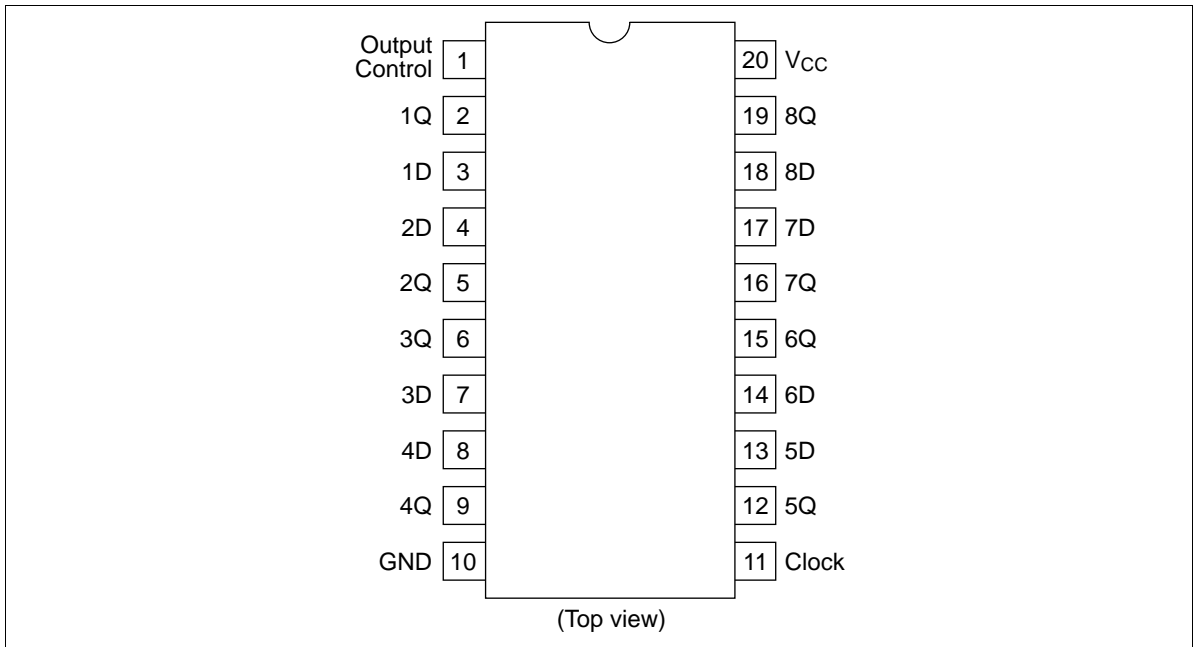
X : Irrelevant

Z : Off (high-impedance) state of a 3-state output.

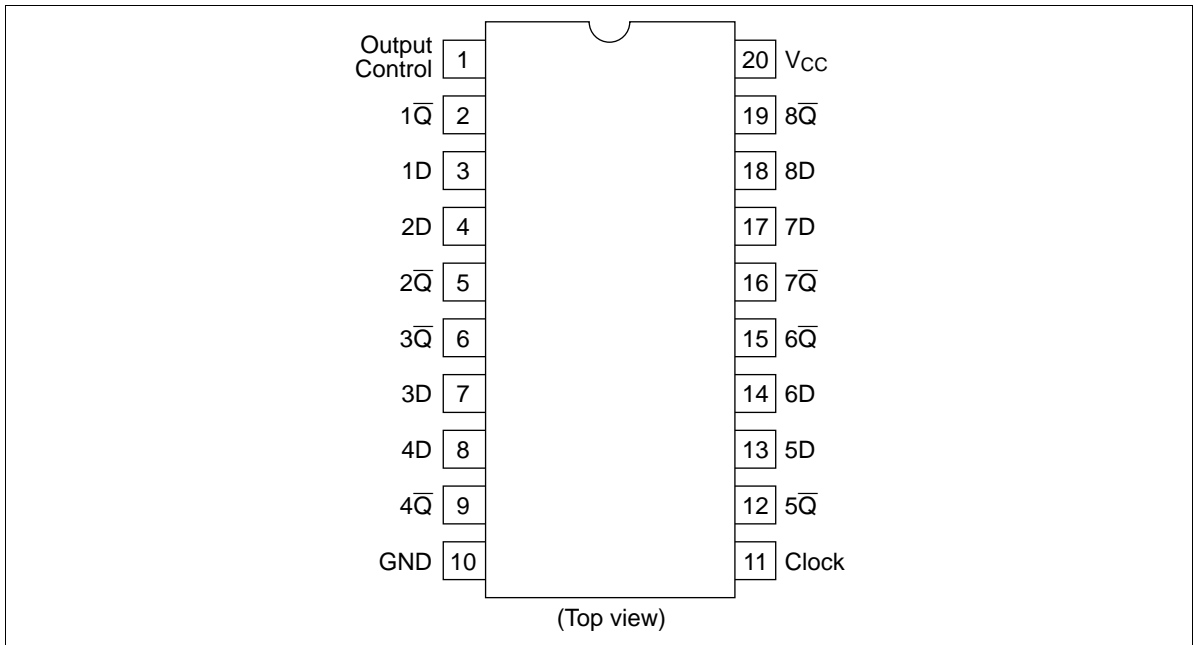
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Pin Arrangement

HD74HCT374



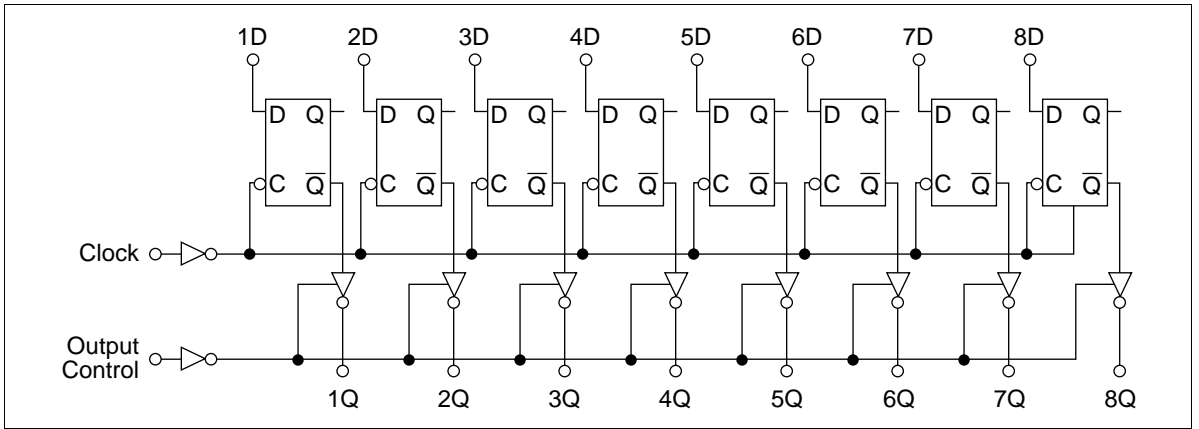
HD74HCT534



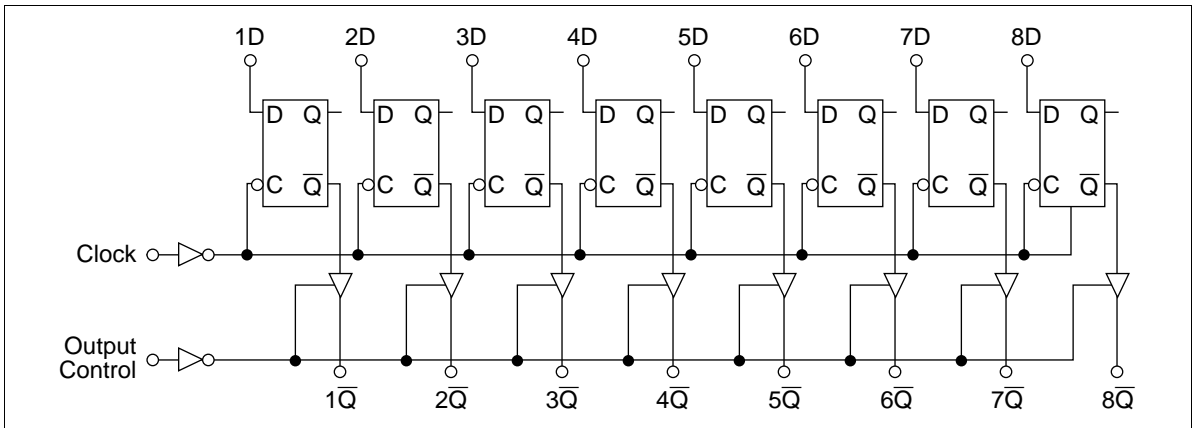
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Block Diagram

HD74HCT374



HD74HCT534



HD74HCT374/HD74HCT534

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC current drain per pin	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

DC Characteristics

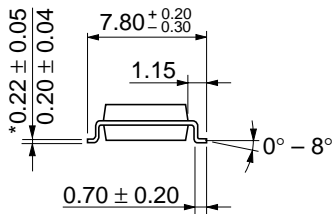
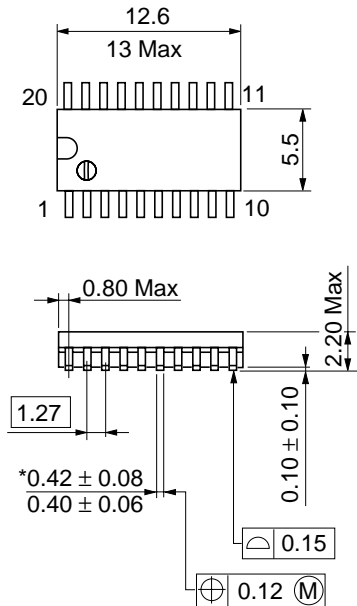
Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
		Min	Typ	Max	Min		Max	V_{CC} (V)	
Input voltage	V_{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5	
	V_{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5	
Output voltage	V_{OH}	4.4	—	—	4.4	—	V	4.5	$V_{in} = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu A$
		4.18	—	—	4.13	—		4.5	$I_{OH} = -6 \text{ mA}$
	V_{OL}	—	—	0.1	—	0.1	V	4.5	$V_{in} = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu A$
		—	—	0.26	—	0.33		4.5	$I_{OL} = 6 \text{ mA}$
Off-state output current	I_{OZ}	—	—	± 0.5	—	± 5.0	μA	5.5	$V_{in} = V_{IH}$ or V_{IL} , $V_{out} = V_{CC}$ or GND
Input current	I_{in}	—	—	± 0.1	—	± 1.0	μA	5.5	$V_{in} = V_{CC}$ or GND
Quiescent current	I_{CC}	—	—	4.0	—	40	μA	5.5	$V_{in} = V_{CC}$ or GND, $I_{out} = 0 \mu A$

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
		Min	Typ	Max	Min		Max	V _{cc} (V)	
Maximum clock frequency	f _{max}	—	—	30	—	24	MHz	4.5	
Propagation delay time	t _{PLH}	—	12	28	—	35	ns	4.5	
	t _{PHL}	—	15	28	—	35		4.5	
Output enable time	t _{ZL}	—	16	30	—	38	ns	4.5	
	t _{ZH}	—	15	30	—	38		4.5	
Output disable time	t _{LZ}	—	13	30	—	38	ns	4.5	
	t _{HZ}	—	16	30	—	38		4.5	
Setup time	t _{su}	20	2	—	25	—	ns	4.5	Data to clock
Hold time	t _h	5	0	—	6	—	ns	4.5	Clock to data
Pulse width	t _w	16	5	—	20	—	ns	4.5	Clock, output control
Output rise/fall time	t _{TLH}	—	4	12	—	15	ns	4.5	
	t _{THL}								
Input capacitance	C _{in}	—	5	10	—	10	pF	—	

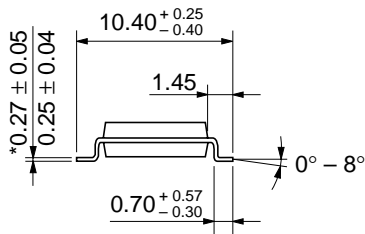
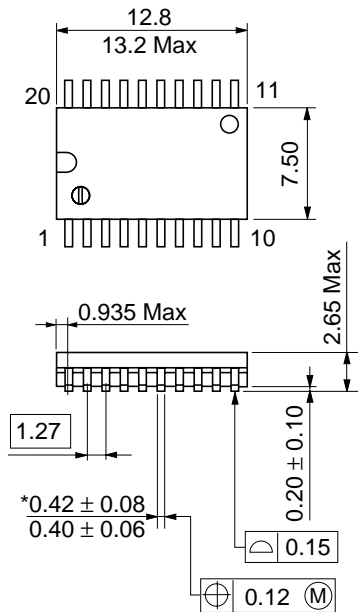


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



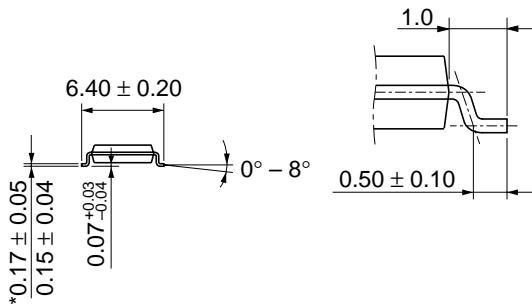
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
 Base material dimension



Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

*Dimension including the plating thickness
Base material dimension

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