

200-mA LOW-NOISE, HIGH-PSRR NEGATIVE OUTPUT LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **Ultralow Noise:** 60- μV_{RMS} Typical
- **High PSRR:** 65-dB Typical at 1 kHz
- **Low Dropout Voltage:** 280-mV Typical at 200 mA, 2.5 V
- **Available in -2.5 V, and Adjustable (-1.2 V to -10 V) Versions**
- **Stable With a 2.2- μF Ceramic Output Capacitor**
- **Less Than 2- μA Typical Quiescent Current in Shutdown Mode**
- **2% Overall Accuracy (Line, Load, Temperature)**
- **Thermal and Overcurrent Protection**
- **5-Pin SOT-23 (DBV) Package**
- **-40°C to 125°C Operating Junction Temperature Range**

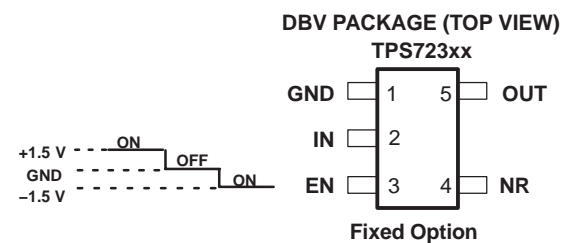
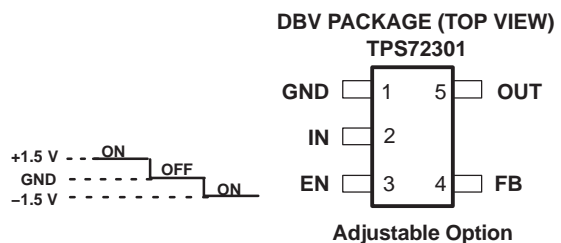
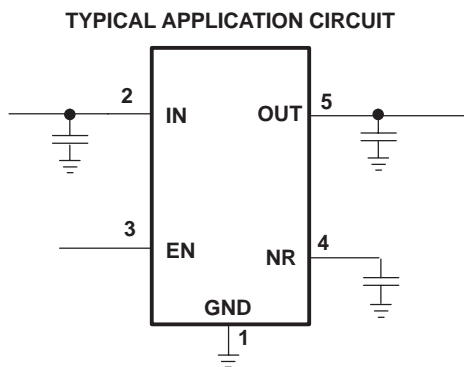
APPLICATIONS

- **Optical Drives**
- **Optical Networking**
- **Noise Sensitive Circuitry**
- **GaAs FET Gate Bias**
- **Video Amplifiers**

DESCRIPTION

The TPS723xx family of low-dropout (LDO) negative voltage regulators offers an ideal combination of features to support low noise applications. The devices are capable of operating with input voltages from -10 V to -2.7 V, and supporting outputs from -10 V to -1.2 V. These regulators are stable with small, low-cost ceramic capacitors, and include enable (EN) and noise reduction (NR) functions. Thermal short-circuit and over-current protections are provided by internal detection and shutdown logic. High PSRR (65 dB at 1 k Hz) and low noise (60 μV_{RMS}) make the TPS723xx ideal for low-noise applications.

The TPS723xx uses a precision voltage reference to achieve 2% overall accuracy over load, line, and temperature variations. Available in a small SOT23-5 package, the TPS723xx family is fully specified over a temperature range of -40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _J	VOLTAGE ⁽¹⁾	PACKAGE	PART NUMBER		SYMBOL
–40°C to 125°C	Variable –1.2 V to –10 V	SOT-23 (DBV)	TPS72301DBVT ⁽²⁾	TPS72301DBVR ⁽³⁾	TO8I
	–2.5 V		TPS72325DBVT ⁽²⁾	TPS72325DBVR ⁽³⁾	TO2I

(1) Custom output voltages from –1.2 V to –9 V in 100-mV increments are available. Minimum order quantities apply. Contact TI for details and availability.

(2) The DBVT indicates tape and reel of 250 parts.

(3) The DBVR indicates tape and reel of 3000 parts.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	UNITS
Input voltage range, V _{IN}	–11 V to 0.3 V
Enable voltage range, V _(EN)	–V _I to 5 V
Output voltage range, V _{OUT}	–11 + V _{DO}
Output current, I _{OUT}	Internally limited
Output short-circuit duration	Indefinite
Continuous total power dissipation, P _D	See Dissipation Rating Table
Junction temperature range, T _J	–55°C to 150°C
Storage temperature range, T _{stg}	–65°C to 150°C
ESD rating, HBM	2 kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage range, V _{IN}	–10		–2.7	V
Output voltage range, V _{OUT}	–10 + V _{DO}		–1.2	V
Operating junction temperature, T _J	–40		125	°C

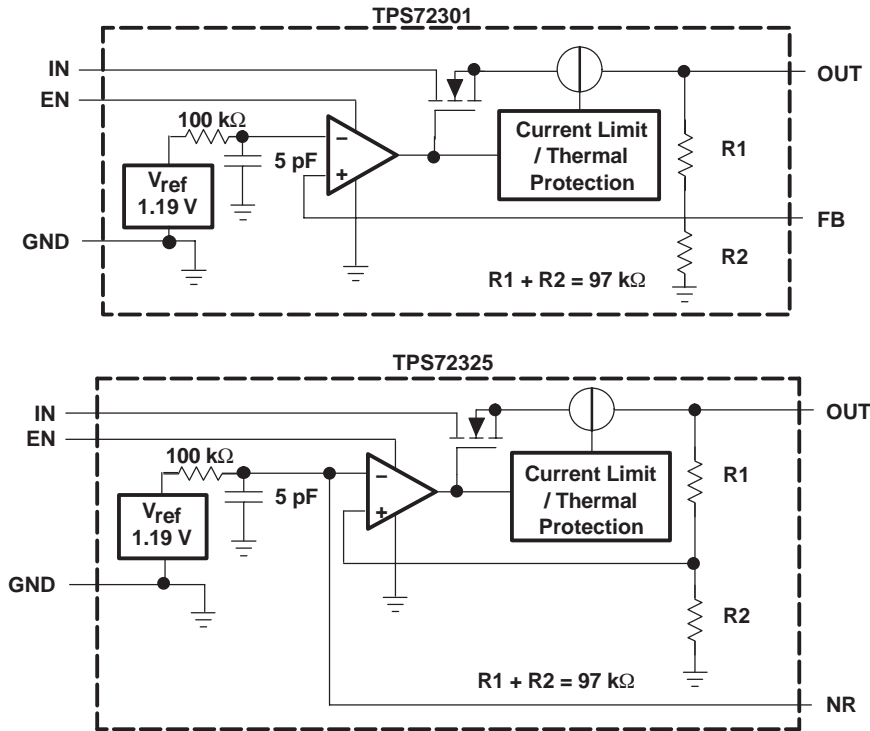
ELECTRICAL CHARACTERISTICS

 over operating junction temperature range, $V_{IN} = V_{OUT(nom)} - 0.5\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{(EN)} = 1.5\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{(NR)} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted). Typical values are at 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range ⁽¹⁾			-10		-2.7	V
$V_{(FB)}$	Feedback reference voltage	TPS72301	$T_J = 25^\circ\text{C}$	-1.210	-1.186	-1.162	V
V_{OUT}	Output voltage range	TPS72301		$-10 + V_{DO}$		$V_{(FB)}$	V
	Accuracy	Nominal	$T_J = 25^\circ\text{C}$	-1%		1%	
		TPS72325 vs $V_{IN}/I_{OUT}/T$	$-10\text{ V} < V_{IN} < V_{OUT} - 0.5\text{ V}$, $10\text{ }\mu\text{A} < I_{OUT} < 200\text{ mA}$	-2%		$\pm 1\%$	2%
		TPS72301 vs $V_{IN}/I_{OUT}/T$		-3%		$\pm 1\%$	3%
V_{OUT}/V_{IN}	Line regulation		$-10\text{ V} < V_{IN} < V_{OUT(nom)} - 0.5\text{ V}$		0.04	%/V	
V_{OUT}/I_{OUT}	Load regulation		$0\text{ mA} < I_O < 200\text{ mA}$		0.002	%/mA	
V_{DO}	Dropout voltage at $V_{OUT} = 0.96 \times V_{OUT(nom)}$	TPS72325	$I_{OUT} = 200\text{ mA}$		280	500	mV
$I_{(CL)}$	Current limit		$V_{OUT} = 0.85 \times V_{OUT(nom)}$	300	550	800	mA
$I_{(GND)}$	Ground pin current		$I_{OUT} = 0\text{ mA}$, (I_Q) $-10\text{ V} < V_{IN} < V_{OUT} - 0.5\text{ V}$		130	200	μA
			$I_{OUT} = 200\text{ mA}$, $-10\text{ V} < V_{IN} < V_{OUT} - 0.5\text{ V}$		350	500	
$I_{(SHDN)}$	Shutdown ground pin current		$-0.4\text{ V} < V_{(EN)} < 0.4\text{ V}$, $-10\text{ V} < V_{IN} < V_{OUT} - 0.5\text{ V}$		0.1	2.0	μA
$I_{(FB)}$	Feedback pin current		$-10\text{ V} < V_{IN} < V_{OUT} - 0.5\text{ V}$		0.05	1.0	μA
PSRR	Power supply rejection ratio	TPS72325	$I_{OUT} = 200\text{ mA}$, 1 kHz, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$		65		dB
			$I_{OUT} = 200\text{ mA}$, 10 kHz, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$		48		
V_n	Output noise voltage	TPS72325	$C_{OUT} = 10\text{ }\mu\text{F}$, 10 Hz = 100 kHz, $I_{OUT} = 200\text{ mA}$		60		μV_{rms}
$t_{(STR)}$	Startup time		$V_{OUT} = -2.5\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $R_L = 25\text{ }\Omega$		1		ms
$V_{EN(hi)}$	Enable threshold positive			1.5			V
$V_{EN(lo)}$	Enable threshold negative					-1.5	V
$V_{DIS(hi)}$	Disable threshold positive					0.4	V
$V_{DIS(lo)}$	Disable threshold negative			-0.4			V
$I_{(EN)}$	Enable pin current		$-10\text{ V} \leq V_{IN} \leq V - 0.5\text{ V}$, $-10\text{ V} \leq V_{(EN)} \leq \pm 3.5\text{ V}$		0.1	2.0	μA
	Thermal shutdown temperature		Shutdown, temperature increasing		165		$^\circ\text{C}$
			Reset, temperature decreasing		145		
T_J	Operating junction temperature			-40		125	$^\circ\text{C}$

⁽¹⁾ Maximum $V_{IN} = V_{OUT} + V_{DO}$ or -2.7 V , whichever is more negative.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	NO.	DESCRIPTION
GND	1	Ground
VIN	2	Unregulated input supply
EN	3	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode.
NR	4	Fixed voltage versions only. Connecting an external capacitor between this pin and ground, bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	4	Adjustable voltage version only. This is the input to the control loop error amplifier. It is used to set the output voltage of the device
VOUT	5	Regulated output voltage. A small 2.2 μF ceramic capacitor is needed from this pin to GND to ensure stability.

TYPICAL CHARACTERISTICS

(TPS72325 $V_{IN} = V_{OUT(nom)} - 0.5\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{(EN)} = 1.5\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{(NR)} = 0.01\text{ }\mu\text{F}$ unless otherwise noted)

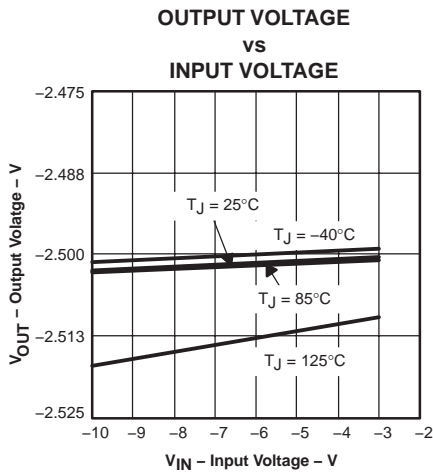


Figure 1

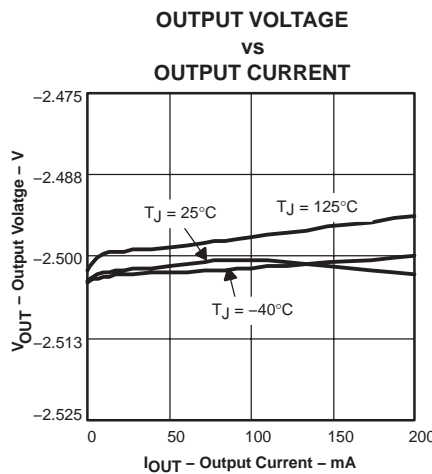


Figure 2

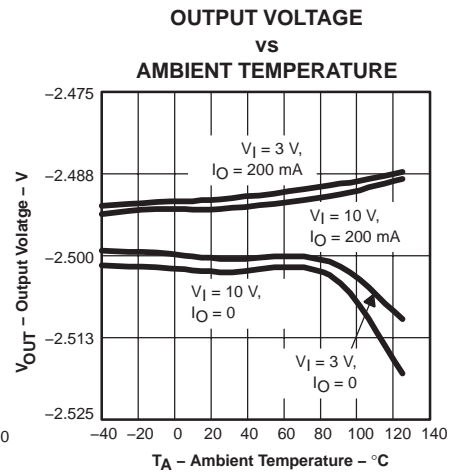


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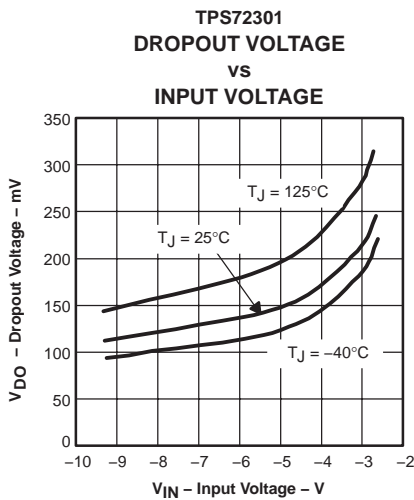


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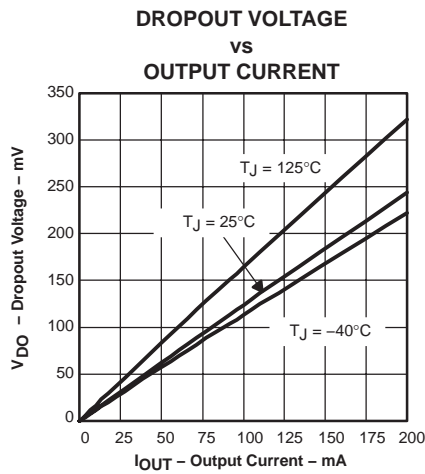


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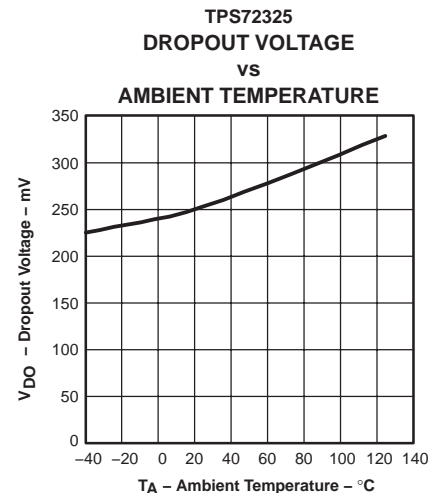


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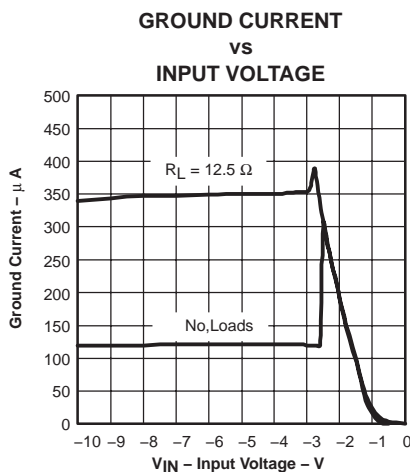


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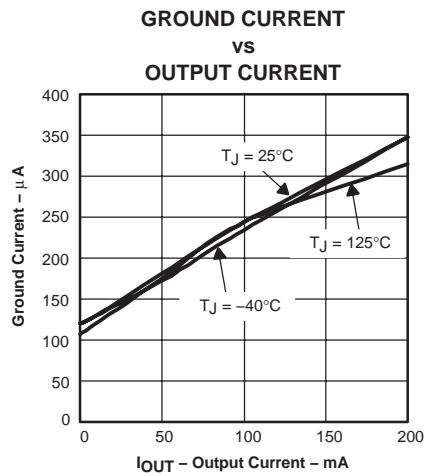


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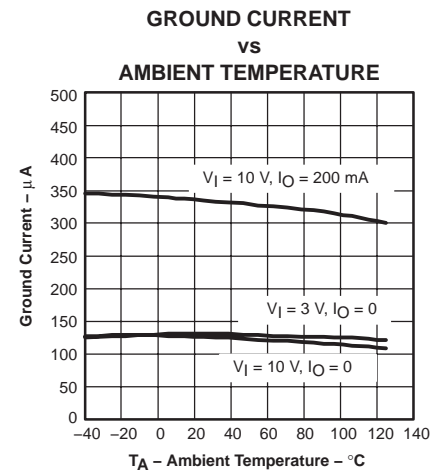


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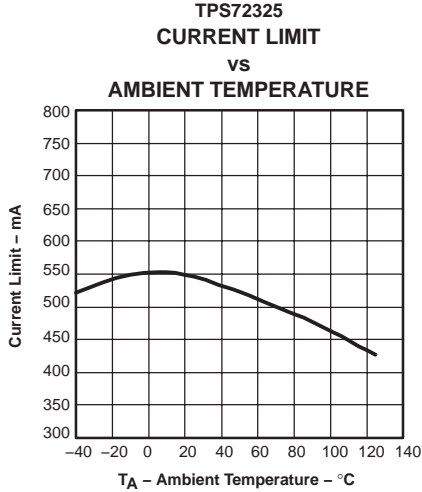


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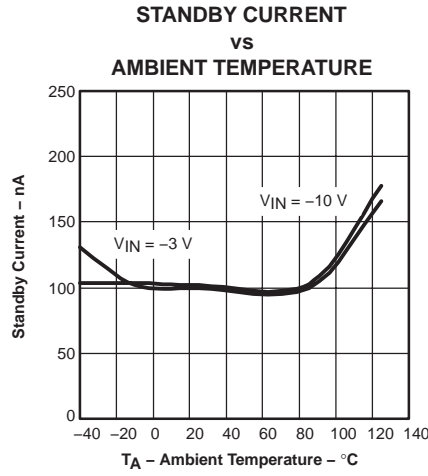


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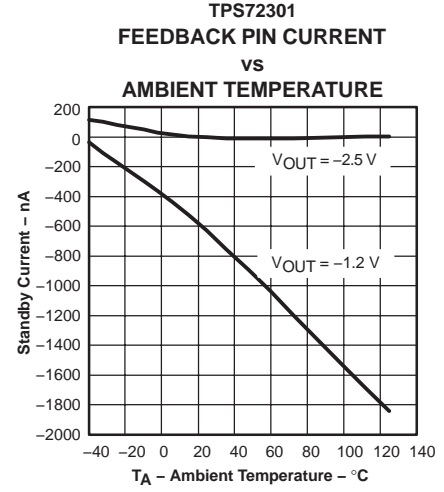


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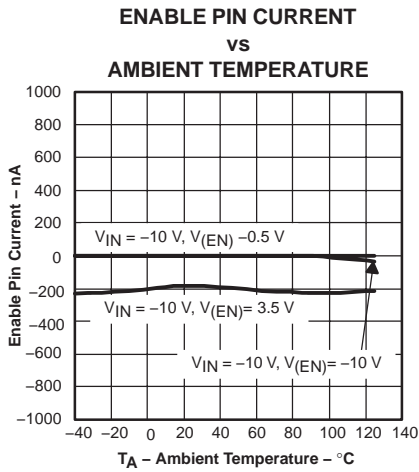


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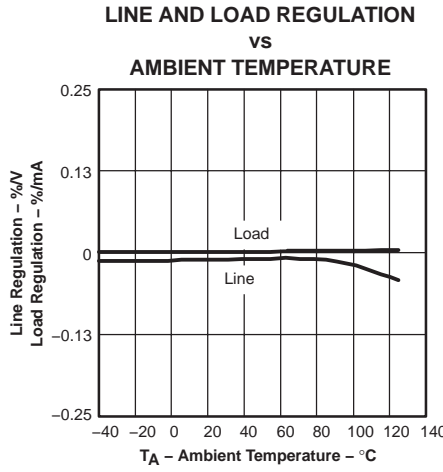


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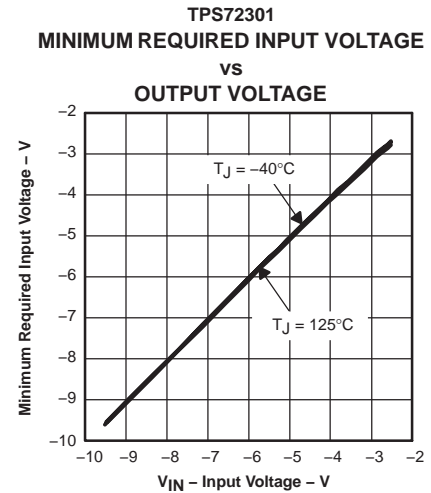


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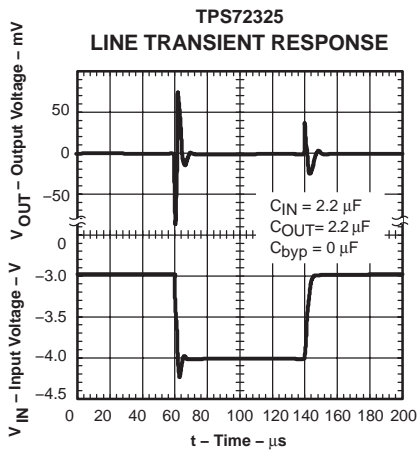


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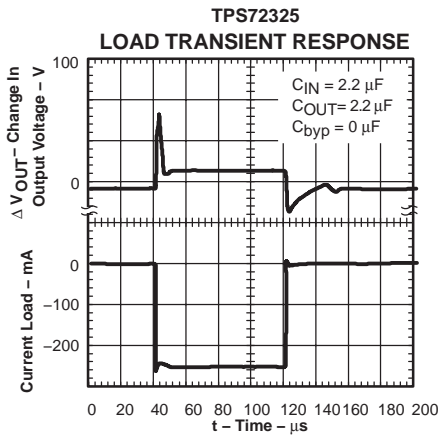


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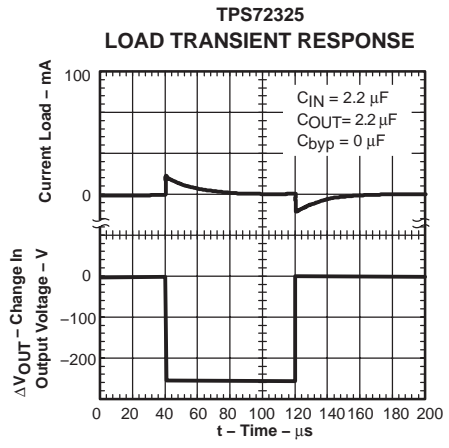


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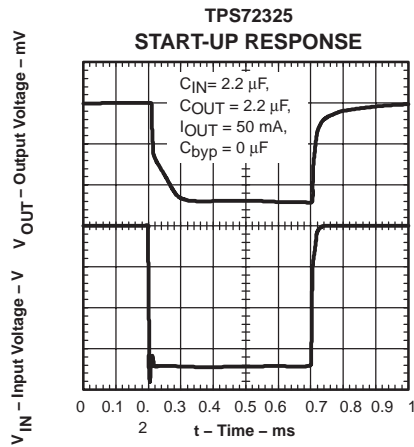


Figure 19

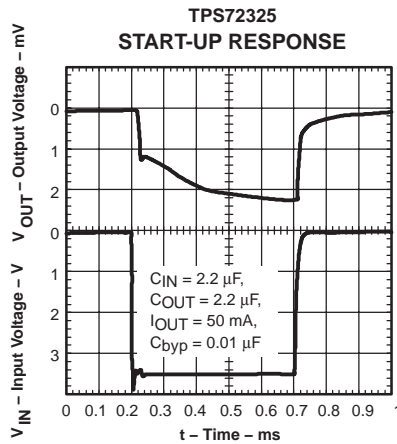


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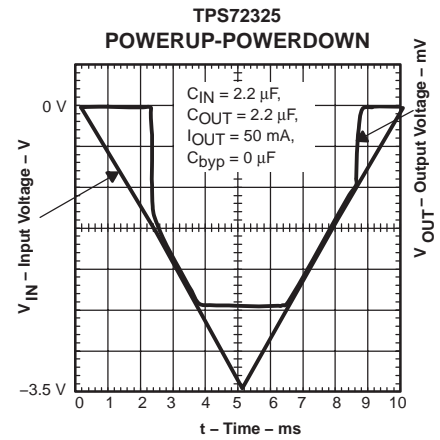


Figure 21

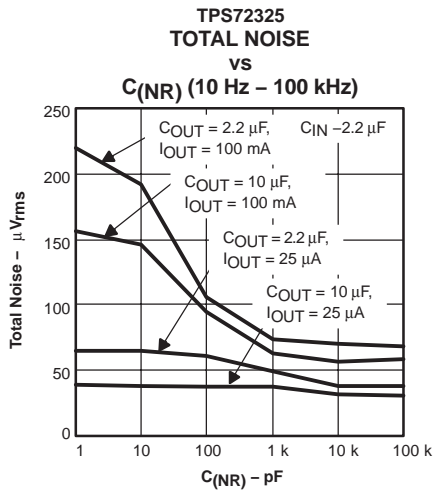


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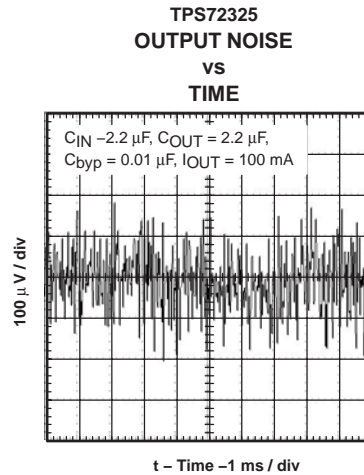


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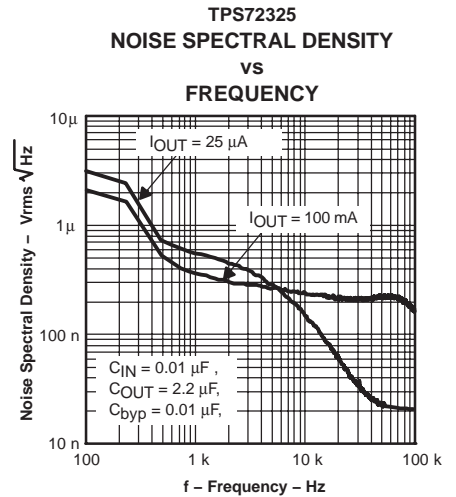


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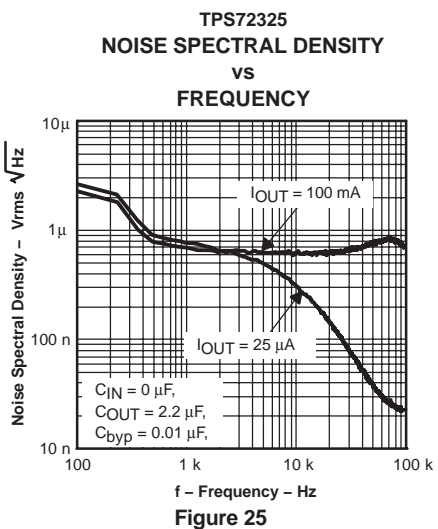


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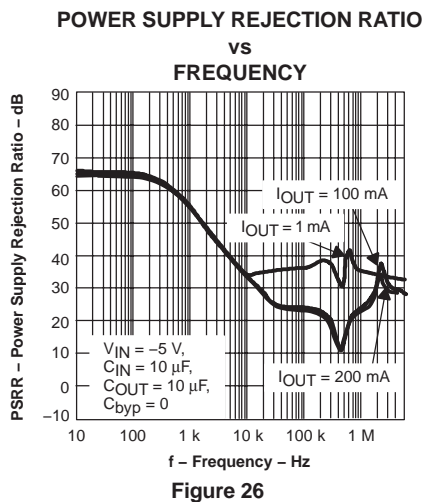


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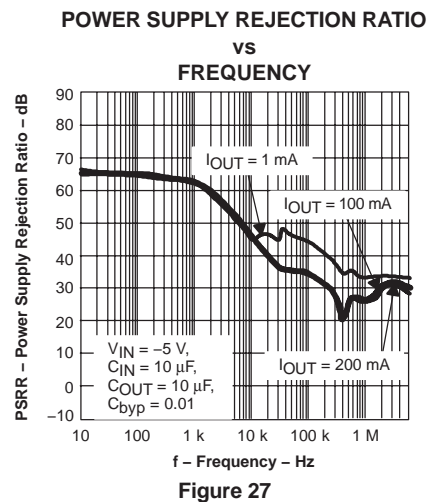


Figure 27

APPLICATION INFORMATION

DEVICE OPERATION

The TPS723xx is a low-dropout negative linear voltage regulator with a rated current of 200 mA. It is offered in trimmed output voltages between -1.5 V and -5.2 V and as an adjustable regulator from -1.2 V to -10 V. It features very low noise and high PSRR making it ideal for high sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to 2 μ A maximum over temperature and process. The TPS723xx is offered in a small SOT23 package and is specified over a -40°C to 125°C temperature range.

ENABLE

The enable pin is active above 1.5 V and below -1.5 V, allowing it to be controlled by a standard TTL signal or by connection to V_I if not used. When driven to GND most internal circuitry is turned off, putting the TPS723xx into shutdown mode, drawing 2 μ A maximum ground current.

ADJUSTABLE VOLTAGE APPLICATIONS

The TPS72301 allows designers to specify any output voltage from -10 V to -1.2 V. As shown in the application circuit in Figure 28, an external resistor divider is used to scale the output voltage V_O to the reference voltage 1.186 V. For best accuracy, use precision resistors for R_1 and R_2 .

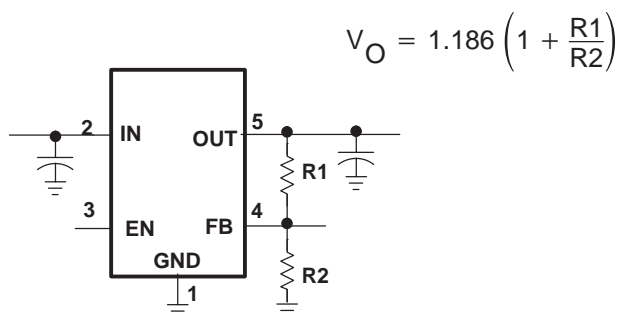


Figure 28. TPS72301 Adjustable LDO Regulator Programming

CAPACITOR SELECTION FOR STABILITY

Appropriate input and output capacitors should be used for the intended application. The TPS723xx only requires a 2.2 - μF ceramic output capacitor to be used for stable operation. Both the capacitor value and ESR affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2 - μF ceramic output capacitor located close to the regulator is sufficient.

OUTPUT NOISE

Without external bypassing, output noise of the TPS723xx from 10 Hz to 100 kHz is 200 μV_{RMS} typical. The dominant contributor to output noise is the internal bandgap reference. Adding an external 0.01 - μF capacitor to ground reduces noise to 60 μV_{RMS} . Best noise performance is achieved using appropriate low ESR capacitors for bypassing noise at the NR and VOUT pins. See the Noise vs C_{OUT} plot in the Typical Characteristics section.

POWER SUPPLY REJECTION

The TPS723xx offers a very high power supply rejection ratio (PSRR) for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high quality input and output capacitors.

CURRENT LIMIT

The TPS723xx has internal circuitry that monitors and limits output current to protect the regulator from damage under all load conditions. When output current reaches the output current limit (550 mA typical), protection circuitry turns on, reducing output voltage to ensure current does not increase. See Current Limit in the Typical Characteristics section.

THERMAL PROTECTION

As protection from damage due to excessive junction temperatures, the TPS723xx has internal protection circuitry. When junction temperature reaches approximately 165°C , the output device is turned off. After the device has cooled by about 20°C , the output device is enabled, allowing normal operation. For reliable operation, design is for worst case junction temperature of $\leq 125^{\circ}\text{C}$ taking into account worst case ambient temperature and load conditions.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS72301DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72301DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72301DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72301DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS72325DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

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