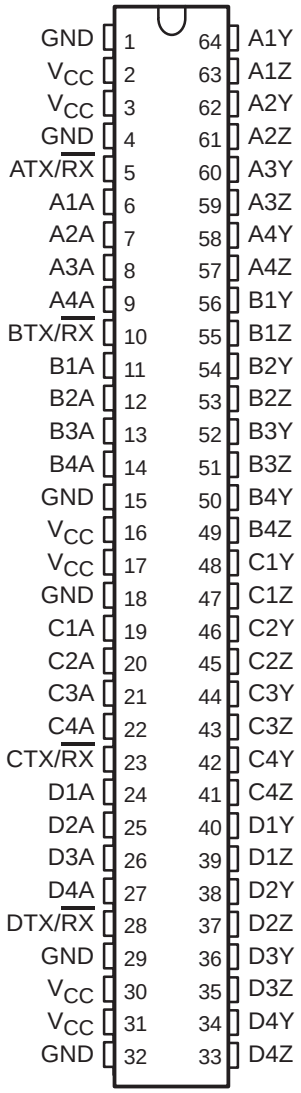
- **Sixteen Low-Voltage Differential Transceivers Designed for Signaling Rates† Up to 630 Mbps**
- **Simplex (Point-to-Point) and Half-Duplex (Multipoint) Interface**
- **Typical Differential Output Voltage of 340 mV Into a 50-Ω Load**
- **Integrated 110-Ω Line Termination on ‘LVDM1677 Product**
- **Propagation Delay Time:**
  - **Driver: 2.5 ns Typ**
  - **Receiver: 3 ns Typ**
- **Recommended Maximum Transfer Rate:**
  - **Driver: 650 M-Transfers/s**
  - **Receiver: 350 M-Transfers/s**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V for Power Up/Down Glitch-Free Performance and Hot-Plugging Events**
- **Bus-Terminal ESD Protection Exceeds 12 kV**
- **Low-Voltage TTL (LVTTL) Logic Input Levels Are 5-V Tolerant**
- **Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch**

SN65LVDM1676DGG (Marked as LVDM1676)
SN65LVDM1677DGG (Marked as LVDM1677)
(TOP VIEW)



description

The SN65LVDM1676 and SN65LVDM1677 (integrated termination) are sixteen differential line drivers and receivers configured as transceivers that use low-voltage differential signaling (LVDS) to achieve signaling rates in excess of 600 Mbps. These products are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers are doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of 100 mV with up to 1 V of ground potential difference between a transmitter and receiver.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of transceivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

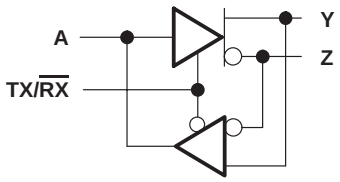
The SN65LVDM1676 and SN65LVDM1677 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

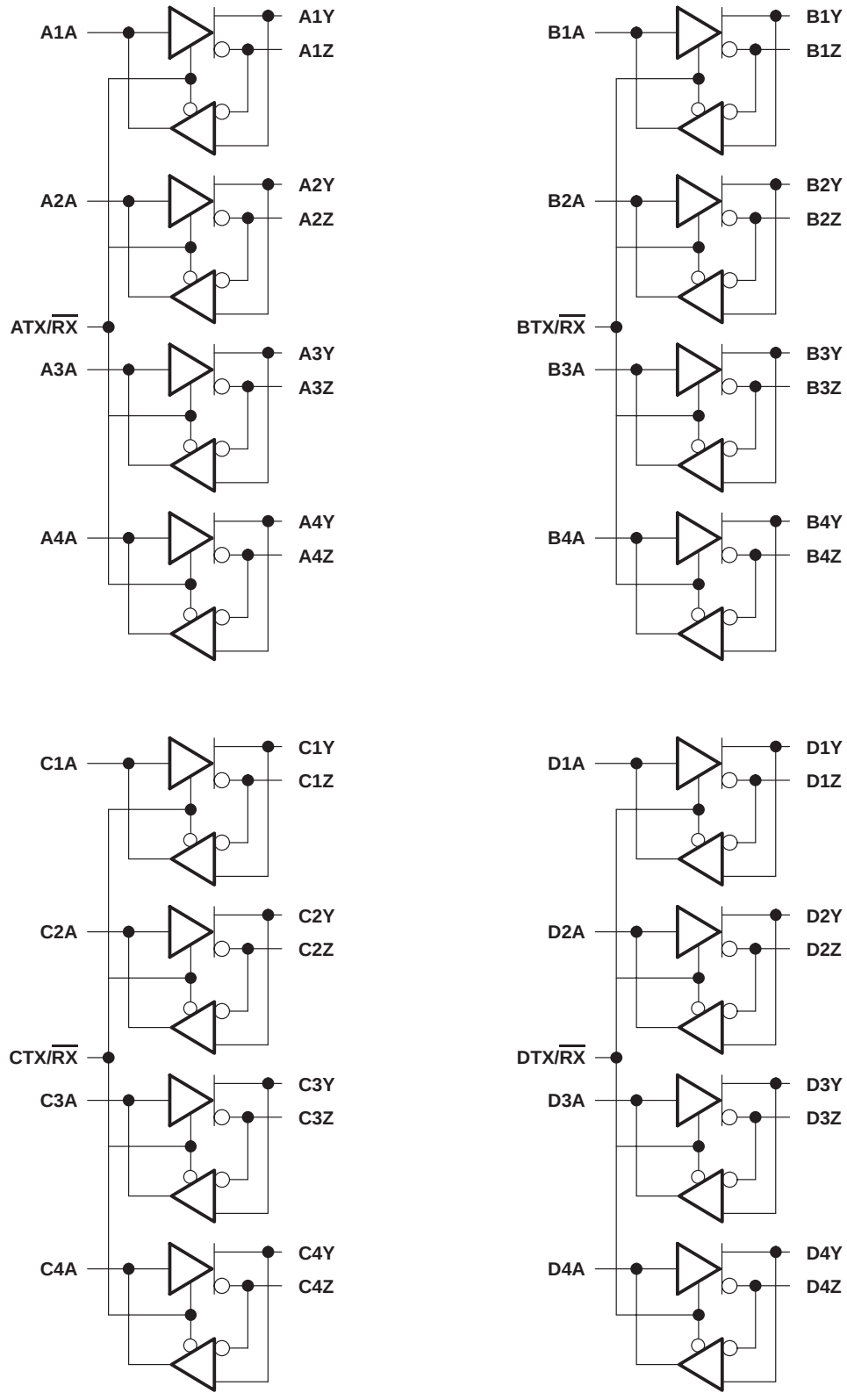
INPUTS			OUTPUTS		
(Y − Z)	TX/$\overline{RX}$	A	Y	Z	A
$V_{ID} \geq 100$ mV	L	NA	Z	Z	H
−100 mV < V_{ID} < 100 mV	L	NA	Z	Z	?
$V_{ID} \leq 100$ mV	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	H
NA	H	L	L	H	Z
NA	H	H	H	L	Z

H = high level, L= low level, Z= high impedance, ? = indeterminate

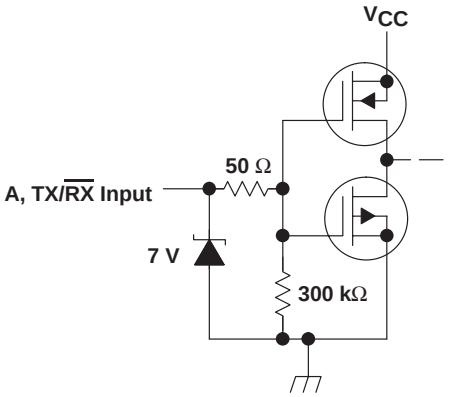
LVD Transceiver

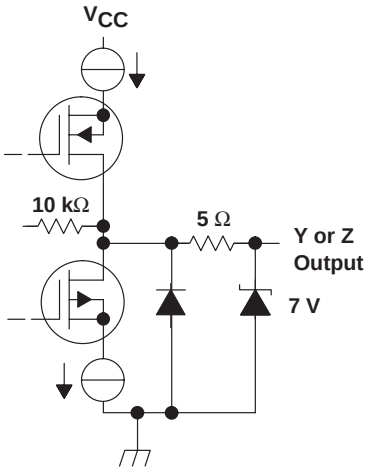


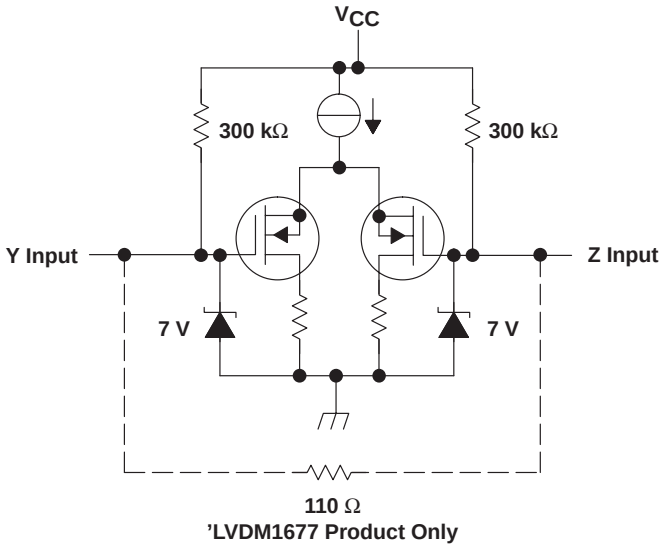
logic diagram (positive logic)



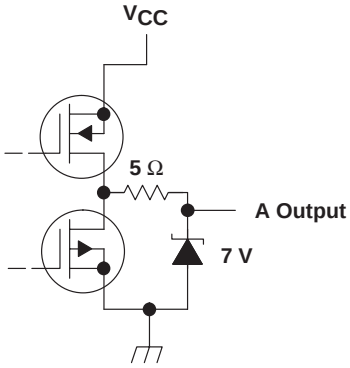
equivalent input and output schematic diagrams







'LVDM1677 Product Only



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 4 V
Input voltage range: A, TX/$\overline{RX}$ . . . . . −0.5 V to 6 V
Y or Z . . . . . −0.5 V to 4 V
Differential input voltage magnitude, V_{ID}, (SN65LVDM1677 only) . . . . . 1 V
Receiver output current, I_O . . . . . ±20 mA
Electrostatic discharge: Y, Z, and GND (see Note 2) . . . . . Class 3, A:8 kV, B:600 V
Continuous power dissipation . . . . . Class 3, A:7 kV, B:500 V
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.
3. This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no airflow.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DGG	2094 mW	16.7 mW/°C	1089 mW

‡ All typical values are at 25°C and with a 3.3-V supply.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		0.6	V
Common-mode input voltage, V_{IC}	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			$V_{CC}-0.8$	V
Receiver low-level output current, I_{OL}			8	mA
Receiver high-level output current, I_{OH}	−8			mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

device

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	Driver enabled, receiver disabled, R_L 50 Ω		140	175	mA
		Driver disabled, receiver enabled, no load		45	60	

‡ All typical values are at 25°C and with a 3.3-V supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 50 Ω, See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		−50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		−50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{IH}	High-level input current	V_{IH} = 2 V		3	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		2	10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			10	mA
		V_{OD} = 0 V			10	mA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±10	µA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6pt) + 0.5 V		5		pF

receiver

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 6 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold			−100			
V_{OH}	High-level output voltage		I_{OH} = −8 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.4	V
I_I	Input current (Y or Z inputs)		V_I = 0 V		−24	−40	µA
			V_I = 2.4 V	−1.2	−8		
I_{ID}	Differential input current $\|I_{IY} - I_{IZ}\|$ (inputs)	'LVDM1676	V_{IY} = 0 V and V_{IZ} = 100 mV, V_{IY} = 2.4 V and V_{IZ} = 2.3 V		5	10	µA
		'LVDM1677	V_{IY} = 0.2 V and V_{IZ} = 0 V, V_{IY} = 2.4 V and V_{IZ} = 2.2 V	1.5		2.2	mA
$I_{I(OFF)}$	Power-off input current (Y or Z inputs)		V_{CC} = 0 V, V_I = 2.4 V			±25	µA

† All typical values are at 25°C and with a 3.3-V supply.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 10 pF, See Figure 4	1.3	2.5	3.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.3	2.5	3.6	ns
t_r	Differential output signal rise time			0.5	1.2	ns
t_f	Differential output signal fall time			0.5	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			0.1	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew†			0.1	0.4	ns
$t_{sk(pp)}$	Part-to-part skew‡				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		11	20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			10	20	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3	10	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			3	10	ns

† $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

‡ $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

receiver

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 7	1.5	3	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.5	3	4.5	ns
t_r	Output signal rise time			0.6	1.6	ns
t_f	Output signal fall time			0.6	1.6	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			0.2	0.8	ns
$t_{sk(o)}$	Channel-to-channel output skew†			0.7	1.2	ns
$t_{sk(pp)}$	Part-to-part skew‡				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 8		9	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 8		8	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 8		12	20	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			11	20	ns

† $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

‡ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

§ All typical values are at 25°C and with a 3.3-V supply.

PARAMETER MEASUREMENT INFORMATION

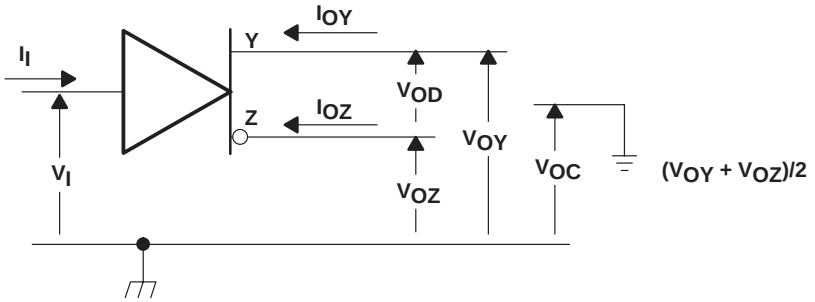


Figure 1. Driver Voltage and Current Definitions

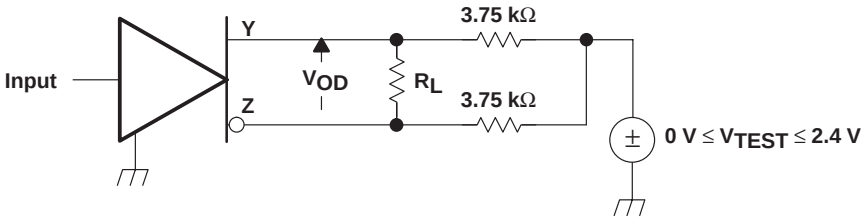
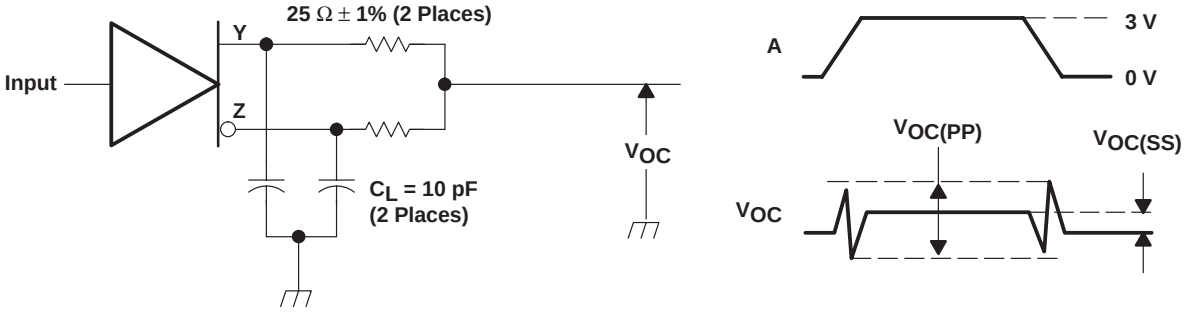


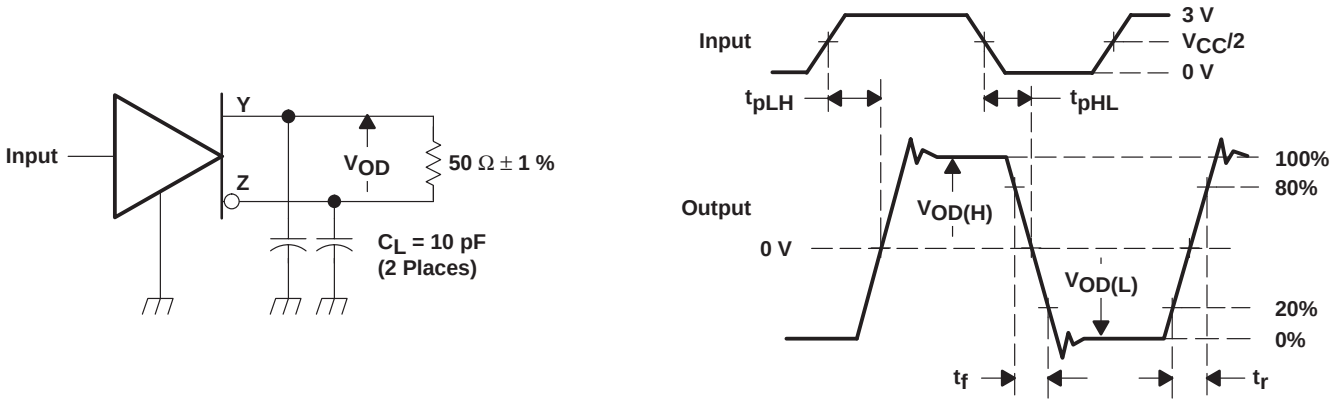
Figure 2. Driver V_{OD} Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a −3 dB bandwidth of at least 300 MHz.

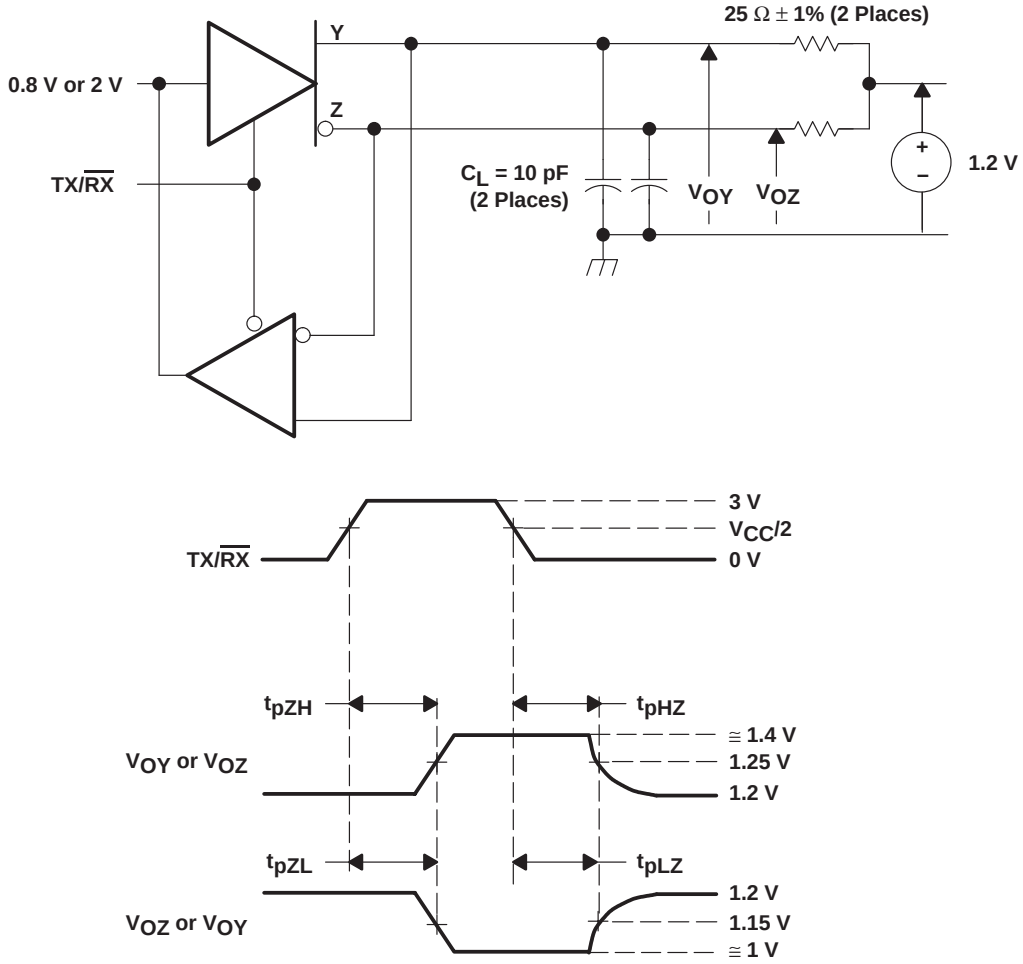
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION

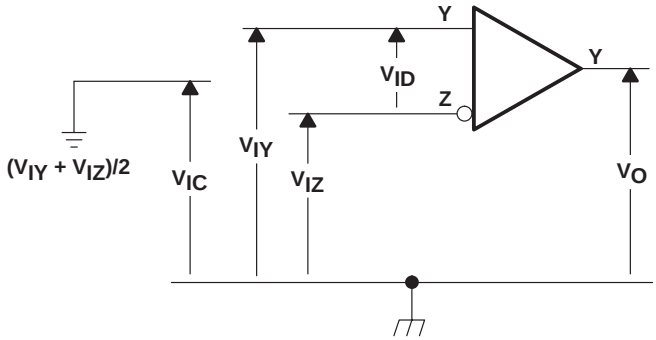
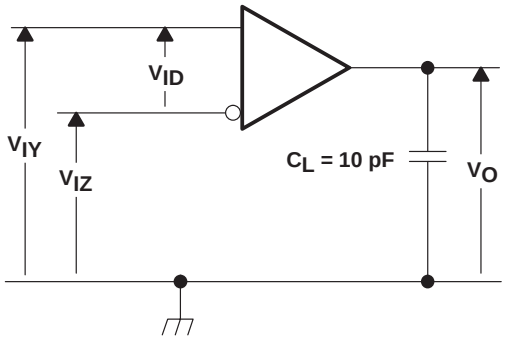
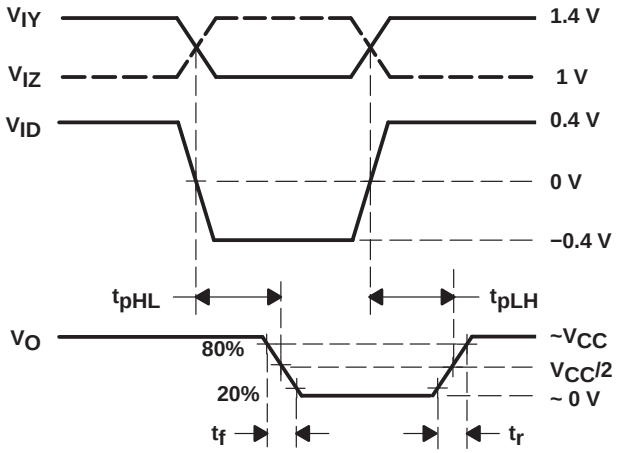


Figure 6. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IY}	V_{IZ}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	−100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	−100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	−100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	−600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	−600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	−600 mV	0.3 V

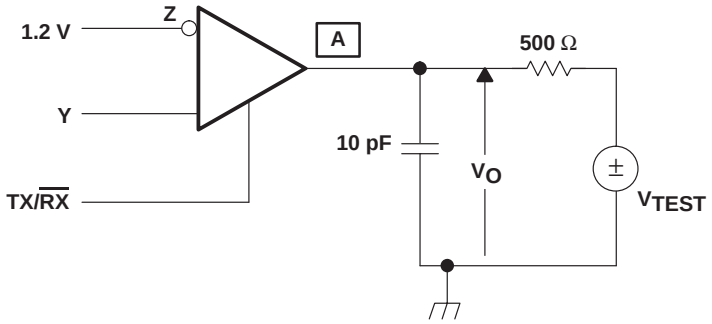




NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 7. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

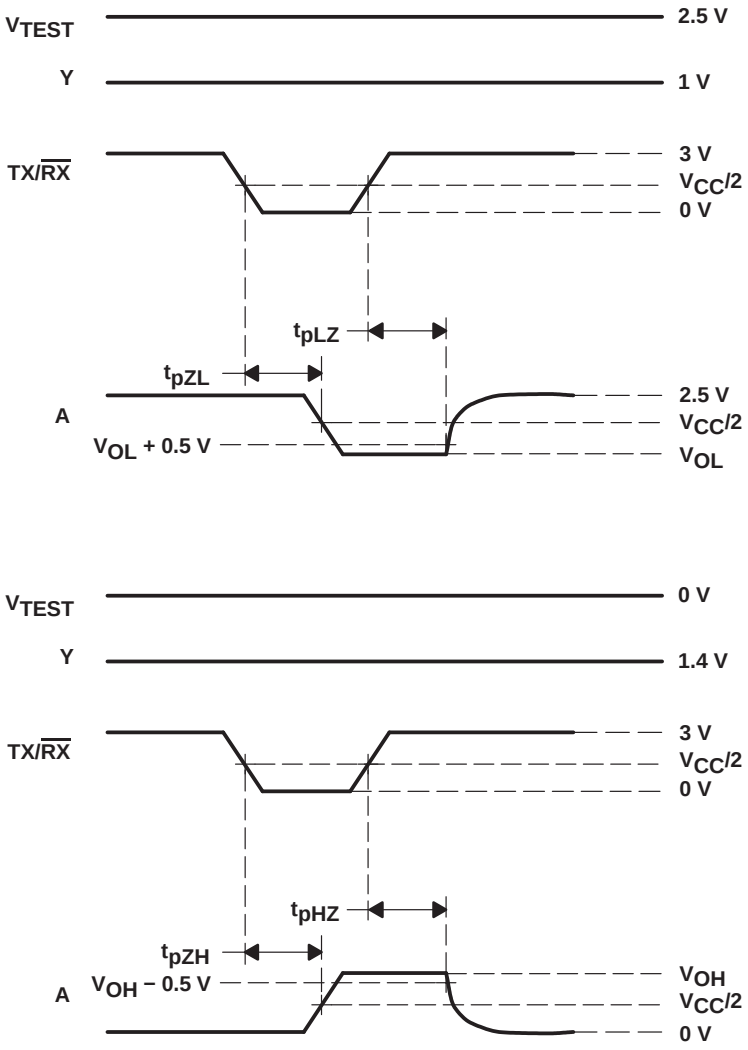


Figure 8. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

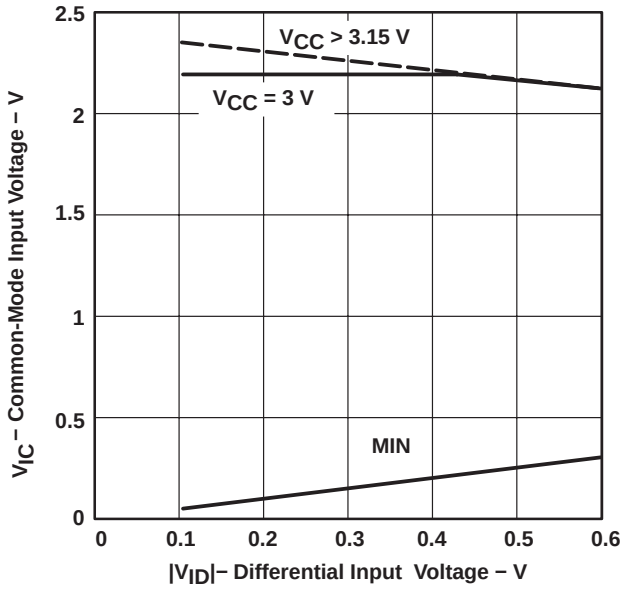


Figure 9

DRIVER
LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

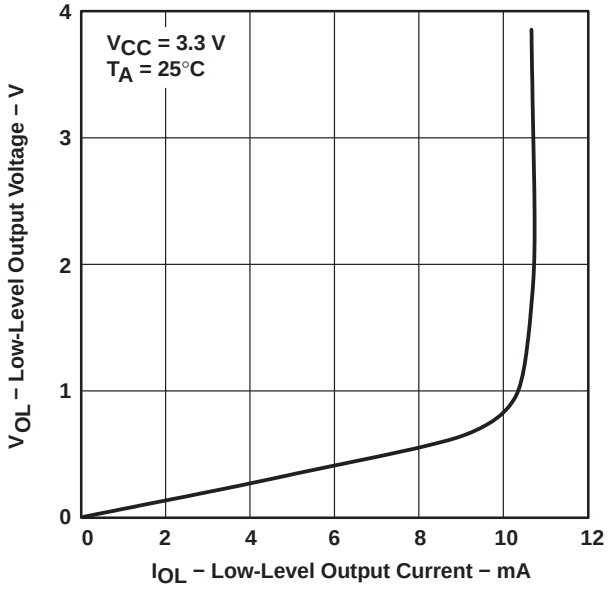


Figure 10

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

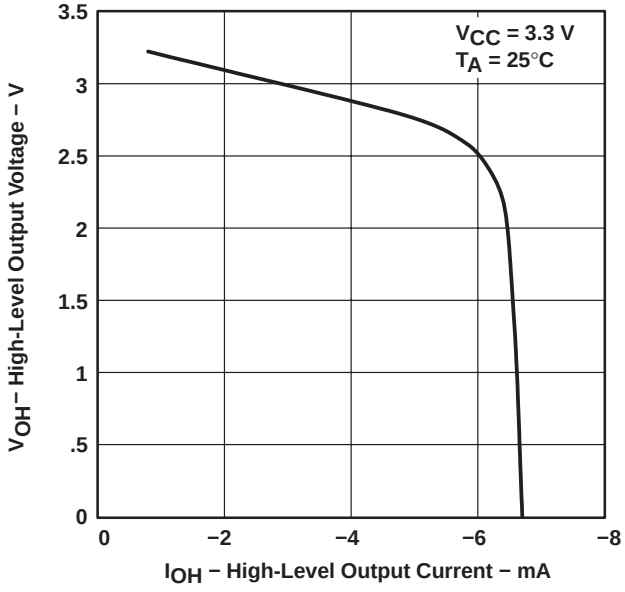


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

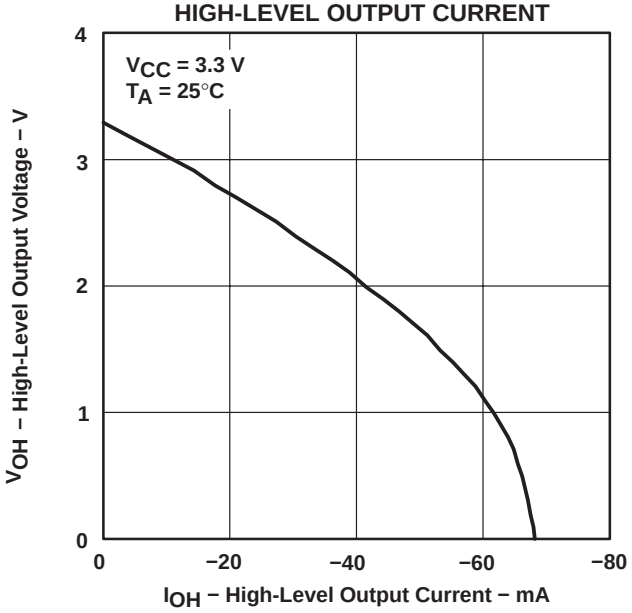


Figure 12

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

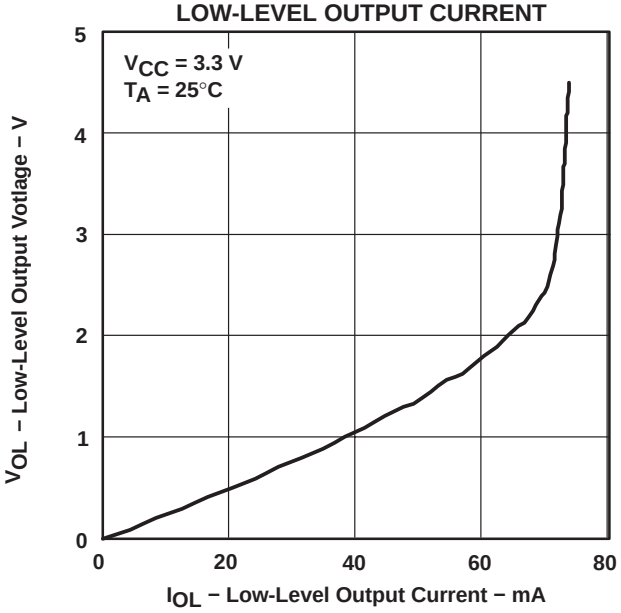


Figure 13

TYPICAL CHARACTERISTICS

driver eye pattern

test conditions

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All 16 channels switching simultaneously with NRZ data. Scope is triggered at the same frequency with pulse. Input signal level = 0 to 3 V single ended.
- Resistive loading with no added capacitance

equipment

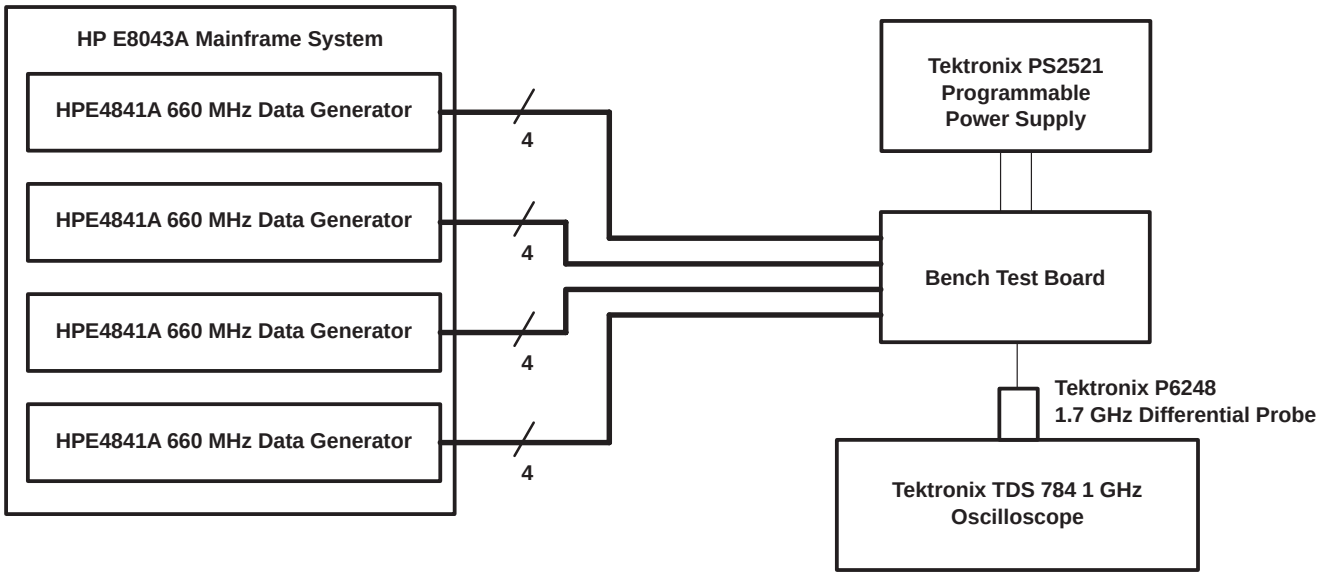
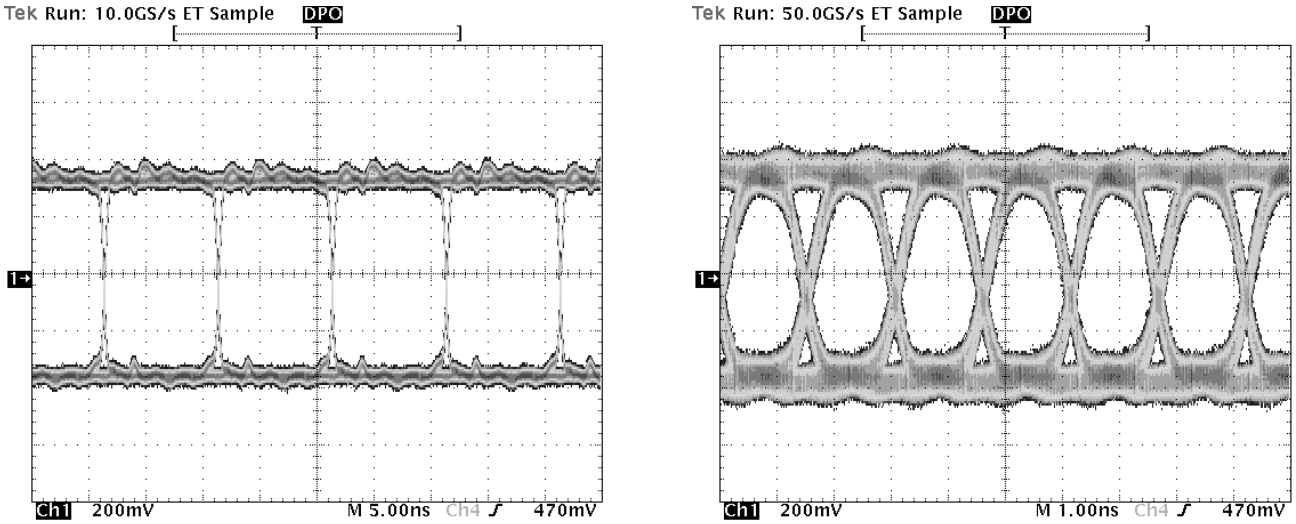


Figure 14. Driver Test Equipment Setup



100 Mbps **650 Mbps**

Figure 15. Typical Driver Eye Pattern for the SN65LVDM1676

TYPICAL CHARACTERISTICS

receiver eye pattern

test conditions

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All 16 channels switching simultaneously with NRZ data. Scope is pulse-triggered simultaneously with NRZ data. Input signal level is 1 V to 1.4 V differential.
- 50-Ω resistive loading with no added capacitance

equipment

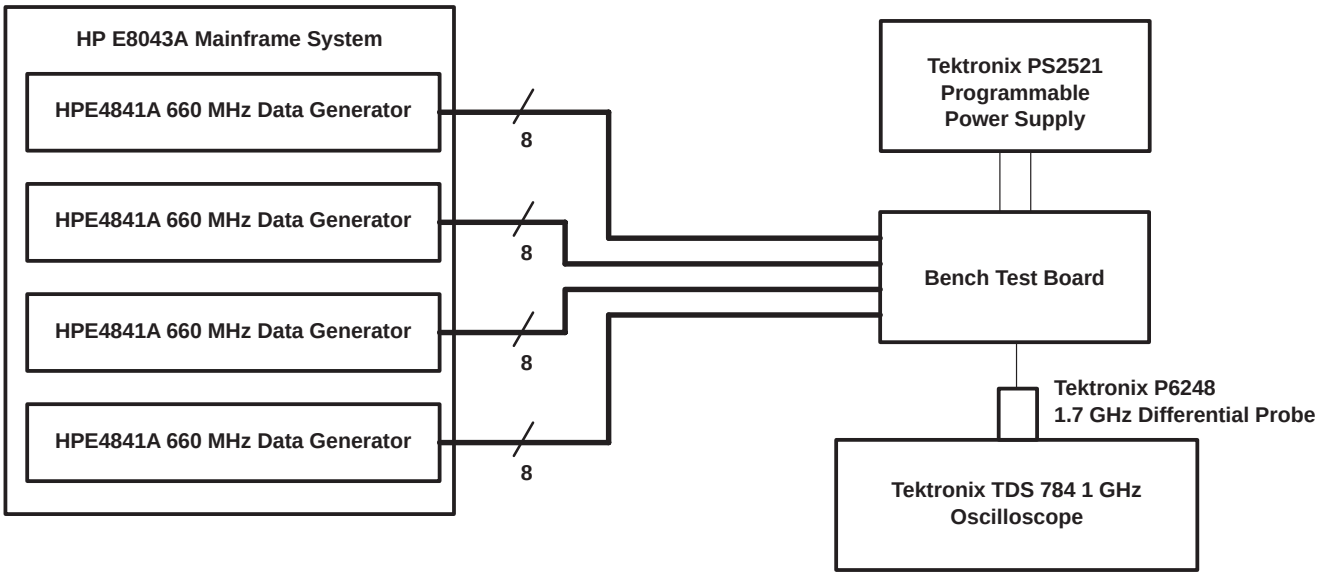
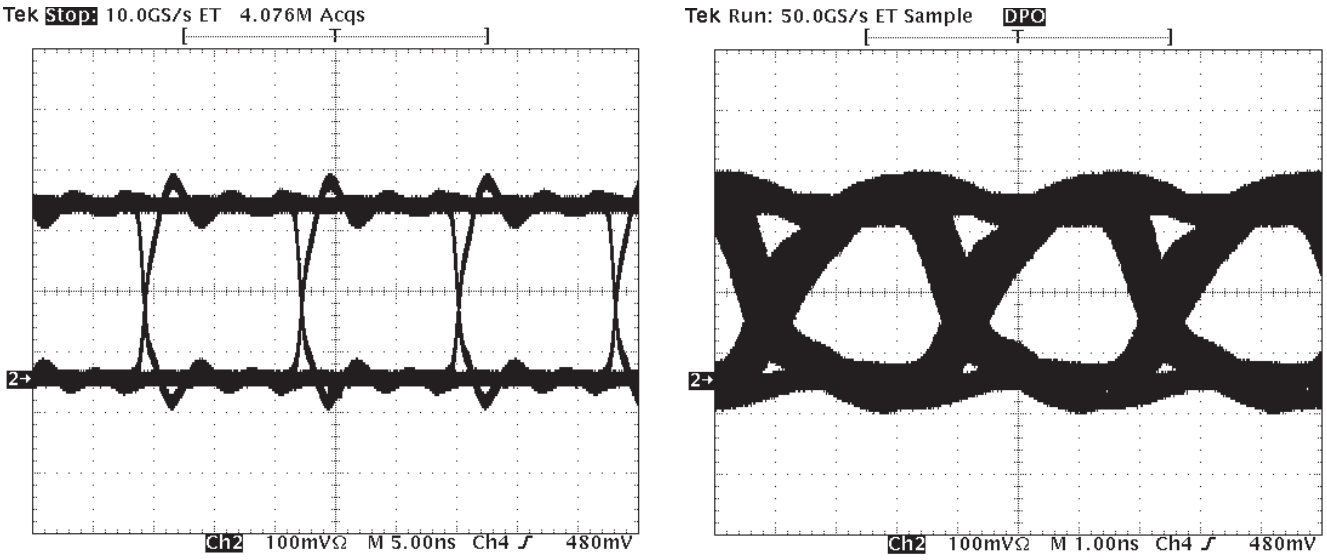


Figure 16. Receiver Test Equipment Setup



100 Mbps **350 Mbps**

Figure 17. Typical Receiver Eye Pattern for the SN65LVDM1677

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between −50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different, however, in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 18. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

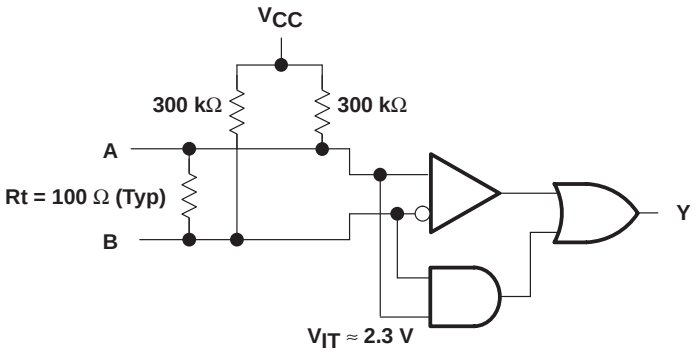


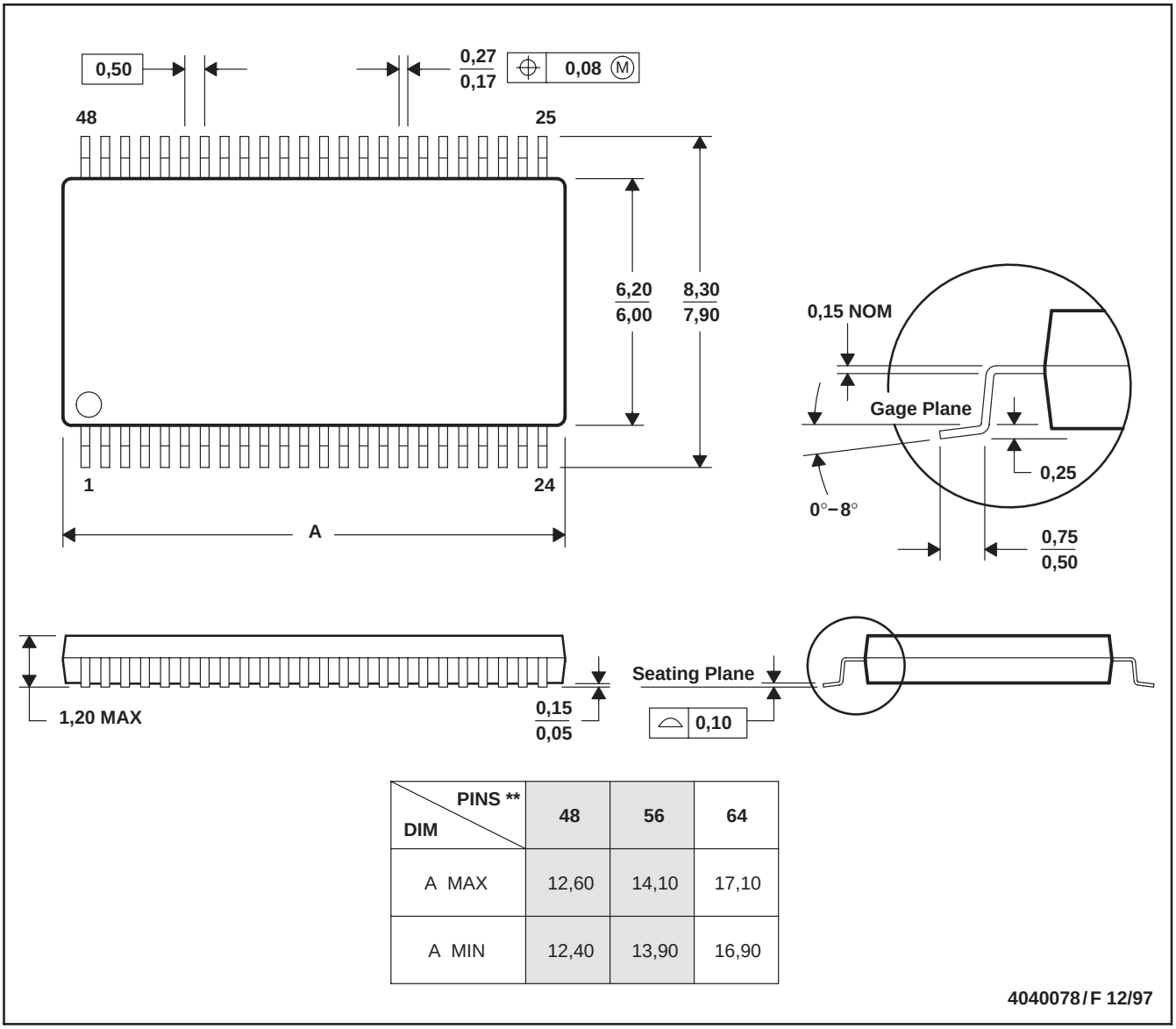
Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDM1676DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1676DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1676DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1676DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM1677DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

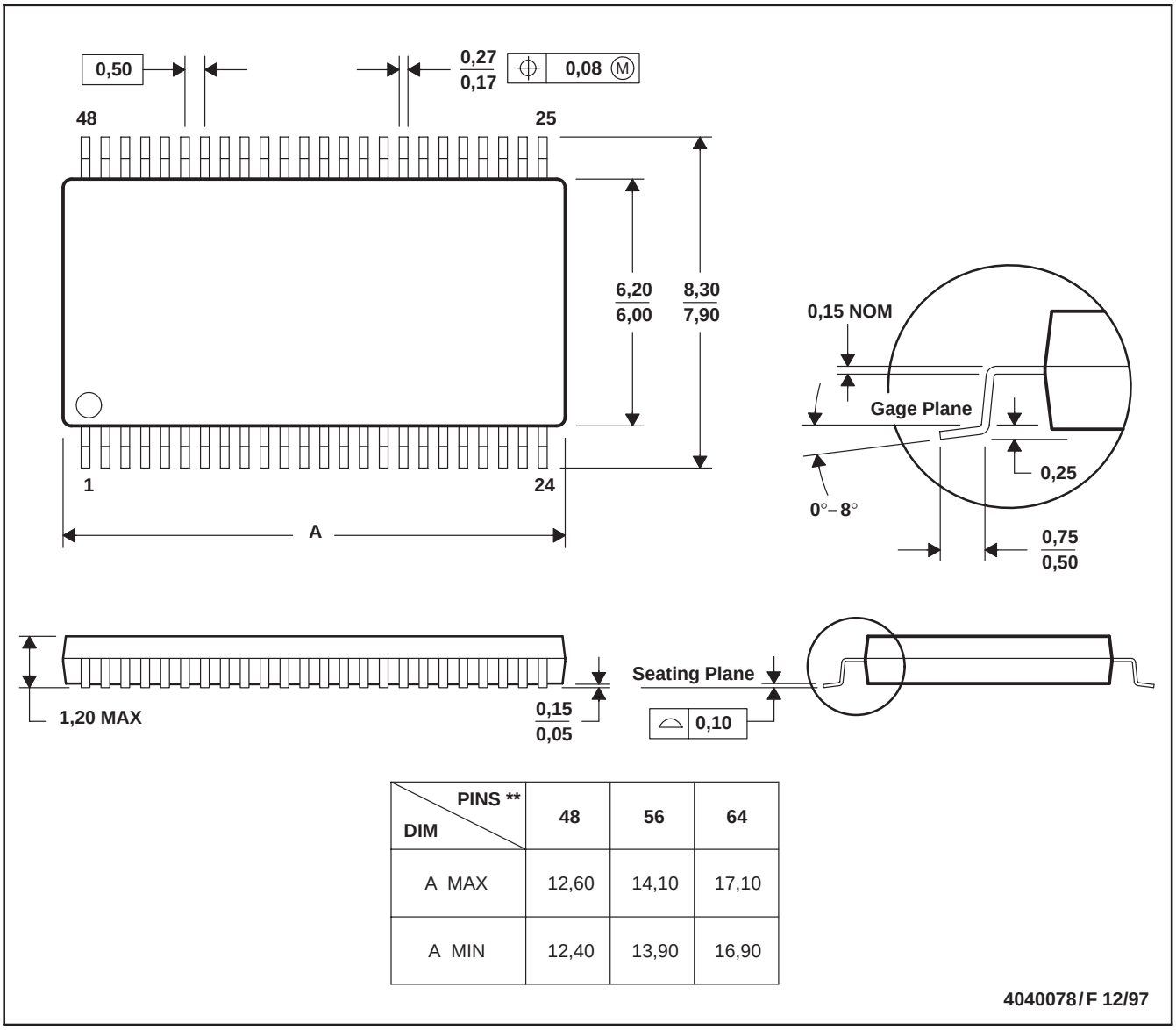
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



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