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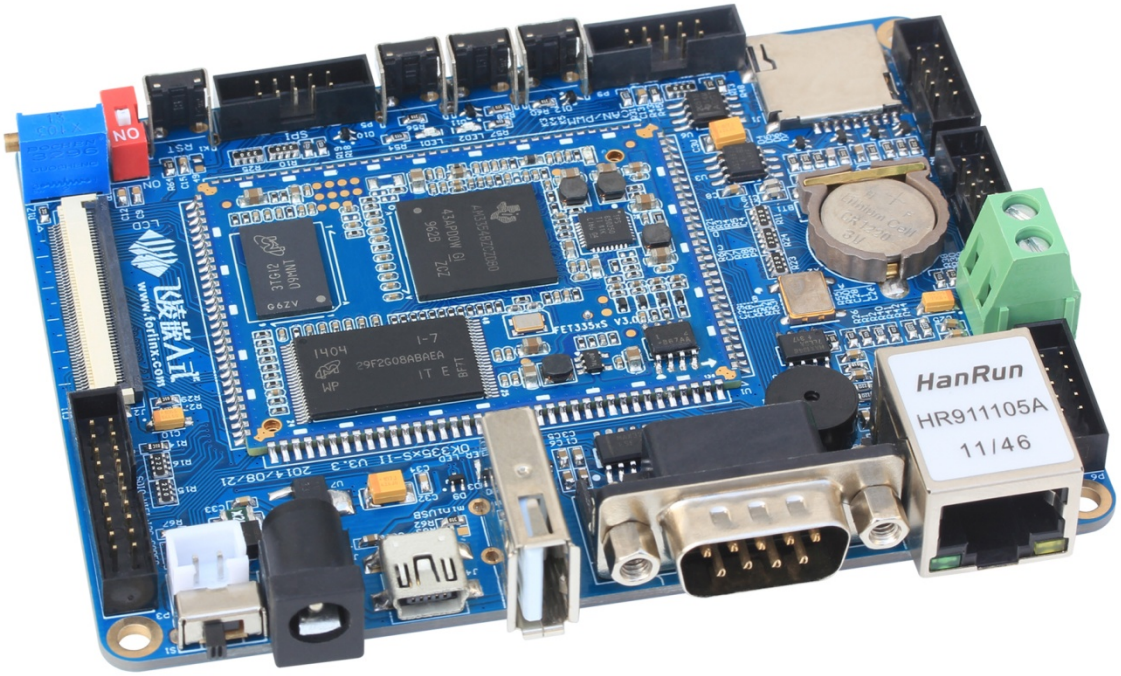
FORLINX EMBEDDED

OK335xS-Ⅱ

Hardware Manual



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Precaution and Maintenance

Working Environment

Working Temperature: -40 – 85 ℃
Working Humidity: 10 – 90%

Precautions:

- Don’t touch the connecting part of the CPU board, it may cause poor contact between CPU module and base board.
- Don’t hot-plug the CPU module when power is on.
- Please keep the board dryness. If you spill or infiltrate any liquid accidentally, please power it off immediately and fully dry it off.
- Please avoid using or storing the board under dusty and dirty environment.
- Please pay attention to the ventilation and radiation to avoid elements damage due to high temperature.
- Please don’t use the board under hot and cold alternating environment to avoid elements damage due to condensation.
- Please don’t try to disassembly the board.
- Please don’t drop, knock or violent shake the boards and maybe the circuit or elements damage.
- Please don’t use organic solvents or corrosive liquids to wash the product.
- Please don’t paint the product.
- Unauthorized modification or accessories may damage the product. Forlinx is not responsible for warranty for any damages due to these reasons.

If the product has some faults, please contact Forlinx Technology Service Department.

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Version history

Time	Version	Contents	Remark
2014.9.15	v1.0	1.Adding CPU JTAG layout. 2.Adding schematics and instruction of Ethernet Chip(LAN8720).	Compiled by: R&D engineers, customer service engineers. Translated by： Linda Lin
2014.7.14	v1.0	Newly compiled files	Compiled by: R&D engineers, customer service engineers. Translated by： Linda Lin
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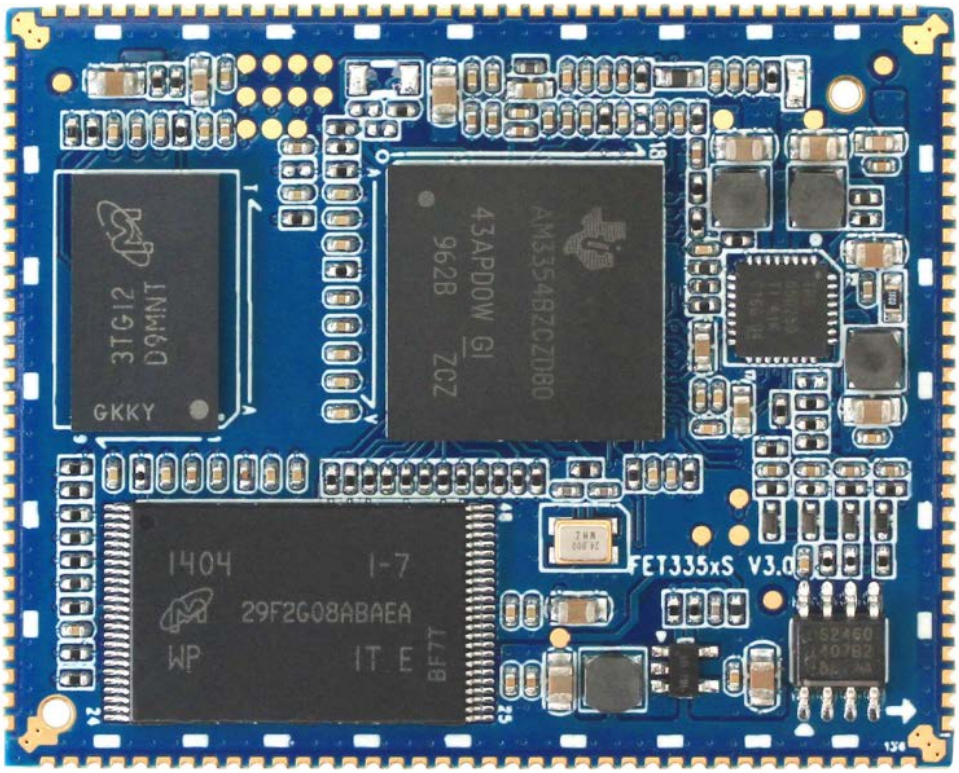
Chapter 1 FET335xS-II CPU Module Overview

1.1 FET335xS-II Processor Features

FET335xS-II CPU module is designed on the basis of Sitara Cortex-A8,AM3354,with main frequency reach up to 800MHz(1GHz maximum).Its maximum ARM MIPS reaches 1600MIPS(Even 2000MIPS when CPU is running at 1GHz).Flexible power management options to minimize active power while enabling standby power as low as 7mW.Furthermore,FET335xS-II CPU module integrates with industrial 128MB,400Mhz DDR3,256MB SLC Nandflash and highly integrated PMU.

FET335xS-II CPU module is designed as 8-layer PCB board,with ENIG technology to ensure reliable electrical and electromagnetic features.CPU module and base board is connected via stamp holes which help to lower cost and enhance reliability of OK335xS-II single board computer.



FET335xS-II CPU Module (Top View)

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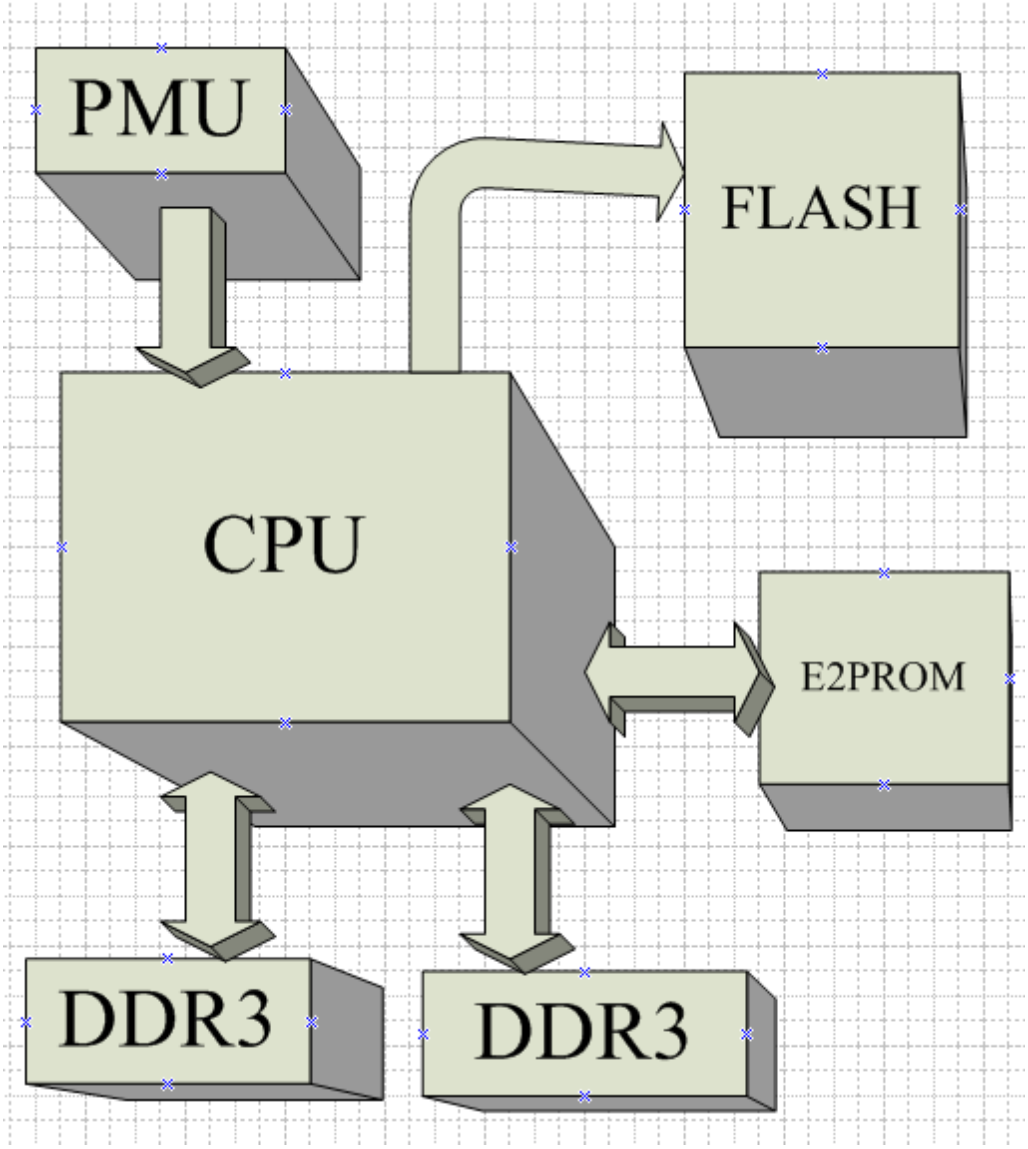
1.2 FET335xS-II CPU Module Block Diagram



1.3 FET335xS-II CPU Module Electricity Features

1.3.1 Electricity Parameter

Power Supply: DC5V ± 10%

Temperature Range:-40 – 85 ℃(Industrial)

Humility:10 – 90%（Non-condensed）

1.3.2 Power Consumption Parameter

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Test Environment: Under normal temperature condition

Hardware platform: FET335xS-II CPU Module

Application program: Linux OS, Video test program

Test Tools: Multi-functional and adjustable DC power supply

Main Components on CPU module:

CPU: AM3354BZCZD80

DDR3:MT41J64M16JT-15E IT

NAND FLASH: MT29F2G08ABAEAWP-IT

POWER IC: TPS650250RHBR, RT8059GJ5

E2PROM:DS2460S

Test procedures: Add DC5V power supply to FET335xS-II CPU module with Linux OS,test and record power consumption data when test different application programs.

Test results:

Operation condition	Power Supply	Current Value	Current Peak Value	Power Consumption
Only running with Linux OS,NO more any other input operations	5V	150mA	——	0.75W
Only running with Linux OS + Video broadcast	5V	200mA	——	1W

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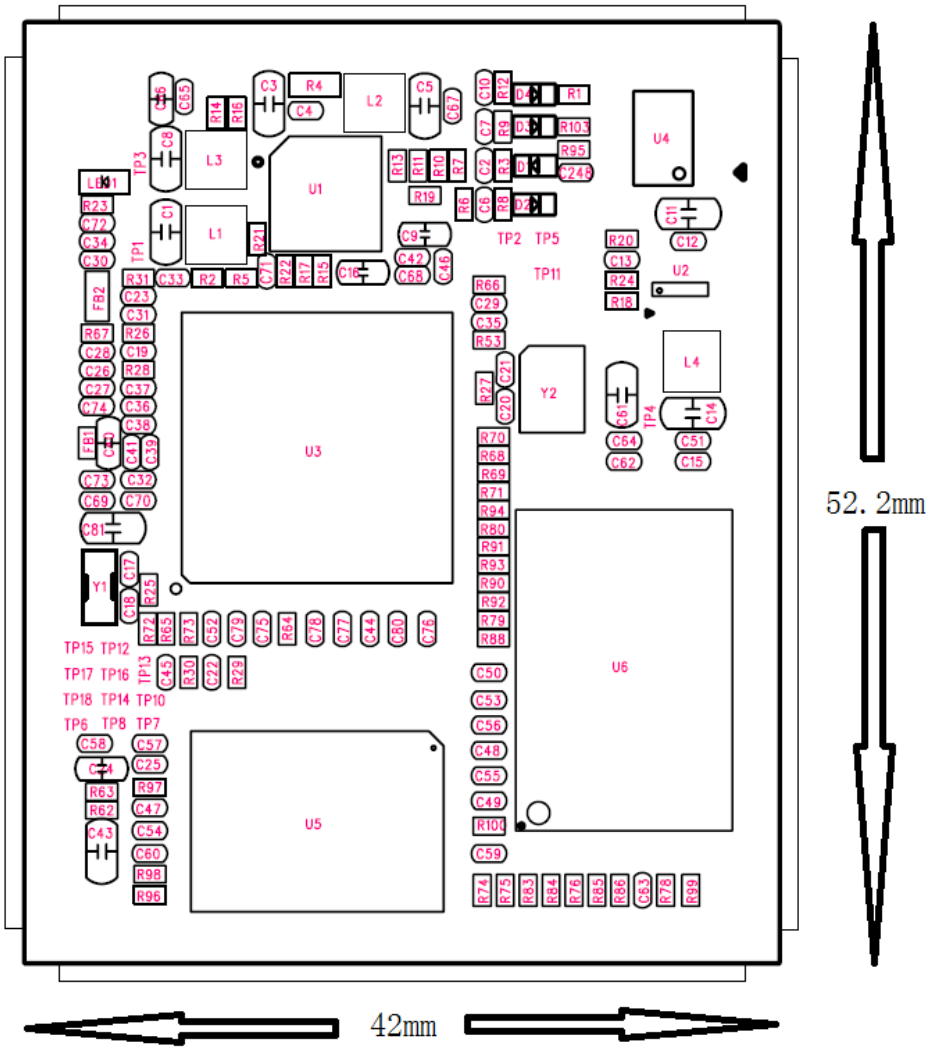
1.4 FET335xS-II CPU Module Size



1.5 Application Fields

OK335xS-II could be applied to portable data terminal, navigation, game devices, smart home, industrial automation, consumer medical apparatus and instruments, printer and intelligent charging system, test devices, education console, toys etc.

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Chapter2 FET335xS-II CPU Module Introduction

2.1 FET335xS-II CPU Module Boot Configuration

FET335xS-II CPU module is default to boot from NAND FLASH. When booting from Nand flash, pins status is as follows:

Pin Name	High/Low Voltage Level
SYS_BOOT0	1
SYS_BOOT1	1
SYS_BOOT2	0
SYS_BOOT3	0
SYS_BOOT4	1
SYS_BOOT5	0
SYS_BOOT6	0
SYS_BOOT7	1
SYS_BOOT8	0
SYS_BOOT9	1
SYS_BOOT10	0
SYS_BOOT11	0
SYS_BOOT12	0
SYS_BOOT13	0
SYS_BOOT14	1
SYS_BOOT15	0

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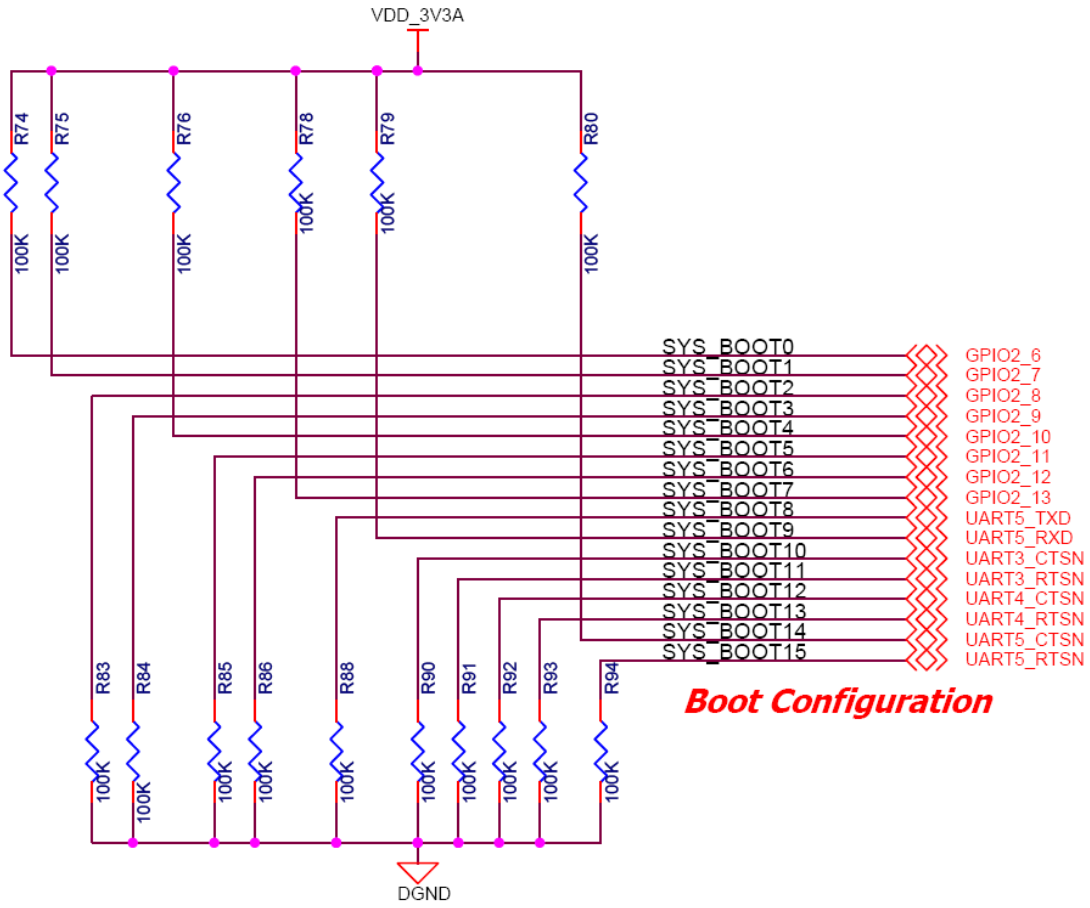
Boot configuration schematic is as follows:



Considering there are too many pins are used for FET335xS-II boot configuration, Forlinx modified and improve something on Boot method.CPU boot method only could be changed via modification on one signal status (Chip select status need to be modified when the board is powered).Boot keys should refers to the base board boot instruction.

2.2 FET335xS-II CPU Module Pin Definition

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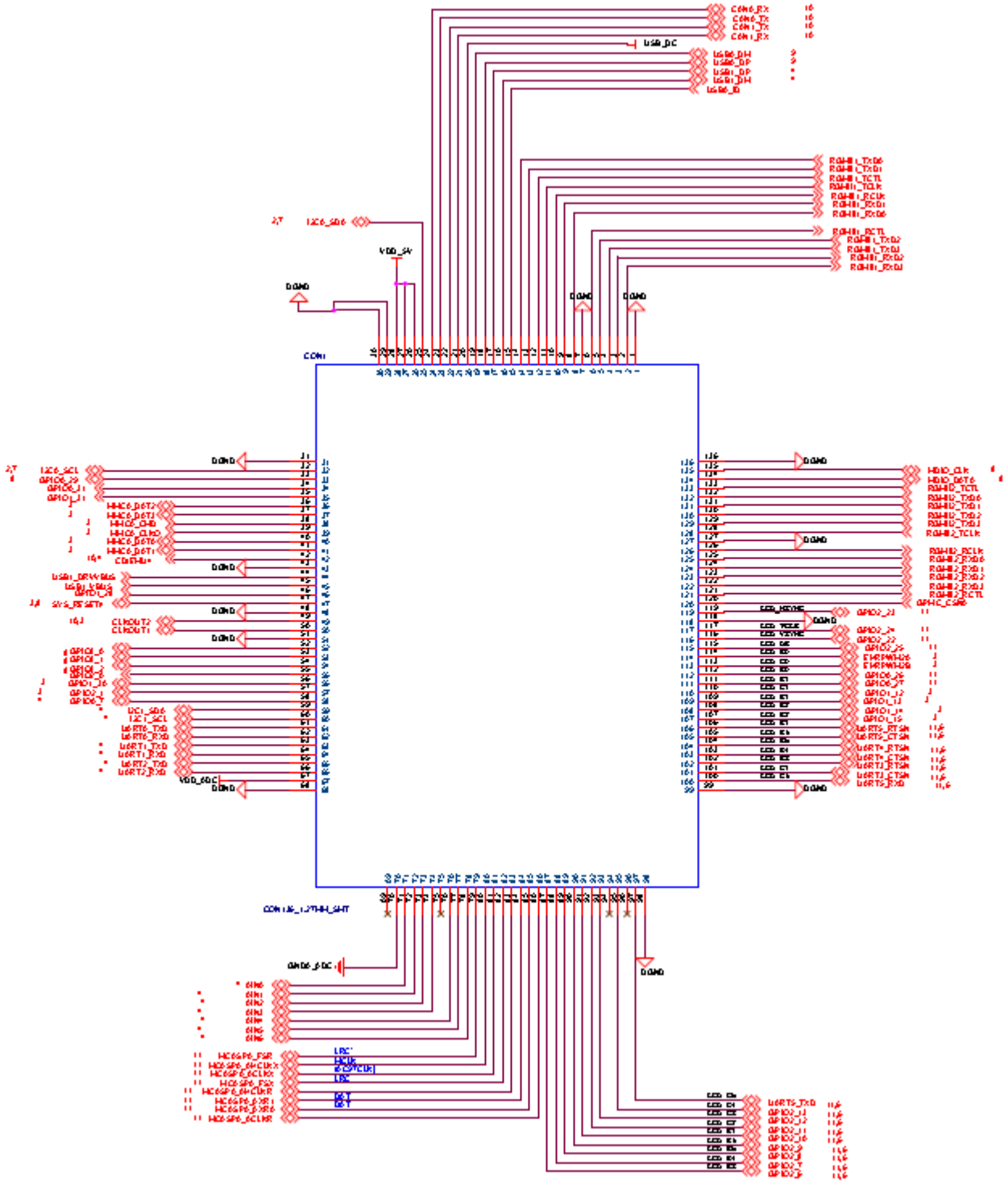

2.3 FET335xS-II CPU Module Pin Definition

FET335xS-II CPU module pin are derived to Base board via 136 pins with the pitch of 1.27mm.

2.3.1 FET335xS-II CPU Module Pin Definition List

We strongly suggest users to develop products base on default function of CPU module. Default software provided by Forlinx could be directly opened to run on the board. Generally speaking, default function of CPU module could basically satisfy the requirements. Besides, users also could select the multiplexed function according to special demands and integrates with PinMux tools to configure pin function.

Pin	Ball	Pin Name	V	Description
1	NC	DGND	0	Digital ground
2	L17	RGMII1_RXD3	3.3	RGMII1 receive data3
		UART3_RXD	3.3	UART3 receive data
		GMII1_RXD3	3.3	MII1 receive data3
		MMC0_DAT5	3.3	MMC/SD/SDIO data
		MMC1_DAT2	3.3	MMC/SD/SDIO data
		UART1_DTRN	3.3	UART1 data set ready
		MCASP0_AXR0	3.3	McASP0 serial data
		GPIO2_18	3.3	General purpose IO
3	L16	RGMII1_RXD2	3.3	RGMII1 receive data2
		UART3_TXD	3.3	UART3 transmit data
		GMII1_RXD2	3.3	MII1 receive data2
		MMC0_DAT4	3.3	MMC/SD/SDIO data
		MMC1_DAT3	3.3	MMC/SD/SDIO data
		UART1_RIN	3.3	UART1 Ring indicator
		MCASP0_AXR1	3.3	McASP0 serial data
		GPIO2_19	3.3	General purpose IO
4	J18	RGMII1_TXD3	3.3	RGMII transmit data3
		DCAN0_TX	3.3	DCAN0 transmit data
		GMII1_TXD3	3.3	MII1transmit data3
		UART4_RXD	3.3	UART4 receive data
		MCASP1_FSX	3.3	McASP1transmit frame sync.
		MMC2_DAT1	3.3	MMC/SD/SDIO data
		MCASP0_FSR	3.3	McASP0receive frame sync.
		GPIO0_16	3.3	General purpose IO
5	K15	RGMII1_TXD2	3.3	RGMII1 transmit data2
		DCAN0_RX	3.3	DCAN0 receive data
		GMII1_TXD2	3.3	MII1 transmit data2
		UART4_TXD	3.3	UART4 transmit data
		MCASP1_AXR0	3.3	McASP1 serial data

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		MMC2_DAT2	3.3	MMC/SD/SDIO data
		MCASP0_AHCLKX	3.3	McASP0 transmit master clock
		GPIO0_17	3.3	General purpose IO
6	J17	RGMII1_RCTL	3.3	RGMII1 receive control
		LCD_MEMORY_CLK	3.3	LCD main clock
		RGMII1_RXDV	3.3	MII1 receive data available
		UART5_TXD	3.3	UART5 transmit data
		MCASP1_ACLKX	3.3	McASP1 transmit bit clock
		MMC2_DAT0	3.3	MMC/SD/SDIO data
		MCASP0_ACLKR	3.3	McASP0 receive bit clock
		GPIO3_4	3.3	General purpose IO
7	NC	DGND	0	Digital ground
8	M16	RGMII1_RXD0	3.3	RGMII1 receive data0
		RMII 1_RXD0	3.3	RMII1 receive data0
		GMII1_RXD0	3.3	MII1 receive data0
		MCASP1_AHCLKX	3.3	McASP1 transmit master clock
		MCASP1_AHCLKR	3.3	McASP1 receive master clock
		MCASP1_ACLKR	3.3	McASP1 receive bit clock
		MCASP0_AXR3	3.3	McASP0 serial data
		GPIO2_21	3.3	General purpose IO
9	L15	RGMII1_RXD1	3.3	RGMII receive data1
		RMII1_RXD1	3.3	RMII receive data1
		GMII1_RXD1	3.3	MII1receive data1
		MCASP1_AXR3	3.3	McASP1serial data
		MCASP1_FSR	3.3	McASP1receive frame sync.
		EQEP0_STROBE	3.3	eQEP0 strobe
		MMC2_CLK	3.3	MMC/SD/SDIO clock
		GPIO2_20	3.3	General purpose IO
10	L18	RGMII1_RCLK	3.3	RGMII1 receive clock
		UART2_TXD	3.3	UART2 transmit data
		GMII1_RXCLK	3.3	MII1receive data
		MMC0_DAT6	3.3	MMC/SD/SDIO data
		MMC1_DAT1	3.3	MMC/SD/SDIO data
		UART1_DSRN	3.3	UART1 data set ready
		MCASP0_FSX	3.3	McASP0 transmit frame sync
		GPIO3_10	3.3	General purpose IO
11	K18	RGMII1_TCLK	3.3	RGMII transmit clock
		UART2_RXD	3.3	UART2 receive data
		GMII1_TXCLK	3.3	GMII1 transmit clock
		MMC0_DAT7	3.3	MMC/SD/SDIO data7
		MMC1_DAT0	3.3	MMC/SD/SDIO data0
		UART1_DCDN	3.3	UART1data carrier detect

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		MCASP0_ACLKX	3.3	McASP0 transmit bit clock
		GPIO3_9	3.3	General purpose IO
12	J16	RGMII1_TCTL	3.3	RGMII1transmit control
		MII1_TXEN	3.3	MII1 transmit enable
		GMII1_TXEN	3.3	GMII1 transmit enable
		TIMER4	3.3	Timer4/PWM output
		MCASP1_AXR0	3.3	McASP1 transmit/receive pin
		EQEP0_INDEX	3.3	eQEP0 index
		MMC2_CMD	3.3	MMC/SD/SDIO command
		GPIO3_3	3.3	General purpose IO
13	K16	RGMII1_TXD1	3.3	RGMII1
		GMII1_TXD1	3.3	GMII1
		RMII1_TXD1	3.3	RMII1
		MCASP1_AXR1	3.3	McASP1
		MCASP1_FSR	3.3	McASP1
		EQEP0A_IN	3.3	eQEP0
		MMC1_CMD	3.3	MMC/SD/SDIO
		GPIO0_21	3.3	General purpose IO
14	K17	RGMII1_TXD0	3.3	RGMII1transmit data0
		RMII1_TXD0	3.3	RMII1
		GMII1_TXD0	3.3	MII1
		MCASP1_AXR2	3.3	McASP1 serial data
		MCASP1_ACLKR	3.3	McASP1
		EQEP0B_IN	3.3	eQEP0B
		MMC1_CLK	3.3	MMC/SD/SDIO clock
		GPIO0_28	3.3	General purpose IO
		MCASP1_AXR2	3.3	McASP1transmit/receive pin
15	P16	USB0_ID	3.3	USB0 OTG identification
16	R18	USB1_DM		USB1 data-
17	R17	USB1_DP		USB1 data+
18	N17	USB0_DP		USB0 data+
19	N18	USB0_DM		USB0 data-
20		USB_DC	+5V	TPS65217C USB power supply
21	E17	CAN1_RX	3.3	DCAN1 receive
		UART4_TXD	3.3	UART4 transmit
		UART0_RTS	3.3	UART0 request to send
		I2C1_SCL	3.3	I2C1 clock
		SPI1_D1	3.3	SPI1 data1
		SPI1_CS0	3.3	SPI1 chip select
		PR1_EDC_SYNC1_OUT *	3.3	PRU_ edc_sync1_out data output
		GPIO1_9	3.3	I2C1 clock

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22	E18	CAN1_TX	3.3	DCAN1 transmit
		UART4_RXD	3.3	UART4 receive
		UART0_CTS	3.3	UART0 clear to transmit
		I2C1_SDA	3.3	I2C1 data line
		SPI1_D0	3.3	SPI1 data0
		TIMER7	3.3	Timer7/PWM output
		PR1_EDC_SYNC0_OUT *	3.3	PRU_ edc_sync0_out data output
		GPIO1_8	3.3	General purpose IO
23	D18	CAN0_TX	3.3	DCAN0 transmit data
		TIMER6	3.3	Timer6/PWM output
		UART1_CTS	3.3	UART1clear to transmit
		I2C2_SDA	3.3	I2C2 data line
		SPI1_CS0	3.3	SPI1 chip select
		PR1_UART0_CTS_N*	3.3	PRU_UART0 clear to transmit
		PR1_EDC_LATCH0_IN*	3.3	PRU data input
		GPIO0_12	3.3	General purpose IO
24	D17	CAN0_RX	3.3	DCAN0 receive data
		TIMER5	3.3	Timer5/PWM output
		UART1_RTS	3.3	UART1 request to send
		I2C2_SCL	3.3	I2C2 clock
		SPI1_CS1	3.3	SPI1 chip select
		PR1_UART0_RTS_N*	3.3	PRU_UART0 request to send
		PR1_EDC_LATCH1_IN*	3.3	PRU data input
		GPIO0_13	3.3	General purpose IO
25	NC	I2C0_SDA	3.3	I2C0_SDA data line
26	NC	VDD_5V	5	DC5V power supply
27	NC	VDD_5V	5	DC5V power supply
28	NC	VDD_5V	5	DC5V power supply
29	NC	DGND	0	Digital ground
30	NC	DGND	0	Digital ground
31	NC	DGND	0	Digital ground
32	NC	I2C0_SCL		I2C0 serial clock
33	H18	GPIO0_29	3.3	General purpose IO
		RGMII1_REFCLK	3.3	MII1 reference clock
		XDMA_EVENT_INTR2	3.3	External DMA interrupt pin2
		SPI1_CS0	3.3	SPI1 chip slect
		UART5_TXD	3.3	UART5 transmit data
		MCASP1_AXR3	3.3	McASP1 serial data
		MMC0_POW	3.3	MMC/SD/SDIO power supply control
		MCASP1_AHCLKX	3.3	McASP1transmit master clock
34	U17	GPIO0_31	3.3	General purpose IO
		GPMC_WPN	3.3	GPMC write protect

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		GMII2_RXERR	3.3	MII2 receive data error
		GPMC_CSN5	3.3	GPMC chip select
		RMII2_RXERR	3.3	RMII2 receive data error
		MMC2_SDCD	3.3	MMC/SD/SDIO detect
		PR1_MII1_TXEN	3.3	MII1 transmit enable
		UART4_TXD	3.3	UART4 transmit data
35	V9	GPIO1_31	3.3	General purpose IO
		GPMC_CS2n	3.3	GPMC chip select
		GPMC_BE1N	3.3	GPMC upper byte enable
		MMC1_CMD	3.3	MMC/SD/SDIO command
		PR1_EDIO_DATA_IN7*	3.3	PRU data input
		PR1_EDIO_DATA_OUT7*	3.3	PRU data output
		PR1_PRU1_PRU_R30_13*	3.3	PRU data output
		PR1_PRU1_PRU_R31_13*	3.3	PRU data input
36	F18	MMC0_DAT2	3.3	MMC/SD/SDIO data2
		GPMC_A21	3.3	GPMC address21
		UART4_RTSN	3.3	UART4 request to send
		TIMER6	3.3	Timer6/PWM output
		UART1_DSRN	3.3	UART1 data set ready
		PR1_PRU0_PRU_R30_9*	3.3	PRU data output
		PR1_PRU0_PRU_R31_9*	3.3	PRU data input
		GPIO2_27	3.3	General purpose IO
37	F17	MMC0_DAT3	3.3	MMC/SD/SDIO address3
		GPMC_A20	3.3	GPMC address 20
		UART4_CTSN	3.3	UART clear to transmit
		TIMER5	3.3	Timer5/PWM output
		UART1_DCDN	3.3	UART1 data carrier detect
		PR1_PRU0_PRU_R30_8*	3.3	PRU data output
		PR1_PRU0_PRU_R31_8*	3.3	PRU data input
		GPIO2_26	3.3	General purpose IO
38	G18	MMC0_CMD	3.3	MMC/SD/SDIO command
		GPMC_A25	3.3	GPMC address output25
		UART3_RTSN	3.3	UART3 request to send
		UART2_TXD	3.3	UART2 transmit data
		DCAN1_RX	3.3	DCAN1 receive data
		PR1_PRU0_PRU_R30_13*	3.3	PRU data output
		PR1_PRU0_PRU_R31_13*	3.3	PRU data input
		GPIO2_31	3.3	General purpose IO
39	G17	MMC0_CLKO	3.3	MMC/SD/SDIO clock
		GPMC_A24	3.3	GPMC address24
		UART3_CTSN	3.3	UART3 clear to send
		UART2_RXD	3.3	UART2 receive data

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		DCAN1_TX	3.3	DCAN1 transmit data
		PR1_PRU0_PRU_R30_12*	3.3	PRU data input
		PR1_PRU0_PRU_R31_12*	3.3	PRU data input
		GPIO2_30	3.3	General purpose IO
40	G16	MMC0_DAT0	3.3	MMC/SD/SDIO data0
		GPMC_A23	3.3	GPMC address 23
		UART5_RTSN	3.3	UART5 request to send
		UART3_TXD	3.3	UART3 transmit data
		UART1_RIN	3.3	UART1 ring indication
		PR1_PRU0_PRU_R30_11*	3.3	PRU data output
		PR1_PRU0_PRU_R31_11*	3.3	PRU data input
		GPIO2_29	3.3	General purpose IO
41	G15	MMC0_DAT1	3.3	
		gpmc_a22	3.3	GPMC address22
		uart5_ctsn	3.3	UART5 clear to send
		uart3_rxd	3.3	UART3 receive data
		uart1_dtrn	3.3	UART1data terminal ready
		pr1_pru0_pru_r30_10*	3.3	PRU transmit data
		pr1_pru0_pru_r31_10*	3.3	PRU receive data
		GPIO2_28	3.3	General purpose IO
42	C15	CD/EMU4	3.3	SD Card detect
		eCAP1_in_PWM1_out	3.3	Enhanced capture module 1 input or auxiliary PWM1 output
		mmc0_pow	3.3	MMC/SD0 power supply control
		xdma_event_intr2	3.3	External DMA interrupt 2
		mmc0_sdcd	3.3	MMC/SD/SDIO card detect
		SPI0_CS1	3.3	SPI0 chip select
		uart3_rxd	3.3	UART3 receive data
		gpio0_6	3.3	General purpose IO
43		GND	0	Ground
44	F15	USB1_DRVVBUS	3.3	USB1 BUS supply control
		GPIO3_13	3.3	General purpose IO
45	T18	USB1_VBUS	5.0	USB1 BUS power supply
46	U18	GPIO1_28	3.3	General purpose IO
		GPMC_BE1N	3.3	GPMC upper byte enable
		GMII2_COL	3.3	GMII2 collision detect
		GPMC_CSN6	3.3	GPMC bus chip select
		MMC2_DAT3	3.3	MMC2 data
		GPMC_DIR	3.3	GPMC bus signal direction control
		PR1_MII1_RXLINK	3.3	MII1 receive link
		MCASP0_ACLKR	3.3	McASP0 receive bit clock
47	NC	SYS_RESETN	3.3	system reset signal

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48	NC	DGND	0	Digital ground
49	D14	CLKOUT2	3.3	Clock output2
		EVENT_INT1	3.3	External DMA interrupt1
		TCLKIN	3.3	Clock input
		TIMER7	3.3	Timer7 / PWM output
		PR1_PRU0_PRU_R31_16*	3.3	PRU data input
		EMU3	3.3	Misc emulation3
		GPIO0_20	3.3	General purpose IO
50	A15	CLKOUT1	3.3	Clock output1
		EVENT_INTR0	3.3	External DMA interrupt 0
		TIMER4	3.3	Timer5 / PWM output
		SPI1_CS1	3.3	SPI1 chip select
		PR1_PRU1_PRU_R31_16*	3.3	PRU data input
		EMU2	3.3	MISCemulation2
		GPIO0_19	3.3	General purpose IO
51	NC	DGND	0	Digital ground
52	H16	GPIO3_0	3.3	General purpose IO
		RGMII1_COL	3.3	MII1 collision detect
		RMII2_REFCLK	3.3	RMII2 reference clock
		SPI1_SCLK	3.3	SPI1 clock
		UART5_RXD	3.3	UART5 receive data
		MCASP1_AXR2	3.3	McASP1 serial data
		MMC2_DAT3	3.3	MMC/SD/SDIO data3
		MCASP0_AXR2	3.3	McASP0 serial data
53	H17	GPIO3_1	3.3	General purpose IO
		RGMII1_CRS	3.3	MII1 carrier sense
		RMII1_CRS	3.3	RMII1 carrier sense
		SPI1_D0	3.3	SPI1 data
		I2C1_SDA	3.3	I2C1 data
		MCASP1_ACLKX	3.3	McASP1 transmit bit clock
		UART5_CTSN	3.3	UART5 clear to send
54	J15	GPIO3_2	3.3	General purpose IO
		RGMII1_RXERR	3.3	MII1 receive data error indication
		RMII1_RXERR	3.3	RMII1 receive data error indication
		SPI1_D1	3.3	SPI1 data
		I2C1_SCL	3.3	I2C1 clock
		MCASP1_FSX	3.3	McASP1send frame sync.
		UART5_RTSN	3.3	UART5 request to send
		UART2_TXD	3.3	UART2 transmit data
55	T13	GPIO2_0	3.3	General purpose IO
		GPMC_CSN3	3.3	GPMC chip select
		GPMC_A3	3.3	GPMC address 3

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		RMII2_CRS_DV	3.3	RMII2 carrier sense/Data valid
		MMC2_CMD	3.3	MMC/SD/SDIO command
		PR1_MII0_CRS*	3.3	PRU_MII carrier sense
		PR1_MDIO_DATA*	3.3	MDIO data
		EMU4	3.3	Emulation4
56	U9	GPIO1_30	3.3	General purpose IO
		GPMC_CSN1	3.3	GPMC chip select
		GPMC_CLK	3.3	GPMC clock
		MMC1_CLK	3.3	MMC/SD/SDIO clock
		PR1_EDIO_DATA_IN6*	3.3	PRU data input
		PR1_EDIO_DATA_OUT6*	3.3	PRU data output
		PR1_PRU1_PRU_R30_12*	3.3	PRU data output
		PR1_PRU1_PRU_R31_12*	3.3	PRU data input
57	V12	GPIO2_1	3.3	General purpose IO
		GPMC_CLK	3.3	GPMC clock
		LCD_MEMORY_CLK	3.3	LCD mater clock
		GPMC_WAIT1	3.3	GPMC wait
		MMC2_CLK	3.3	MMC/SD/SDIO clock
		PR1_MII1_CRS*	3.3	PRU_MII carrier sense
		PR1_MDIO_MDCLK*	3.3	PRU_MDIO clock
		MCASP0_FSR	3.3	McASP0 receive frame sync
58	C18	GPIO0_7	3.3	General purpose IO
		LCD_ENBKL	3.3	LCD backlight control（PWM0 output）
		UART3_TXD	3.3	UART3 transmit data
		SPI1_CS1	3.3	SPI1 chip select1 output when master,input when slave
		PR1_ECAP0_ECAP_CAPIN_APWM_0*	3.3	Enhanced capture module 0 input or auxiliary PWM0 output
		SPI1_SCLK	3.3	SPI1 clock
		MMC0_SDWP	3.3	MMC/SD/SDIO write protect
		XDMA_EVENT_INTR2	3.3	External DMA interrupt2
59	B16	I2C1_SDA	3.3	UART1 receive serial data
		SP10_D1	3.3	I2C1 data
		MMC1_SDWP	3.3	MMC/SD/SDIO
		EHRPWM0_TRIPZONE_INPUT	3.3	DCAN1 transmit
		PR1_EDIO_DATA_IN0	3.3	PRU
		PR1_EDIO_DATA_OUT0	3.3	PRU
		PR1_UART0_TXD	3.3	PRU_UART0 output data
		GPIO0_4	3.3	General purpose IO
60	A16	I2C1_SCL	3.3	I2C1_SCL
		SP10_CS0	3.3	SP10 chip select0
		MMC2_SDWP	3.3	MMC/SD/SDIO
		EHRPWM0_SYNCI_O	3.3	EHRPWM sync signal

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		PR1_UART0_TXD	3.3	PRU_UART0 transmit data
		PR1_EDIO_DATA_IN1	3.3	PRU
		PR1_EDIO_DATA_OUT1	3.3	PRU
		GPIO0_5	3.3	General purpose IO
61	E16	UART0_TXD	3.3	UART0 transmit data
		SPI1_CS1	3.3	SPI1 chip select
		DCAN0_RX	3.3	DCAN0 receive data
		I2C2_SCL	3.3	I2C2 serial clock
		ECAP1_IN_PWM1_OUT	3.3	Enhanced capture module1 input or auxiliary PWM1 output
		PR1_PRU1_PRU_R30_15*	3.3	PRU data output
		PR1_PRU1_PRU_R31_15*	3.3	PRU data input
		GPIO1_11	3.3	General purpose IO
62	E15	UART0_RXD	3.3	UART0 receive data
		SPI1_CS0	3.3	SPI1 chip select
		DCAN0_TX	3.3	DCAN0 transmit
		I2C2_SDA	3.3	I2C2 serial data
		ECAP2_IN_PWM2_OUT	3.3	Enhanced capture module2 input or auxiliary PWM2 output
		PR1_PRU1_PRU_R30_14*	3.3	PRU data output
		PR1_PRU1_PRU_R31_14*	3.3	PRU data input
		GPIO1_10	3.3	General purpose IO
63	D15	UART1_TXD	3.3	UART1 transmit data
		MMC2_SDWP	3.3	MMC/SD/SDIO write protect
		DCAN1_RX	3.3	DCAN1 receive
		I2C1_SCL	3.3	I2C1 clock
		PR1_UART0_TXD*	3.3	PRU_UART0 transmit data
		PR1_PRU0_PRU_R31_16*	3.3	PRU data input
		GPIO0_15	3.3	General purpose IO
64	D16	UART1_RXD	3.3	UART1 receive data
		MMC1_SDWP	3.3	MMC/SD/SDIO write protect
		DCAN1_TX	3.3	DCAN1transmit data
		I2C1_SDA	3.3	I2C1 serial data
		PR1_UART0_RXD*	3.3	PRU_UART0 receive data
		PR1_PRU1_PRU_R31_16*	3.3	PRU data input
		GPIO0_14	3.3	General purpose IO
65	B17	UART2_TXD	3.3	UART2 transmit data
		I2C2_SCL	3.3	I2C2 serial clock
		EHRPWM0B	3.3	eHRPWM0 B output
		PR1_UART0_RTS_N*	3.3	PRU_ART0 request to send
		PR1_EDIO_LATCH_IN*	3.3	PRU latch input
		EMU3	3.3	Misc emulation3

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		GPIO0_3	3.3	General purpose IO
		SPI0_D0	3.3	SPI0 data
66	A17	UART2_RXD	3.3	UART2 receive data
		I2C2_SDA	3.3	I2C2 serial data
		EHRPWM0A	3.3	eHRPWM0 A output
		PR1_UART0_CTS_N*	3.3	PRU_UART clear to send
		PR1_EDIO_SOF*	3.3	PRU start of frame
		EMU2	3.3	Misc emulation2
		GPIO0_2*	3.3	General purpose IO
		SPI0_SCLK	3.3	SPI0 serial clock
67	NC	VDD_ADC	1.8	ADC power supply
68	NC	DGND	0	Digital ground
69		NC		Not connected
70		GND_ADC	0	ADC analog ground
71	B6	AIN0		Analog input0
72	C7	AIN1		Analog input1
73	B7	AIN2		Analog input2
74	A7	AIN3		Analog input3
75		NC		Not connect
76	C8	AIN4		Analog input4
77	B8	AIN5		Analog input5
78	A8	AIN6		Analog input6
79	C13	MCASP0_FSR	3.3	McASP0 receive frame sync.
		EQEP0B_IN	3.3	eQEP0Binput
		MCASP0_AXR3	3.3	mcasp0 serial data
		MCASP1_FSX	3.3	McASP1 transmit frame sync.
		EMU2	3.3	Misc emulation2
		PR1_PRU0_PRU_R30_5*	3.3	PRU0 digital output
		PR1_PRU0_PRU_R31_5*	3.3	PRU0 digital input
		GPIO3_19	3.3	General purpose IO
80	A14	MCASP0_AHCLKX	3.3	McASP0
		EQEP0_STROBE	3.3	eQEP0B
		MCASP0_AXR3	3.3	McASP0
		MCASP1_AXR1	3.3	McASP1
		EMU4	3.3	Misc emulation4
		PR1_PRU0_R30_7	3.3	PRU0 data
		PR1_PRU0_R31_7	3.3	PRU0 data
		GPIO3_21	3.3	General purpose IO
81	A13	MCASP0_ACLKX	3.3	McASP0
		EHRPWM0A	3.3	eHRPWM0A output
		SPI1_SCLK	3.3	SPI1_SCLK
		MMC0_SDCD	3.3	MMC0_SDCD

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		PR1_PRU0_R30_0	3.3	PRU0 data
		PR1_PRU0_R31_0	3.3	PRU0 data
		GPIO3_24	3.3	General purpose IO
82	B13	MCASP0_FSX	3.3	McASP0 transmit frame sync.
		EHRPWM0B	3.3	eHRPWM0Boutput
		SPI1_D0	3.3	SPI1_D0
		MMC1_SDCD	3.3	MMC1_SDCD
		PR1_PRU0_R30_1	3.3	PRU0 data
		PR1_PRU0_R31_1	3.3	PRU0 data
		GPIO3_15	3.3	General purpose IO
83	C12	MCASP0_AHCLKR	3.3	McASP0
		EHRPWM0_SYNCI_O	3.3	EHRPWM0 sync. signal
		MCASP0_AXR2	3.3	McASP0 serial data
		SPI1_CS0	3.3	SPI1_CS0
		ECAP2_IN_PWM2_OUT	3.3	ECAP-PWM output
		PR1_PRU0_R30_3	3.3	PRU0 data
		PR1_PRU0_R31_3	3.3	PRU0 data
		GPIO3_17	3.3	General purpose IO
84	D13	MCASP0_AXR1	3.3	McASP1
		EQEP0_INDEX	3.3	Eqep0
		MCASP1_AXR0	3.3	MCASP1data
		EMU3	3.3	Misc emulation3
		PR1_PRU0_R30_6	3.3	PRU0 data
		PR1_PRU0_R31_6	3.3	PRU0 data
		MCASP0_AXR1	3.3	McASP1
		GPIO3_20	3.3	General purpose IO
85	D12	MCASP0_AXR0	3.3	McASP0
		EHRPWM0_TRIPZONE_INPUT	3.3	EHRPWM0
		SPI1_D1	3.3	SPI1 data
		MMC2_SDCD	3.3	MMC2_SDCD
		PR1_PRU0_R30_2	3.3	PRU0 data
		PR1_PRU0_R31_2	3.3	PRU0 data
		GPIO3_16	3.3	General purpose IO
86	B12	MCASP0_ACLKR	3.3	McASP
		EQEP0A_IN	3.3	LCD data 12
		MCASP0_AXR2	3.3	MCASP0 serial data
		MCASP1_ACLKX	3.3	MCASP1 transmit clock
		MMC2_SDWP	3.3	MMC2_SDWP write protect
		PR1_PRU0_R30_4	3.3	PRU0 data
		PR1_PRU0_R31_4	3.3	PRU0 data
		GPIO3_18	3.3	General purpose IO
87	R1	GPIO2_6	3.3	General purpose IO

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		LCD_D0	3.3	LCD data0
		GPMC_A0	3.3	GPMC address 0
		PR1_MII_MT0_CLK*	3.3	PRU_MII transmit clock
		EHRPWM2A	3.3	eHRPWM2 A output
		PR1_PRU1_PRU_R30_0*	3.3	PRU data output
		PR1_PRU1_PRU_R31_0*	3.3	PRU data input
88	R2	GPIO2_7	3.3	General purpose IO
		LCD_D1	3.3	LCD data1
		GPMC_A1	3.3	GPMC address1
		PR1_MII0_TXEN*	3.3	PRU_MII transmit enable
		EHRPWM2B	3.3	eHRPWM2 B output
		PR1_PRU1_PRU_R30_1*	3.3	PRU data output
		PR1_PRU1_PRU_R31_1*	3.3	PRU data input
89	R3	GPIO2_8	3.3	General purpose IO
		LCD_D2	3.3	LCD data2
		GPMC_A2	3.3	GPMC address 2
		PR1_MII0_TXD3*	3.3	PRU_MII transmit data
		EHRPWM2_TRIPZONE_INPUT	3.3	eHRPWM2 quadrature input
		PR1_PRU1_PRU_R30_2*	3.3	PRU data output
		PR1_PRU1_PRU_R31_2*	3.3	PRU data input
90	R4	GPIO2_9	3.3	General purpose IO
		LCD_D3	3.3	LCD data3
		GPMC_A3	3.3	GPMC address 3
		PR1_MII0_TXD2*	3.3	PRU_MII transmit data
		EHRPWM0_SYNCO	3.3	eHRPWM0 sync output
		PR1_PRU1_PRU_R30_3*	3.3	PRU data output
		PR1_PRU1_PRU_R31_3*	3.3	PRU data input
91	T1	GPIO2_10	3.3	General purpose IO
		LCD_D4	3.3	LCDdata4
		GPMC_A4	3.3	GPMC address 4
		PR1_MII0_TXD1*	3.3	PRU_MII receive data
		EQEP2A_IN	3.3	eQEP2A quadrature input
		PR1_PRU1_PRU_R30_4*	3.3	PRU data output
		PR1_PRU1_PRU_R31_4*	3.3	PRU data input
92	T2	GPIO2_11	3.3	General purpose IO
		LCD_D5	3.3	LCD data 5
		GPMC_A5	3.3	GPMC address 5
		PR1_MII0_TXD0*	3.3	PRU_MII transmit data
		EQEP2B_IN	3.3	eQEP2B quadrature input
		PR1_PRU1_PRU_R20_5*	3.3	PRU data output
		PR1_PRU1_PRU_R31_5*	3.3	PRU data input
93	T3	GPIO2_12	3.3	General purpose IO

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		LCD_DAT6	3.3	LCD data6
		GPMC_A6	3.3	GPMC address 6
		PR1_EDIO_DATA_IN6*	3.3	PRU_data input
		EQEP2_INDEX	3.3	eQEP2 index
		PR1_EDIO_DATA_OUT6*	3.3	PRU_data output
		PR1_PRU1_PRU_R30_6*	3.3	PRU_data output
		PR1_PRU1_PRU_R31_6*	3.3	PRU_data input
94		NC		NC
95	T4	GPIO2_13	3.3	General purpose IO
		LCD_D7	3.3	LCD data7
		GPMC_A7	3.3	GPMC address7
		PR1_EDIO_DATA_IN7*	3.3	PRU_data input
		EQEP2_STROBE	3.3	qQEP2 strobe
		PR1_EDIO_DATA_OUT7*	3.3	PRU_data output
		PR1_PRU1_PRU_R30_7*	3.3	PRU_data output
		PR1_PRU1_PRU_R31_7*	3.3	PRU_data input
96		NC		NC
97	U1	LCD_D8	3.3	LCD
		GPMC_A12	3.3	GPMC address 12
		eHRPWM1_TRIPZONE_INPUT	3.3	eHRPWM1
		MCASP0_ACLKX	3.3	McASP0
		UART5_TXD	3.3	UART5 transmit data
		PR1_MII0_RXD3	3.3	PRU_MII
		UART2_CTSN	3.3	UART2
		GPIO2_14	3.3	General purpose IO
98		DGND	0	Digital ground
99		DGND	0	Digital ground
100	U2	LCD_D9	3.3	LCD
		GPMC_A13	3.3	GPMC
		Ehrpwm0_SYNC0	3.3	eHRPWM0
		MCASP0_FSX	3.3	McASP0
		UART5_RXD	3.3	UART5
		PR1_MII0_RXD2	3.3	PRU_MII
		UART2_RTSN	3.3	UART2 request to send
		GPIO2_15	3.3	General purpose IO

101	U3	LCD_D10	3.3	LCD
		GPMC_A14	3.3	GPMC
		eHRPWM1A	3.3	eHRPWM1
		MCASP0_AXR0	3.3	McASP0
		PR1_MII0_RXD1	3.3	PRU_MII

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		UART3_CTSN	3.3	UART3
		GPIO2_16	3.3	General purpose IO
102	U4	UART3_RTSN	3.3	UART3 request to send
		LCD_D11	3.3	LCDdata11
		GPMC_A15	3.3	GPMC address 15
		EHRPWM1B	3.3	eHRPWM1 B output
		MCASP0_AHCLKR	3.3	McASP0 receive high frequency mater clock
		MCASP0_AXR2	3.3	McASP0 serial data
		PR1_MII0_RXD0*	3.3	PRU_MII receive data
		GPIO2_17	3.3	General purpose IO
103	V2	LCD_D12	3.3	LCD data12
		GPMC_A16	3.3	GPMC address 16
		EQEP1A_IN	3.3	eQEP1A
		MCASP 0_ACLKR	3.3	McASP receive bit clock
		MCASP 0_AXR2		McASP0 serial data
		PR1_MII0_rxlink *		PRU_MII receive link
		UART4_CTSN	3.3	UART clear to send
		GPIO2_26	3.3	General purpose IO
104	V3	UART4_RTSN	3.3	UART4 request to send
		LCD_D13	3.3	LCD data13
		GPMC_A17	3.3	GPMC address 17
		EQEP1B_IN	3.3	eQEP1B quadrature input
		MCASP0_FSR	3.3	McASP0 receive frame sync.
		MCASP0_AXR3	3.3	McASP0 serial data
		PR1_MII0_RXER*	3.3	PRU_MII receive error
		GPIO0_9	3.3	General purpose IO
105	V4	LCD_D14	3.3	LCD data14
		GPMC_A18	3.3	GPMC address18
		EQEP1_INDEX	3.3	eQEP1 index
		MCASP0_AXR1	3.3	MCASP0 serial data
		UART5_RXD	3.3	UART5 receive data
		PR1_MII0_CLK*	3.3	PRU_MII receive clock
		UART5_CTSN	3.3	UART5 clear to send
		GPIO2_28	3.3	General purpose IO
106	T5	LCD_D15	3.3	LCD data15
		GPMC _A19	3.3	GPMC address19
		EQEP 1_ STROBE	3.3	EQEP 1 strobe
		MCASP 0_AHCLKX	3.3	McASP0 transmit high frequency master clock
		MCASP 0_AXR3	3.3	MCASP 0 data
		PR1_MII0_RXDV	3.3	PR1_MII0_RXDV receive data valid
		UART5_RTSN	3.3	UART5 request to send

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		GPIO0_11	3.3	General purpose IO
107	U13	GPIO1_15	3.3	General purpose IO
		GPMC_D15	3.3	GPMC data15
		LCD_DAT16	3.3	LCD data16
		MMC1_DAT7	3.3	MMC/SD/SDIO data
		MMC2_DAT3	3.3	MMC/SD/SDIO data
		EQEP2_STROBE	3.3	eQEP2 strobe
		PR1_ECAP0_ECAP_CAPIN_ APWM_O*	3.3	Enhanced capture input / PWM output
		PR1_PRU0_PRU_R31_15*	3.3	PRU data input
108	V13	GPIO1_14	3.3	General purpose IO
		GPMC_D14	3.3	GPMC data14
		LCD_DAT17	3.3	LCD data17
		mmc1_dat6	3.3	MMC/SD/SDIO data
		mmc2_dat2	3.3	MMC/SD/SDIO data
		eQEP2_index	3.3	eQEP2 index
		pr1_mii0_txd0*	3.3	PRU_MII transmit data
		pr1_pru0_pru_r31_14*	3.3	PRU data input
109	R12	GPIO1_13	3.3	General purpose IO
		GPMC_D13	3.3	GPMC data13
		LCD_DAT18	3.3	LCD data18
		MMC1_DAT5	3.3	MMC/SD/SDIO data
		MMC2_DAT1	3.3	MMC/SD/SDIO data
		EQEP2B_IN	3.3	eQEP2Bquadrature input
		PR1_MII0_TXD1*	3.3	PRU_MII transmit data
		PR1_PRU0_PRU_R30_15*	3.3	PRU data output
110	T12	GPIO1_12	3.3	General purpose IO
		GPMC_D12	3.3	GPMC data12
		LCD_DAT19	3.3	LCD data19
		MMC1_DAT4	3.3	MMC/SD/SDIO data
		MMC2_DAT0	3.3	MMC/SD/SDIO data
		EQEP2A_IN	3.3	eQEP2A quadrature input
		PR1_MII0_TXD2*	3.3	PRU_MII transmit data
		PR1_PRU0_PRU_R30_14*	3.3	PRU data transmit
111	U12	GPIO0_27	3.3	General purpose IO
		GPMC_D11	3.3	GPMC data11
		LCD_DAT20	3.3	LCD data20
		MMC1_DAT3	3.3	MMC/SD/SDIO data
		MMC2_DAT7	3.3	MMC/SD/SDIO data
		EHRPWM0_SYNCO	3.3	eHRPWM0 sync.output
		PR1_MII0_TXD3*	3.3	PRU_MII transmit data
112	T11	GPIO0_26	3.3	General purpose IO

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		GPMC_D10	3.3	GPMC data10
		LCD_DAT21	3.3	LCD data21
		MMC1_DAT2	3.3	MMC/SD/SDIO data
		MMC2_DAT6	3.3	MMC/SD/SDIO data
		EHRPWM2_TRIPZONE_INPUT	3.3	eHRPWM2 tripzone input
		PR1_MII0_TXEN*	3.3	PRU_MII transmit enable
113	T10	EHRPWM2B	3.3	eHRPWM2 B output
		GPMC_D9	3.3	GPMC data9
		LCD_DAT22	3.3	LCD data22
		MMC1_DAT1	3.3	MMC/SD/SDIO data
		MMC2_DAT5	3.3	MMC/SD/SDIO data
		PR1_MII0_COL*	3.3	PRU_MII collision detect
		GPIO0_23	3.3	General purpose IO
114	U10	EHRPWM2A	3.3	eHRPWM2 A output
		GPMC_D8	3.3	GPMC data8
		LCD_DAT23	3.3	LCD data23
		MMC1_DAT0	3.3	MMC/SD/SDIO data
		MMC2_DAT4	3.3	MMC/SD/SDIO data
		PR1_MII_MT0_CLK*	3.3	PRU_MII transmit clock
		GPIO0_22	3.3	General purpose IO
115	R6	GPIO2_25	3.3	General purpose IO
		GPMC_A11	3.3	GPMC address 11
		PR1_MII1_CRS*	3.3	PRU_MII carrier detect
		PR1_EDIO_DATA_IN5*	3.3	PRU data input
		PR1_EDIO_DATA_OUT5*	3.3	PRU data output
		PR1_PRU1_PRU_R30_11*	3.3	PRU data output
		PR1_PRU1_PRU_R31_11*	3.3	PRU data input
		LCD_AC_BIAS_EN	3.3	LCD AC bias enable
116	U5	GPIO2_22	3.3	General purpose IO
		LCD_VSYNC	3.3	LCD vertical sync.
		GPMC_A8	3.3	GPMC address 8
		GPMC_A1	3.3	GPMC address 1
		PR1_EDIO_DATA_IN2*	3.3	PRU data input
		PR1_EDIO_DATA_OUT2*	3.3	PRU data output
		PR1_PRU1_PRU_R30_8*	3.3	PRU data output
		PR1_PRU1_PRU_R31_8*	3.3	PRU data input
117	V5	GPIO2_24	3.3	General purpose IO
		LCD_PCLK	3.3	LCD pixel clock
		GPMC_A10	3.3	GPMC address10
		PR1_MII0_CRS*	3.3	PRU_MII carrier detect
		PR1_EDIO_DATA_IN4*	3.3	PRU data input
		PR1_EDIO_DATA_OUT4*	3.3	PRU data output

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		PR1_PRU1_PRU_R30_10*	3.3	PRU data output
		PR1_PRU1_PRU_R31_10*	3.3	PRU data input
118	NC	DGND	0	Digital ground
119	R5	GPIO2_23	3.3	General purpose IO
		LCD_HSYNC	3.3	LCD horizontal sync
		GPMC_A9	3.3	GPMC address9
		GPMC_A2	3.3	GPMC address2
		PR1_EDIO_DATA_IN3*	3.3	PRU data input
		PR1_EDIO_DATA_OUT3*	3.3	PRU data output
		PR1_PRU1_PRU_R30_9*	3.3	PRU data output
		PR1_PRU1_PRU_R31_9*	3.3	PRU data input
120	NC	GPMC_CSN0	3.3	BOOT configuration pin
121	V14	RGMII2_RCTL	3.3	RGMII2 receive control
		GPMC_A1	3.3	GPMC address 1
		GMII2_RXDV	3.3	MII2 receive data valid
		MMC2_DAT0	3.3	MMC/SD/SDIO data
		GPMC_A17	3.3	GPMC address 17
		PR1_MII1_TXD3*	3.3	MII1 transmit data3
		EHRPWM0_SYNCO	3.3	eHRPWM0 sync output
		GPIO1_17	3.3	General purpose IO
122	V16	RGMII2_RXD3	3.3	RGMII2 receive data3
		GPMC_A8	3.3	GPMC address 8
		GMII2_RXD3	3.3	MII2 receive data3
		MMC2_DAT6	3.3	MMC/SD/SDIO data
		GPMC_A24	3.3	GPMC address 4
		PR1_MII1_RXD0*	3.3	PRU_MII receive data
		MCASP0_ACLKX	3.3	McASP0 transmit clock
		GPIO1_24	3.3	General purpose IO
123	U16	RGMII2_RXD2	3.3	RGMII2 receive data2
		GPMC_A9	3.3	GPMC address 9
		GMII2_RXD2	3.3	MII2 receive data2
		MMC2_DAT7	3.3	MMC/SD/SDIO data
		GPMC_A25	3.3	GPMC address25
		PR1_MII_MR1_CLK*	3.3	PRU_MII receive clock
		MCASP0_FSX	3.3	McASP0 frame sync for transmit
		GPIO1_25	3.3	General purpose IO
124	T16	RGMII2_RXD1	3.3	RGMII2 receive data1
		GPMC_A10	3.3	GPMC address 10
		GMII2_RXD1	3.3	MII2 receive data 1
		RMII2_RXD1	3.3	RMII2 receive data1
		GPMC_A26	3.3	GPMC address 26
		PR1_MII_RXDV*	3.3	PRU_MII receive data valid

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		MCASP0_AXR0	3.3	McASP serial data output
125	V17	RGMII2_RXD0	3.3	RGMII2 receive data0
		GPMC_A11	3.3	GPMC address11
		GMII2_RXD0	3.3	MII2 receive data0
		RMII2_RXD0	3.3	RMII2 receive data0
		GPMC_A27	3.3	GPMC address27
		PR1_MII_RXER*	3.3	PRU_MII receive error
		MCASP0_AXR1	3.3	McASP serial data
		GPIO1_27	3.3	General purpose IO
126	T15	RGMII2_RCLK	3.3	RGMII2 receive clock
		GPMC_A7	3.3	GPMC address7
		GMII2_RXCLK	3.3	MII2 receive clock
		MMC2_DAT5	3.3	MMC/SD/SDIO data5
		GPMC_A23	3.3	GPMC address23
		PR1_MII1_RXD1*	3.3	PRU_MII1 receive data1
		EQEP1_STROBE	3.3	eQEP1strobe
		GPIO1_23	3.3	General purpose IO
127	NC	DGND	0	Digital ground
128	U15	RGMII2_TCLK	3.3	RGMII2 transmit clock
		GPMC_A6	3.3	GPMC address6
		GMII2_TXCLK	3.3	MII2 transmit clock
		MMC2_DAT4	3.3	MMC/SD/SDIO data
		GPMC_A22	3.3	GPMC address 22
		PR1_MII1_RXD2*	3.3	PRU_MII receive data
		EQEP1_INDEX	3.3	eQEP1 index
		GPIO1_22	3.3	General purpose IO
129	U14	RGMII2_TXD3	3.3	RGMII2 transmit data3
		GPMC_A2	3.3	GPMC address2
		GMII2_TXD3	3.3	MII2 transmit data3
		MMC2_DAT1	3.3	MMC/SD/SDIO data
		GPMC_A18	3.3	GPMC address 18
		PR1_MII1_TXD2*	3.3	PRU_MII transmit data 2
		EHRPWM1A	3.3	eHRPWM1 A output
		GPIO1_18	3.3	General purpose IO
130	T14	RGMII2_TXD2	3.3	RGMII2 transmit data2
		GPMC_A3	3.3	GPMC address3
		GMII2_TXD2	3.3	MII2 transmit data2
		MMC2_DAT2	3.3	MMC/SD/SDIO data
		GPMC_A19	3.3	GPMC address19
		PR1_MII1_TXD1*	3.3	PRU_MII transmit data1
		EHRPWM1B	3.3	eHRPWM1 B output
		GPIO1_19	3.3	General purpose IO

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131	R14	RGMII2_TXD1	3.3	RGMII2 transmit data1
		GPMC_A4	3.3	GPMC address4
		GMII2_TXD1	3.3	MII2 transmit data1
		RMII2_TXD1	3.3	RMII2 transmit data1
		GPMC_A20	3.3	GPMC address 20
		PR1_MII1_TXD0*	3.3	PRU_MII transmit data
		EQEP1A_IN	3.3	eQEP1A quadrature input
		GPIO1_20	3.3	General purpose IO
132	V15	RGMII2_TXD0	3.3	RGMII2 transmit data0
		GPMC_A5	3.3	GPMC address5
		GMII2_TXD0	3.3	RMII2 transmit data0
		RMII2_TXD0	3.3	RMII2 transmit data0
		GPMC_A21	3.3	GPMC address21
		PR1_MII1_RXD3*	3.3	PRU_MII receive data
		EQEP1B_IN	3.3	eQEP1B quadrature input
		GPIO1_21	3.3	General purpose IO
133	R13	RGMII2_TCTL	3.3	RGMII2 transmit control
		GPMC_A0	3.3	GPMC address0
		GMII2_TXEN	3.3	MII2 transmit enable
		RMII2_TXEN	3.3	RMII2 transmit enable
		GPMC_A16	3.3	GPMC address16
		PR1_MII_MT1_CLK*	3.3	PRU_MII transmit clock
		EHRPWM1_TRIPZONE_INPUT	3.3	eHRPWM1 trip zone input
		GPIO1_16	3.3	General purpose IO
134	M17	MDIO_DATA	3.3	MDIO data
		timer6	3.3	Timer6 / PWM output
		uart5_rxd	3.3	UART5 receive data
		uart3_ctsn	3.3	UART3 clear to send
		mmc0_sdcd	3.3	MMC/SD/SDIO card detect
		mmc1_cmd	3.3	MMC/SD/SDIO command
		mmc2_cmd	3.3	MMC/SD/SDIO command
		gpio0_0	3.3	General purpose IO
135	M18	MDIO_CLK	3.3	MDIO clock
		timer5	3.3	Timer5 / PWM output
		uart5_txd	3.3	UART5 transmit data
		uart3_rtsn	3.3	UART3 request to send
		mmc0_sdwp	3.3	MMC/SD/SDIO write protect
		mmc1_clk	3.3	MMC/SD/SDIO clock
		mmc2_clk	3.3	MMC/SD/SDIO clock
		gpio0_1	3.3	General purpose IO
136	NC	DGND	0	Digital ground

Note: Items with *marker represents it is not included in AM3354.

2.3.2 FET335xS-II CPU Module Power Jack

FET335xS-II CPU module integrates with highly integrated PMU (TPS650250)

Corresponding pins On CPU Module	Signal Name	Description
26,27,28	VDD5V	Power input +5V
47	SYS-RESETn	CPU module reset signal

2.4 FET335xS-II CPU Module Functions

Following pin definition is the default configuration of FET335xS-II CPU module.

2.4.1 MAC

MAC1 uses RMII signal:

Pin	Signal	Description
8	RGMII1_RXD0	RMII1 receive data 0
9	RGMII1_RXD1	RMII1 receive data 1
12	RGMII1_TCTL	RMII1 transmit enable
13	RGMII1_TXD1	RMII1 transmit data1
14	RGMII1_TXD0	RMII1 transmit data 0
33	GPIO0_29	RMII1 external clock input
53	GPIO3_1	RMII1 carrier sense/ data valid
54	GPIO3_2	RMII1 receive error

2.4.2 LCD

LCD 16-bit display mode

Pin	Signal Name	Description
87	LCD_D0	LCD data0
88	LCD_D1	LCD data1
89	LCD_D2	LCD data2
90	LCD_D3	LCD data3
91	LCD_D4	LCD data4
92	LCD_D5	LCD data5
93	LCD_D6	LCD data6
95	LCD_D7	LCD data7
97	LCD_D8	LCD data8
100	LCD_D9	LCD data9
101	LCD_D10	LCD data10
102	LCD_D11	LCD data11
103	LCD_D12	LCD data12

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104	LCD_D13	LCD data13
105	LCD_D14	LCD data14
106	LCD_D15	LCD data15
109	LCD_D18	LCD data18
110	LCD_D19	LCD data19
115	LCD_DE	LCD data enable
116	LCD_VSYNC	LCD vertical sync.
117	LCD_PCLK	LCD pixel clock
119	LCD_HSYNC	LCD horizontal sync.

2.4.3 USB

USB subsystem integrates with 2 separated USB2.0 module, USB0:device, USB1:Host

Pin	Signal Name	Description
15	USB0_ID	USB0 OTG marker
19	USB0_DM	USB0 data-
18	USB0_DP	USB0 data+
16	USB1_DM	USB1 data-
17	USB1_DP	USB1 data+
43	USB1_ID	USB1 OTG marker
44	USB1_DRVVBUS	USB1 VBUS supply control
45	USB1_VBUS	USB1_VBUS

2.4.4 ADC Input

Sampling analog voltage range: 0-1.8V.Accuracy:12Bit. Value $_{Max:}$ 4096.

Pin No.	Signal Name	Description
71	Rscreen_XLeft （AIN0）	Analog Input0 Resistive LCD touch input
72	Rscreen_XRight （AIN1）	Analog Input1 Resistive LCD touch input
73	Rscreen_Yup （AIN2）	Analog Input2 Resistive LCD touch input
74	Rscreen_YDown（AIN3）	Analog Input3 Resistive LCD touch input
76	AIN4	Analog Input4
77	AIN5	Analog Input5
78	AIN6	Analog Input6

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2.4.5 MMC / SDIO

MMC0 / SDIO0

Pin No.	Signal Name	Description
36	MMC0_ DAT2	MMC/SD/SDIO data2
37	MMC0_ DAT3	MMC/SD/SDIO data3
38	MMC0_CMD	MMC/SD/SDIO command
39	MMC0_CLK0	MMC/SD/SDIO clock
40	MMC0_DAT0	MMC/SD/SDIO data0
41	MMC0_DAT1	MMC/SD/SDIO data1
42	CD/EMU4	MMC/SD/SDIO card detect

MMC1 / SDIO1

Pin No.	Signal Name	Description
35	MMC1_CMD	SDIO command
56	MMC1_CLK	SDIO clock
107	MMC1_DATA7	SDIO databit7
108	MMC1_DATA6	SDIO databit6
109	MMC1_DATA5	SDIO databit5
110	MMC1_DATA4	SDIO databit4
111	MMC1_DATA3	SDIO databit3
112	MMC1_DATA2	SDIO databit2
113	MMC1_DATA1	SDIO databit1
114	MMC1_DATA0	SDIO databit0

2.4.16 I2C

Pin	Signal Name	Description
59	I2C1_SDA	I2C1 data
60	I2C1_SCL	I2C1 clock

2.4.7 SPI

Pin	Signal Name	Description
81	SPI1_SCLK	SPI1 clock
82	SPI1_D0	SPI1 data
83	SPI1_CS0	SPI1 chip select
85	SPI1_D1	SPI1 data

2.4.8 UART

CPU Module has 5-ch serial interface, in which UART0 is the debugging interface.

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Pin	Signal Name	Description
61	UART0_TXD	UART0 transmit data signal
62	UART0_RXD	UART0 receive data signal
63	UART1_TXD	UART1 transmit data signal
64	UART1_RXD	UART1 receive data signal
65	UART2_TXD	UART2 transmit data signal
66	UART2_RXD	UART2 receive data signal
2	UART3_RXD	UART3 receive data signal
3	UART3_TXD	UART3 transmit data signal
4	UART4_RXD	UART4 receive data signal
5	UART4_TXD	UART4 transmit data signal

2.4.9 Audio Interface

Pin	Signal Name	Description
86	MCASP0_ACLKR	Receive bit clock
84	MCASP0_AXR1	Serial data
80	MCASP0_AHCLKX	Transmit master clock
79	MCASP0_FSR	Receive frame sync

2.4.10 PWM

Pin	Signal Name	Description
58	PWM0	PWM signal0（It defaults to connect LCD backlight）
129	PWM1	PWM signal1(It defaults to connect beeper)
130	PWM2	PWM signal2（It defaults to connect pin connector）

2.4.11 GPIO

Pin	Signal Name	Description
6	GPIO3-4	General purpose IO
10	GPIO3-10	General purpose IO
11	GPIO3-9	General purpose IO
34	GPIO0-31	General purpose IO
121	GPIO1-17	General purpose IO
122	GPIO1-24	General purpose IO
124	GPIO1-26	General purpose IO

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125	GPIO1-27	General purpose IO
126	GPIO1-23	General purpose IO
128	GPIO1-22	General purpose IO
131	GPIO1-20	General purpose IO
132	GPIO1-21	General purpose IO
133	GPIO1-16	General purpose IO

2.4.12 CAN

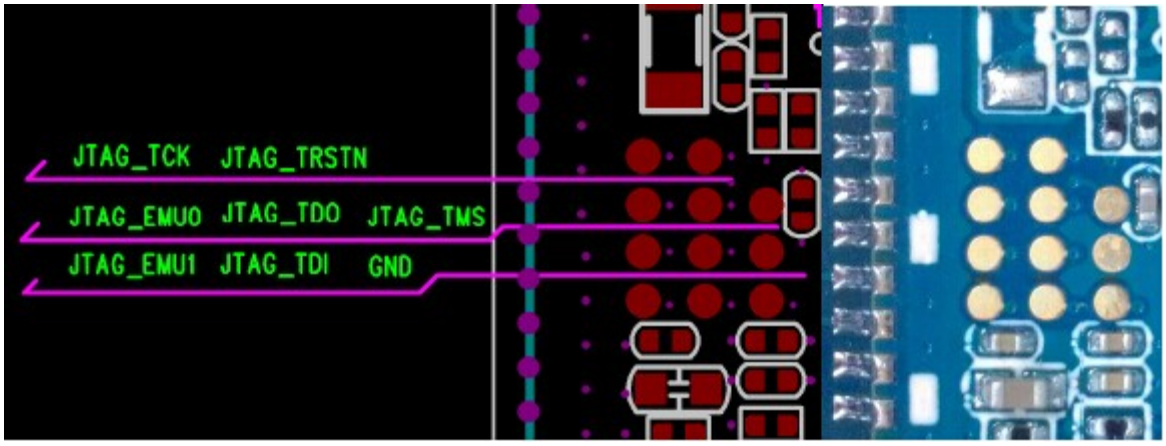
Pin No.	Signal Name	Description
23	CAN0_TX	CAN0 transmit data
24	CAN0_RX	CAN0 receive data
21	CAN1_RX	CAN1 receive data
22	CAN1_TX	CAN1 transmit data

2.4.13 JTAG

This JTAG interface is derived to the CPU Module as the test points. If JTAG function is needed, operators only need to

Pin No.	Signal Name	Description
	JTAG_TRSTn	JTAG test reset
	JTAG_TDO	JTAG test data input
	JTAG_TDI	JTAG test data input
	JTAG_TCK	JTAG Test clock
	JTAG_TMS	JTAG test mode selection
	JTAG_EMU0	MISC Emulation0
	JTAG_EMU1	MISC Emulation1

Following figure shows you the corresponding pin definition for each test point.



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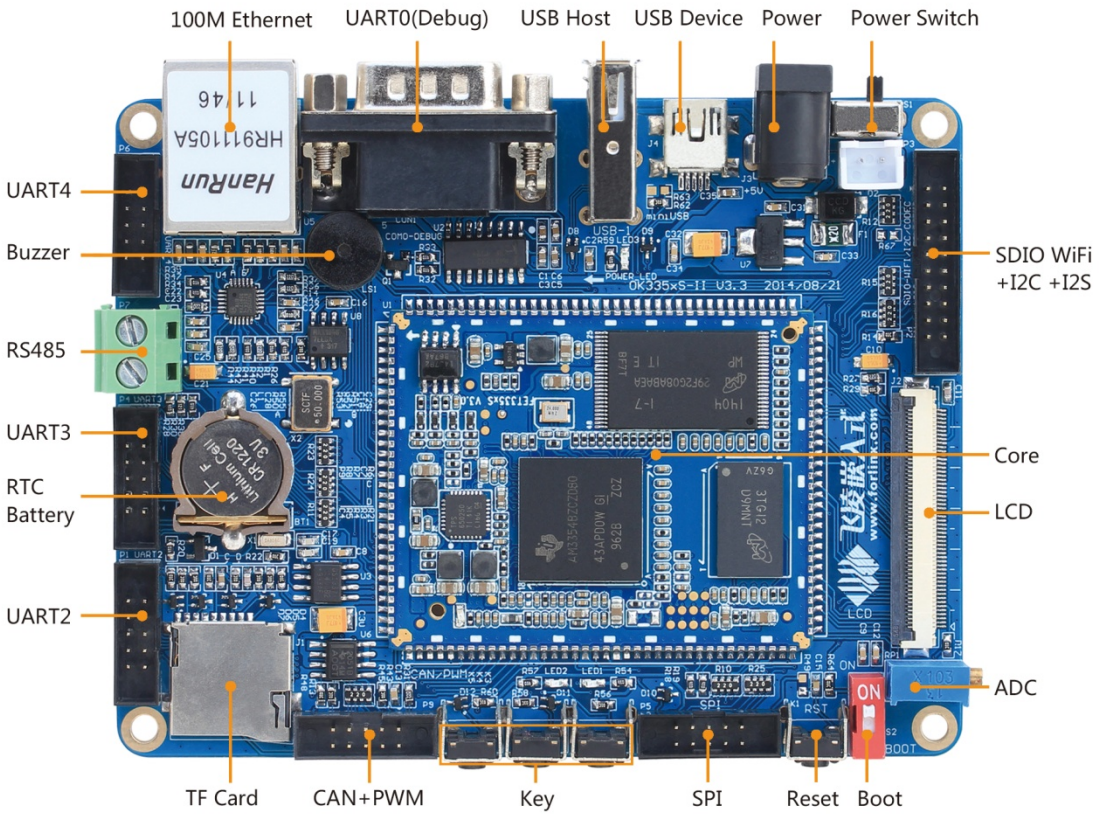
Chapter 3 OK335xS-II Base Board Introduction

3.1 OK335xS-II Base Board and Peripherals Resources

3.1.1 OK335xS-II Base Board Interfaces



OK335xS-II base board size: 104mm×81 mm. More details about location of installation holes and other details could be found from the CD-ROM link.

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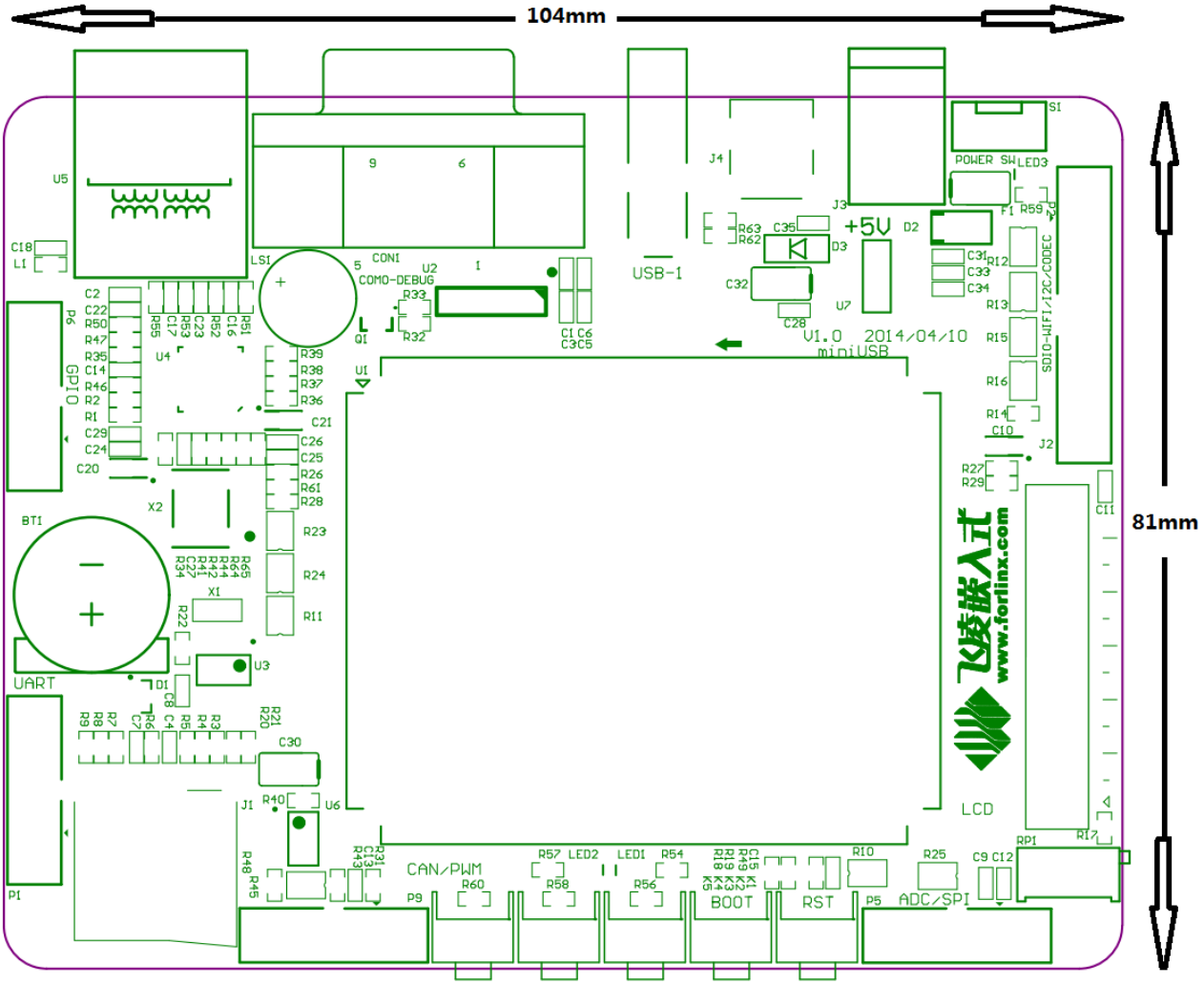
3.1.2 OK335xS-II Base Board Layout Diagram



3.1.3 OK335xS-II Base Board Function List

● 1× TFT LCD Interface
● 1× TF Card Interface
● 3× User Keys
● 2× LEDs
● 1 group of analog input interface, up to 6-ch analog input
● 1 group of I2S Audio Interface
● 5× UART (1× RS-232,3×LVCMOS（3.3V),1× RS485)
● 1×PWM
● 1× USB 2.0 HOST
● 1× USB 2.0 mini USB
● 1×SPI

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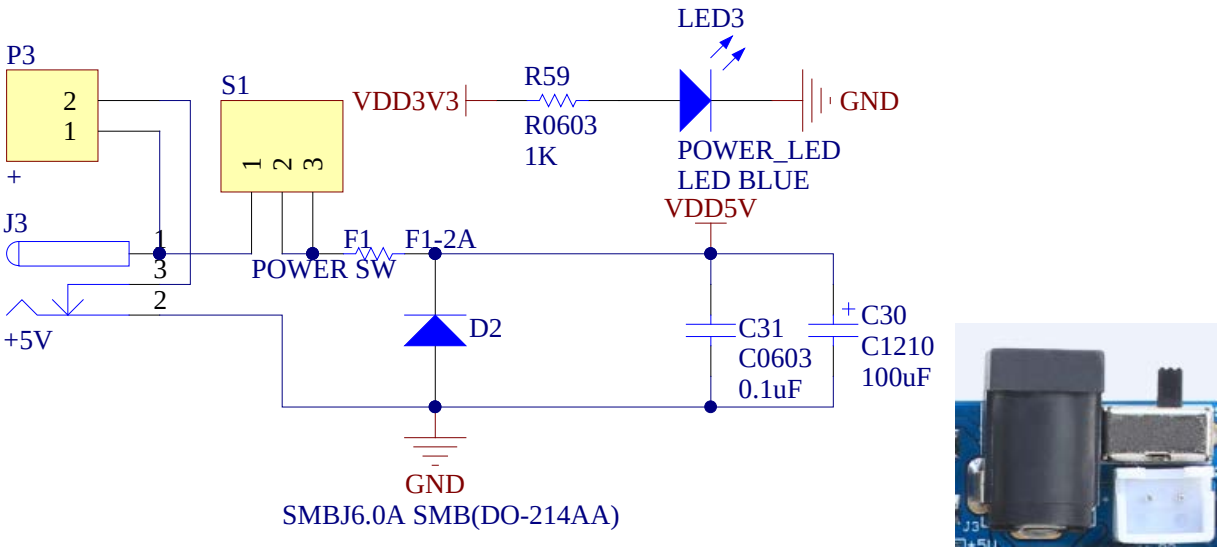
● 1×I2C (Transceiver is not included)
● 2×CAN field bus (without transceiver)
● 1×SDIO WIFI
● 1× 100 M Ethernet interface
● DC5V Power jack
● 4× GPIOs
● 1× On-board RTC DS1337

3.2 OK335xS-II Base Board Functions

3.2.1 Power Jack and Power Switch

OK335xS-II Single board computer is designed to be powered by DC5V.J3 represents power jack, could be directly connected with 5V power adapter.S1 represents power switch, and is responsible to control the power on and off. LED3 represents power indicator(Power Led).

Note: Power adaptor is specified as 5V2A, and is with internal positive and external negative interface.



3.2.2 CPU Module Connector

CPU Module and Base board is connected and soldered via stamp hole. Make sure the direction and pins are right before soldering.

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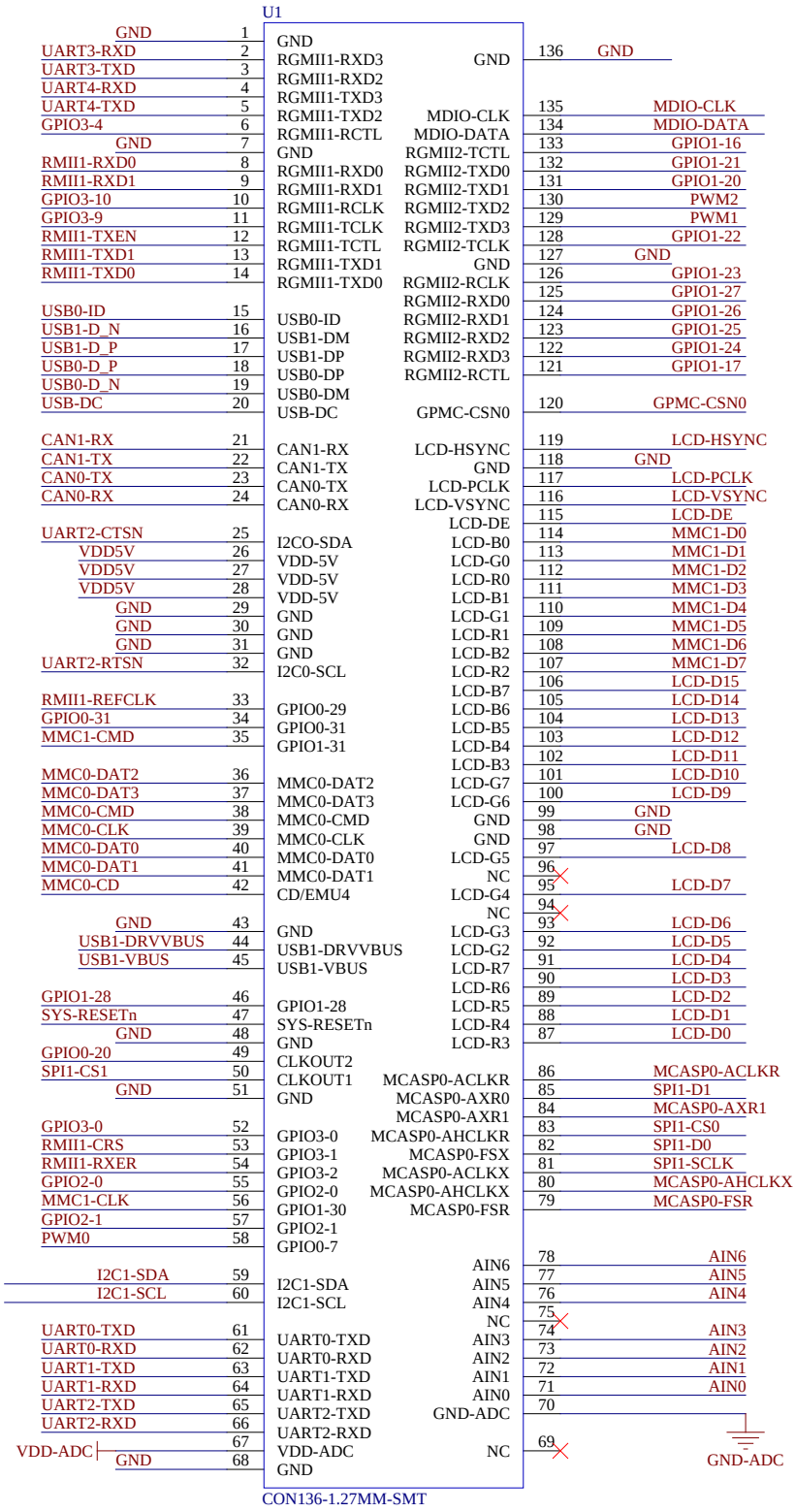

Figure 3.2.2 Schematic

Pin No.	CPU Module Signal Name	Description On Base Board
1	GND	GND
2	RGMII1_RXD3	UART3 receive data
3	RGMII1_RXD2	UART3 transmit data
4	RGMII1_TXD3	UART4 receive data
5	RGMII1_TXD2	UART4 transmit data
6	RGMII1_RCTL	GPIO3-4
7	GND	Ground
8	RGMII1_RXD0	RMII1 receive data 0
9	RGMII1_RXD1	RMII1 receive data1
10	RGMII1_RCLK	GPIO3-10
11	RGMII1_TCLK	GPIO3-9
12	RGMII1_TCTL	RMII1 transmit enable
13	RGMII1_TXD1	RMII1 transmit data1
14	RGMII1_TXD0	RMII1 transmit data0
15	USB0_ID	USB0 status detect。
16	USB1_DM	USB1 data-
17	USB1_DP	USB1 data+
18	USB0_DP	USB0 data+
19	USB0_DM	USB0 data-
20	USB_DC	External USB power supply
21	CAN1_RX	CAN1 receive data
22	CAN1_TX	CAN1 transmit data
23	CAN0_TX	CAN0 transmit data
24	CAN0_RX	CAN0 receive data
25	I2C0_SDA	NC
26	VDD5V	Power supply
27	VDD5V	Power supply
28	VDD5V	Power supply
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	I2C0_SCL	NC
33	GPIO0_29	RMII1 External clock input
34	GPIO0_31	GPIO0-31
35	GPIO1_31	MMC1 command
36	MMC0_DAT2	MMC0 data2
37	MMC0_DAT3	MMC0 data3
38	MMC0_CMD	MMC0 command
39	MMC0_CLK	MMC0 clock output
40	MMC0_DAT0	MMC0 data0

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41	MMC0_DAT1	MMC0-data1
42	CD/EMU4	MMC0-CD card detect
43	GND	GND
44	USB1_DRVVBUS	USB1 VBUS supply control
45	USB1_VBUS	USB1 VBUS power input
46	GPIO1_28	GPIO1-28
47	SYS_RESETn	System reset
48	GND	GND
49	CLKOUT2	GPIO0-20
50	CLKOUT1	SPI1 chip select
51	GND	GND
52	GPIO3_0	GPIO3-0
53	GPIO3_1	RMII1 carrier sense/data valid
54	GPIO3_2	RMII1 receive error
55	GPIO2_0	GPIO2-0
56	GPIO1_30	MMC1 clock output
57	GPIO2_1	GPIO2-1
58	GPIO0_7	PWM0 LCD backlight adjust
59	I2C1_SDA	I2C1 serial data
60	I2C1_SCL	I2C1 clock output
61	UART0_TXD	UART0 transmit data
62	UART0_RXD	UART0 receive data
63	UART1_TXD	UART1 transmit data
64	UART1_RXD	UART1 receive data
65	UART2_TXD	UART2 transmit data
66	UART2_RXD	UART2 receive data
67	VDD_ADC	Analog to digital conversion power output
68	GND	Ground
69	NC	NC
70	GND_ADC	Analog to digital conversion ground
71	AIN0	Analog input0
72	AIN1	Analog input1
73	AIN2	Analog input2
74	AIN3	Analog input3
75	NC	NC
76	AIN4	Analog input4
77	AIN5	Analog input5
78	AIN6	Analog input6
79	MCASP0_FSR	MCASP0 frame sync for receive
80	MCASP0_AHCLKX	MCASP0-AHCLKX transmit master clock
81	MCASP0_ACLKX	SPI1 clock output
82	MCASP0_FSX	SPI1 data bit 0

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83	MCASP0_AHCLKR	SPI1 chip select
84	MCASP0_AXR1	MCASP0 serial data
85	MCASP0_AXR0	SPI1-Data bit1
86	MCASP0_ACLKR	MCASP0 receive bit clock
87	LCD_R3	LCD-D0 LCD data0
88	LCD_R4	LCD-D1 LCD data1
89	LCD_R5	LCD-D2 LCD data2
90	LCD_R6	LCD-D3 LCD data3
91	LCD_R7	LCD-D4 LCD data4
92	LCD_G2	LCD-D5 LCD data5
93	LCD_G3	LCD-D6 LCD data6
94	NC	NC
95	LCD_G4	LCD-D7 LCD data7
96	NC	NC
97	LCD_G5	LCD-D8 LCD data8
98	GND	GND
99	GND	GND
100	LCD_G6	LCD-D9 LCD data9
101	LCD_G7	LCD-D10 LCD data10
102	LCD_B3	LCD-D11 LCD data11
103	LCD_B4	LCD-D12 LCD data12
104	LCD_B5	LCD-D13 LCD data13
105	LCD_B6	LCD-D14 LCD data14
106	LCD_B7	LCD-D15 LCD data15
107	LCD_R2	MMC1-D7 data bit 7
108	LCD_B2	MMC1-Data bit6
109	LCD_R1	MMC1-Data bit5
110	LCD_G1	MMC1-Data bit4
111	LCD_B1	MMC1-Data bit3
112	LCD_R0	MMC1-D2 Data bit2
113	LCD_G0	MMC1-D1 Data bit1
114	LCD_B0	MMC1-D0 Data bit0
115	LCD_DE	LCD-DE data enable
116	LCD_VSYNC	LCD-VSYNC vertical sync
117	LCD_PCLK	LCD-PCLK pixel clock
118	GND	GND
119	LCD_HSYNC	LCD-HSYNC horizontal sync.
120	GPMC_CSN0	BOOT configuration pin
121	RGMII2_RCTL	GPIO1-17
122	RGMII2_RXD3	GPIO1-24
123	RGMII2_RXD2	GPIO1-25
124	RGMII2_RXD1	GPIO1-26

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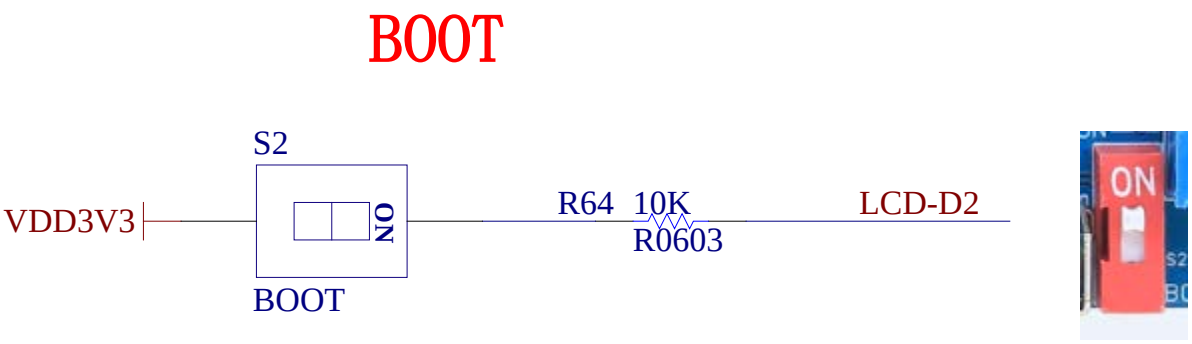
125	RGMII2_RXD0	GPIO1-27
126	RGMII2_RCLK	GPIO1-23
127	GND	GND
128	RGMII2_TCLK	GPIO1-22
129	RGMII2_TXD3	PWM1 beeper out
130	RGMII2_TXD2	PWM2 output
131	RGMII2_TXD1	GPIO1-20
132	RGMII2_TXD0	GPIO1-21
133	RGMII2_TCTL	GPIO1-16
134	MDIO_DATA	MDIO data
135	MDIO_CLK	MDIO clock
136	GND	GND

3.2.3 Boot Switch

There are two boot methods for AM335x boards.

1. Boot from Nandflash.(Switch to OFF)

2. Boot from TF card. (Switch to ON)



3.2.4 LCD

OK335xS-II single board computer provide a general purpose 54 pin LCD interface which could be used to connect with different sized resistive and capacitive LCDs.

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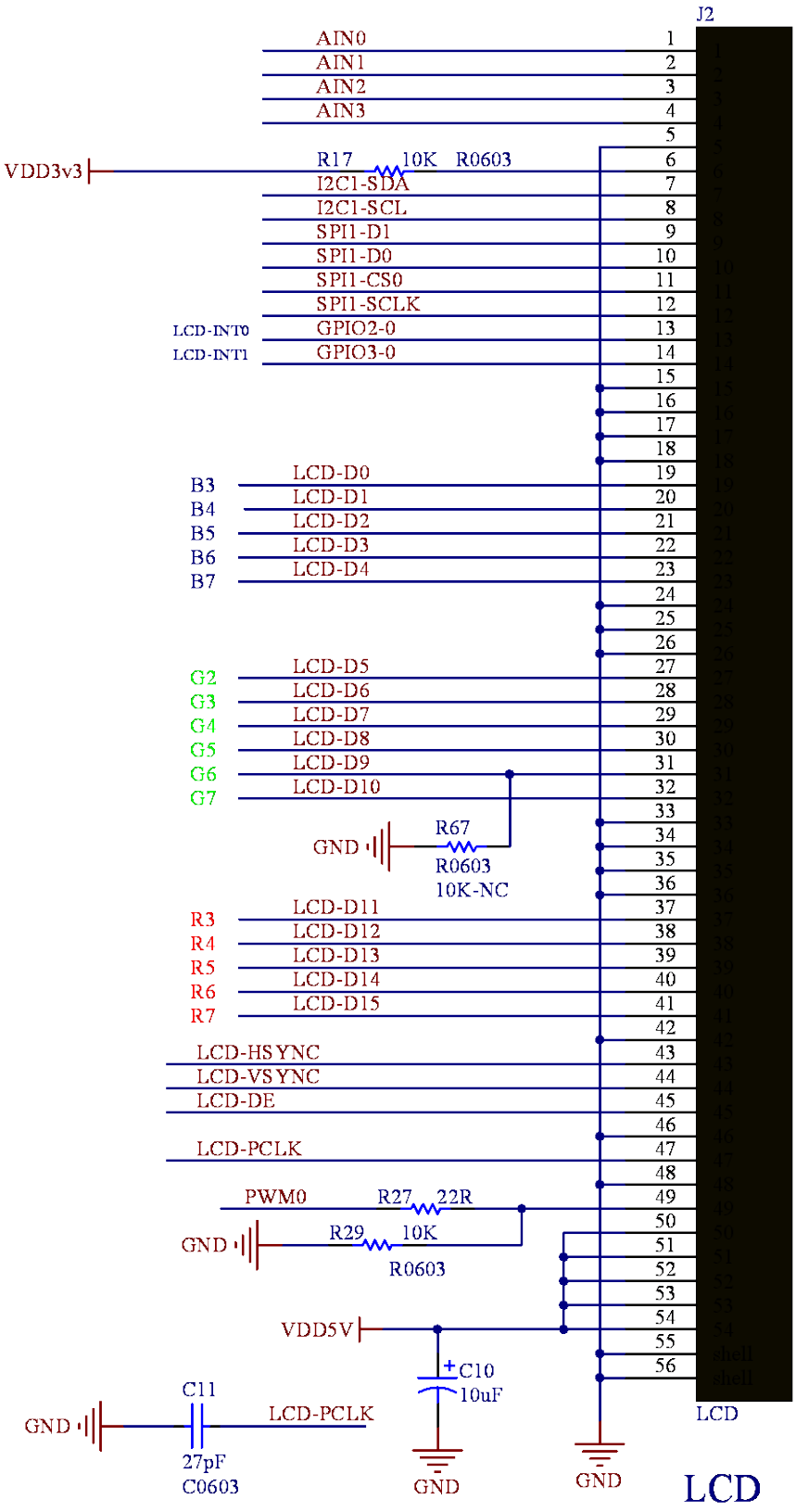

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Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	AIN0	Rscreen_XLeft	Resistive LCD X+	ANALOG
2	AIN1	Rscreen_XRight	Resistive LCD X-	ANALOG
3	AIN2	Rscreen_YUp	Resistive LCD Y+	ANALOG
4	AIN3	Rscreen_YDown	Resistive LCD Y-	ANALOG
5	GND	GND	Ground	GND
6	VDD3V3	NC	Power supply	(3.3V)
7	I2C1_SDA	SPI0_D1	I2C clock	LVCMOS(3.3V)
8	I2C1_SCL	SPI0_CS0	I2C data	LVCMOS(3.3V)
9	SPI1_D1	MCASP0_AXR0	SPI master input slave output	LVCMOS(3.3V)
10	SPI1_D0	MCASP0_FSX	SPI master output slave input	LVCMOS(3.3V)
11	SPI1_CS0	MCASP0_AHCLKR	SPI chip select	LVCMOS(3.3V)
12	SPI1_SCLK	MCASP0_ACLKX	SPI clock	LVCMOS(3.3V)
13	GPIO0_19	EVENT_INT0	EINT1	LVCMOS(3.3V)
14	GPIO0_20	EVENT_INT1	EINT2	LVCMOS(3.3V)
15	GND	GND	Ground	GND
16	GND	GND	Ground	GND
17	GND	GND	Ground	GND
18	GND	GND	Ground	GND
19	B3	LCD_D0	RGB blue data3	LVCMOS(3.3V)
20	B4	LCD_D1	RGB blue data4	LVCMOS(3.3V)
21	B5	LCD_D2	RGB blue data5	LVCMOS(3.3V)
22	B6	LCD_D3	RGB blue data6	LVCMOS(3.3V)
23	B7	LCD_D4	RGB blue data7	LVCMOS(3.3V)
24	GND	GND	GND	GND
25	GND	GND	GND	GND
26	GND	GND	GND	GND
27	G2	LCD_D5	RGB green data2	LVCMOS(3.3V)
28	G3	LCD_D6	RGB green data3	LVCMOS(3.3V)
29	G4	LCD_D7	RGB green data4	LVCMOS(3.3V)
30	G5	LCD_D8	RGB green data5	LVCMOS(3.3V)
31	G6	LCD_D9	RGB green data6	LVCMOS(3.3V)
32	G7	LCD_D10	RGB green data7	LVCMOS(3.3V)
33	GND	GND	Ground	GND
34	GND	GND	Ground	GND
35	GND	GND	Ground	GND
36	GND	GND	Ground	GND
37	R3	LCD_D11	RGB red data3	LVCMOS(3.3V)
38	R4	LCD_D12	RGB red data4	LVCMOS(3.3V)
39	R5	LCD_D13	RGB red data5	LVCMOS(3.3V)

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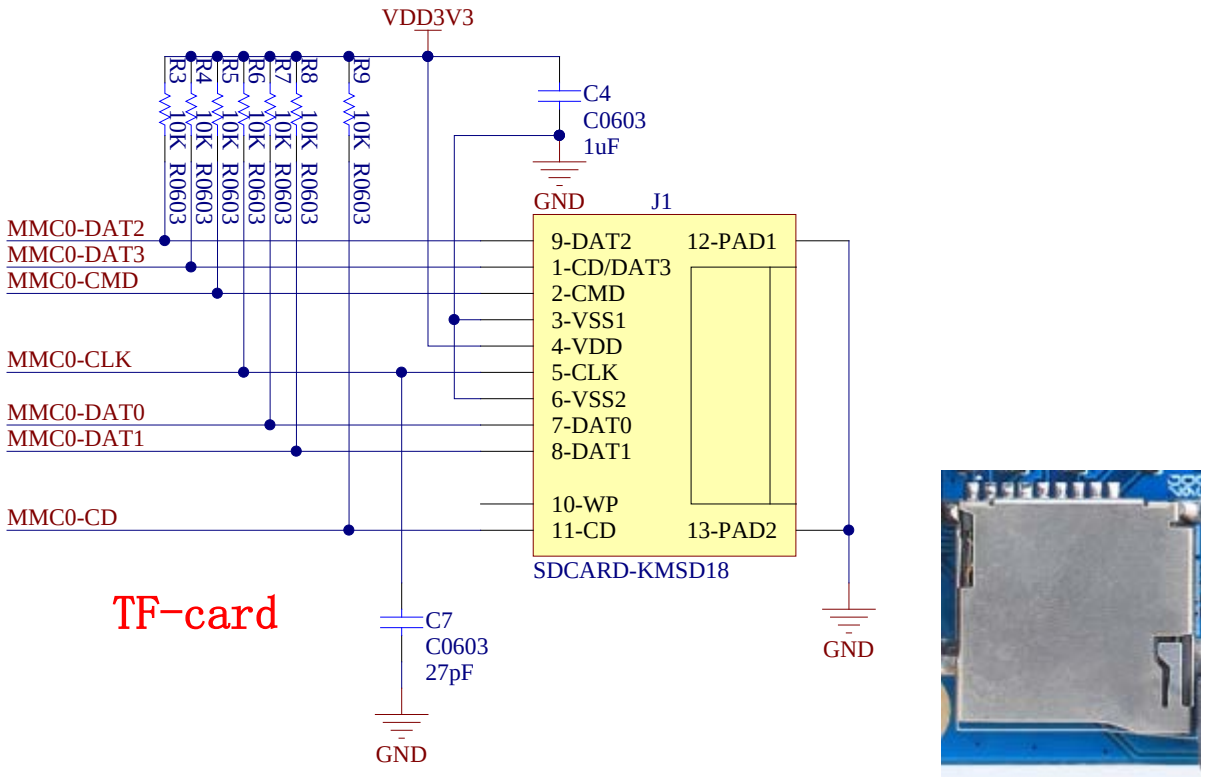
40	R6	LCD_D14	RGB red data6	LVCMOS(3.3V)
41	R7	LCD_D15	RGB red data7	LVCMOS(3.3V)
42	GND	GND	Ground	GND
43	LCD_HSYNC	LCD_HSYNC	RGB horizontal scan	LVCMOS(3.3V)
44	LCD_VSYNC	LCD_VSYNC	RGB vertical scan	LVCMOS(3.3V)
45	LCD_AC_BIAS_EN	LCD_AC_BIAS_EN	RGB data enable	LVCMOS(3.3V)
46	GND	GND	Ground	GND
47	LCD_PCLK	LCD_PCLK	RGB pixel clock	LVCMOS(3.3V)
48	GND	GND	Ground	GND
49	ECPA0_IN_PWM0_OUT	LCD_ENBKL	PWM backlight adjust,connect to PWM0,PIN58	LVCMOS(3.3V)
50	VDD5V	DC5V	5VDC Power supply	POWER
51	VDD5V	DC5V	5VDC Power supply	POWER
52	VDD5V	DC5V	5VDC Power supply	POWER
53	VDD5V	DC5V	5VDC Power supply	POWER
54	VDD5V	DC5V	5VDC Power supply	POWER
55	LCD position frame1	NC	Ground	GND
56	LCD position frame2	NC	Ground	GND

3.2.5 TF Card Slot



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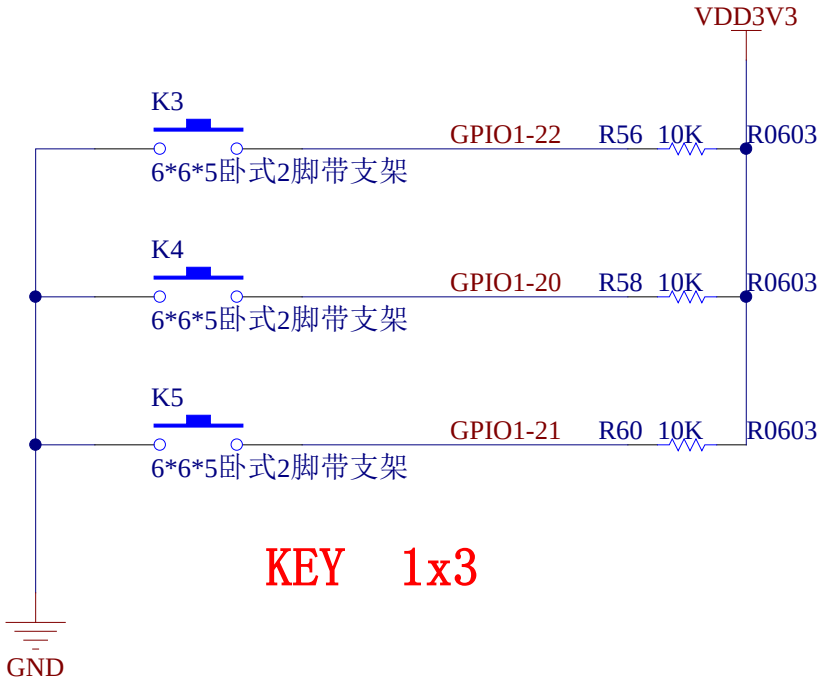
J1 represents TF card with 11 pins. This interface is connected to AM335x MMC0.

Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	MMC0-DAT3	MMC0_DAT3（Pin37）	Bi-directional dada bit3	LVCMOS(3.3V)
2	MMC0-CMD	MMC0_CMD（Pin38）	Bi-directional Command/Respond signal	LVCMOS(3.3V)
3	GND	GND	Ground	GND
4	VDD3V3	VDD3.3V	Power supply	POWER
5	MMC0-CLK	MMC0_CLK（Pin39）	Clock signal from Host machine to SD card	LVCMOS(3.3V)
6	GND	GND	Ground	GND
7	MMC0-DAT0	MMC0_DAT0（Pin40）	Bi-directional dada bit0	LVCMOS(3.3V)
8	MMC0-DAT1	MMC0_DAT1（Pin41）	Bi-directional dada bit1	LVCMOS(3.3V)
9	MMC0-DAT2	MMC0_DAT2（Pin36）	Bi-directional dada bit2	LVCMOS(3.3V)
10	MMC0_wp	GPMC_CSn3	write protect from SD card slot to host machine	LVCMOS(3.3V)
11	MMC0-CD	CD/EMU4（Pin42）	SD chip select enable，available in low level status	LVCMOS(3.3V)

3.2.6 On-board User Keys



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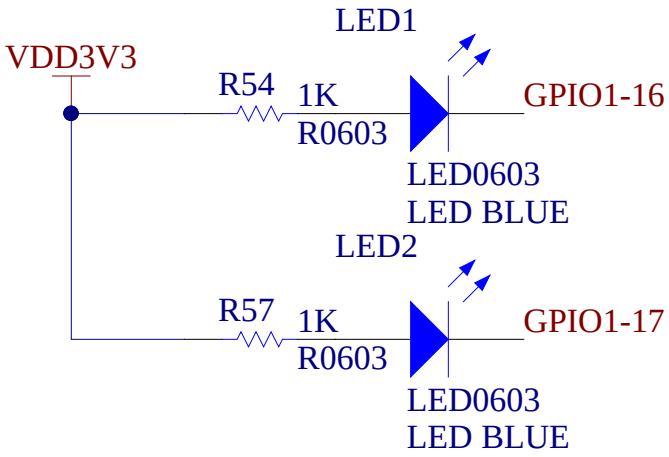
OK335xS-II provides 3 user keys (K3, K4, and K5) on board for users to develop their applications. These keys are OK335xS-II has 3 user keys, respectively marked as K3, K4, and K5 on the board. These keys are connected with AM335x external interrupt pins.

Key No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	K3	GPIO1-22	AM335x GPIO1-22	LVCMOS(3.3V)
2	K4	GPIO1-20	AM335x GPIO1-20	LVCMOS(3.3V)
3	K5	GPIO1-21	AM335x GPIO1-21	LVCMOS(3.3V)

3.2.7 LED Display

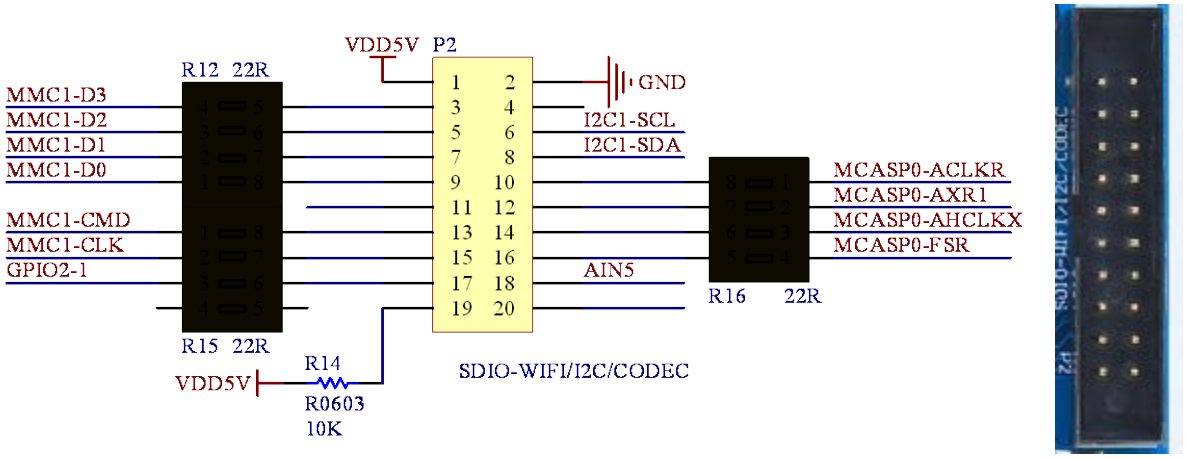


OK335xS-II has two LEDs (LED1, LED2), respectively are connected to AM335x GPIO1_16, GPIO1_17.Please configured these pins as GPIOs before using LED lights.

LED No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	LED1 GPIO1-16	RGMII2_TCTL（Pin）	AM335x的 GPIO1-16	LVCMOS(3.3V)
2	LED2 GPIO1-17	RGMII2_RCTL（Pin）	AM335x的 GPIO1-17	LVCMOS(3.3V)

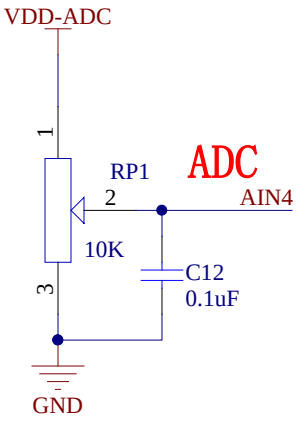
3.2.8 ADC

As OK335Xs-II is designed smart enough, so that many pins are multiplexed on board.
ADC and SPI share 10×2 pin 2.0mm pitch connector.



LED No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
2	GND	GND	GND	GND
1	VDD5V	VDD5V	Power supply	POWER
20,4	NC	NC	NC	NC
18	AIN5	AIN5（Pin77）	AM335x ADC analog input5	0 - 1.8V

Note: Please let all pins are not connected only when ADC function is running. There is 1-ch on-board adjustable ADC which is corresponded to AIN4 on CPU module.



3.2.9 Audio

OK335xS-II single board computer provides 1-ch I2S to expand external audio CODEC, which is multiplexed with SDIO-WIFI and I2C function. We only introduce you CODEC here, other functions could be found in SDIO-WIFI and I2C section.

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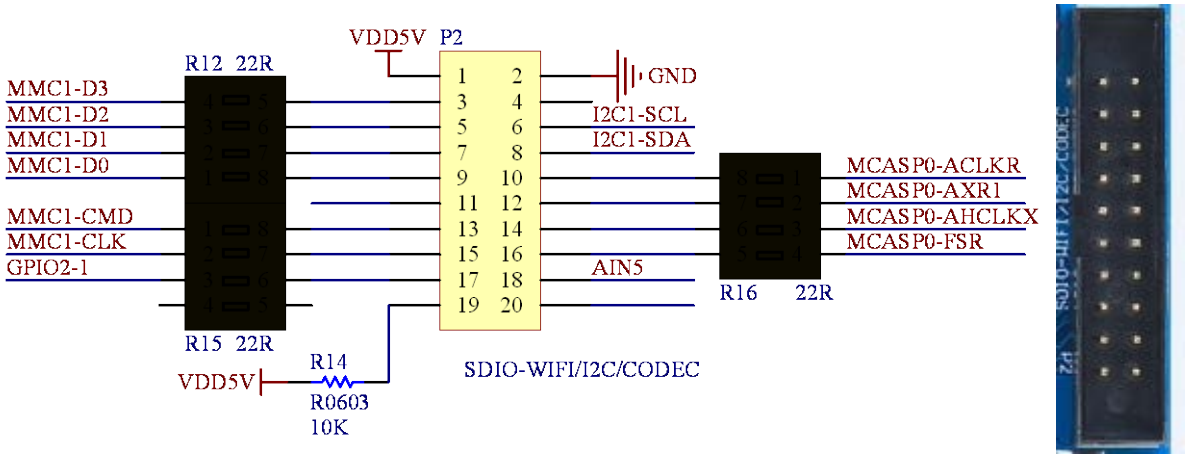
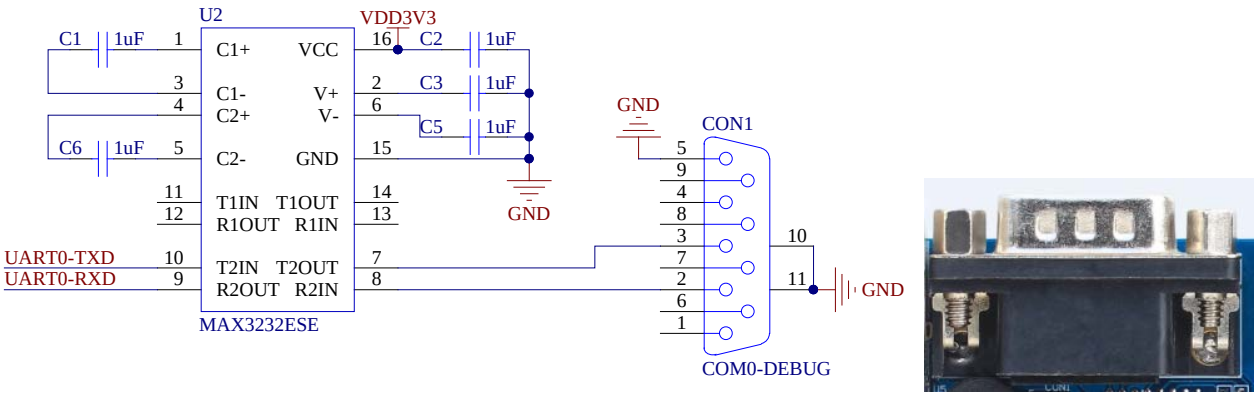


Pin No.	Codec Pin Name	Corresponding Pins On CPU Module	Description	Type
1	VDD5V	VDD5V	Power supply	POWER
2	GND	GND	GND	GND
14	MCASP0-ACLKR	MCASP0_ACLKR（Pin86）	MCASPO receive bit clock	LVCMOS(3.3V)
16	MCASP0-AXR1	MCASP0_AXR1（Pin84）	MCASPO Serial data	LVCMOS(3.3V)
18	MCASP0-AHCLKX	MCASP0_AHCLKX（Pin80）	MCASPO transmit master clock	LVCMOS(3.3V)
20	MCASP0-FSR	MCASP0_FSR（Pin79）	MCASPO receive frame sync.	LVCMOS(3.3V)

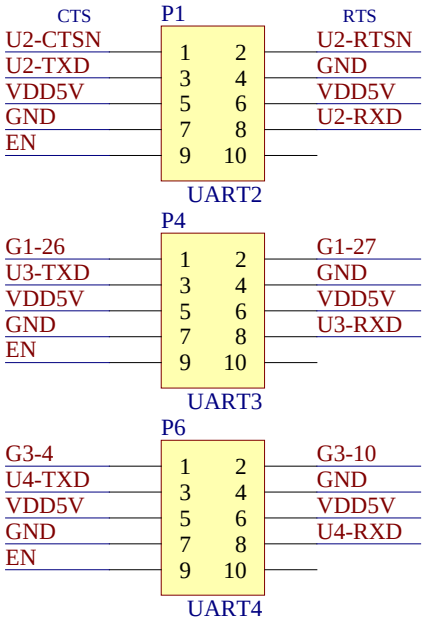
Note: Please let all other pins are not connected when using CODEC function.

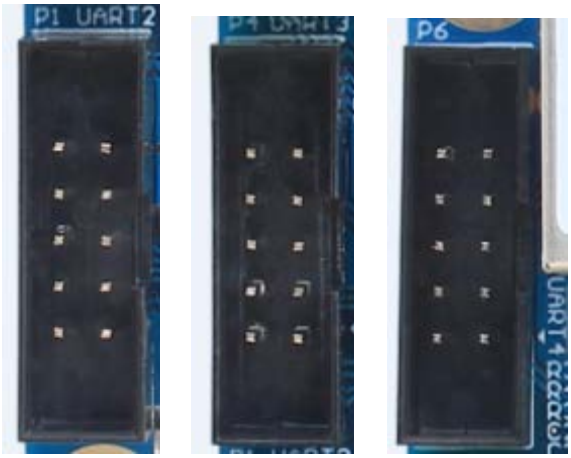
3.2.10 UART

OK335xS-II provides with 1-ch UART (CON1:COM0-DEBUG: UATR0).This interface is designed as DB9 connector with MAX232ESE level conversion chip.



For easy connection, OK335xS-II has 1-ch RS232 level UART and 3-ch 3.3V TTL level UART, respectively correspond to AM335x's UART1, UART2, UART3, and UART4.





UART2 Pin Definition:

Pin No.	Codec Pin Name	Corresponding Pins On CPU Module	Description	Type
1	UART2-CTSN	25	Clear to send	LVCMOS(3.3V)
2	UART2-RTSN	32	Request to transmit	LVCMOS(3.3V)
3	UART2-TXD	65	UART2 transmit data	LVCMOS(3.3V)
4	GND	NC	Ground	GND
5	VDD5V	NC	Power supply	POWER
6	VDD5V	NC	Power supply	POWER
7	GND	NC	Ground	GND
8	UART2-RXD	66	UART2 receive data	LVCMOS(3.3V)
9	EN	NC	External circuit enable	NC
10	NC	NC	NC	NC

Note: UART2 Pin1, Pin 2 could be set as I2C0 or GPIO.

UART3 Pin Definition:

Pin No.	Codec Pin Name	Corresponding Pins On CPU Module	Description	Type
1	GPIO1-26	124	General purpose IO	LVCMOS(3.3V)
2	GPIO1-27	125	General purpose IO	LVCMOS(3.3V)
3	UART3-TXD	3	UART2 transmit data	LVCMOS(3.3V)
4	GND	NC	Ground	GND

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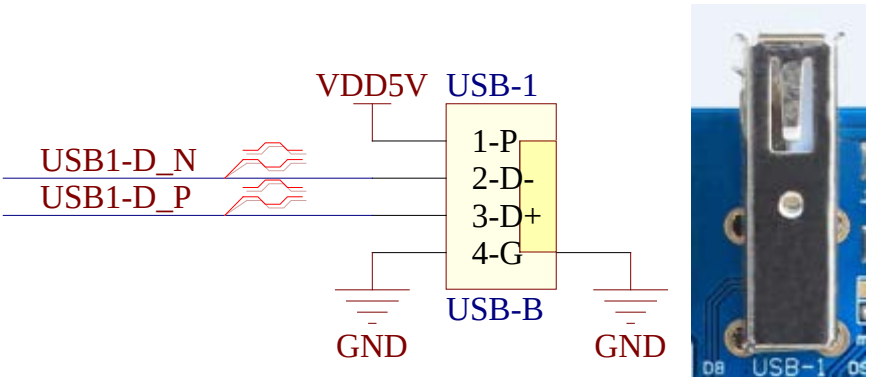
5	VDD5V	NC	Power supply	POWER
6	VDD5V	NC	Power supply	POWER
7	GND	NC	Ground	GND
8	UART3-RXD	2	UART2 receive data	LVCMOS(3.3V)
9	EN	NC	External circuit enable	NC
10	NC	NC	NC	NC

UART4 Pin definition：

Pin No.	Codec Pin Name	Corresponding Pins On CPU Module	Description	Type
1	GPIO3-4	6	General purpose IO	LVCMOS(3.3V)
2	GPIO3-10	10	General purpose IO	LVCMOS(3.3V)
3	UART4-TXD	5	UART2 transmit data	LVCMOS(3.3V)
4	GND	NC	Ground	GND
5	VDD5V	NC	Power supply	POWER
6	VDD5V	NC	Power supply	POWER
7	GND	NC	Ground	GND
8	UART4-RXD	4	UART2 receive data	LVCMOS(3.3V)
9	EN	NC	External circuit enable	NC
10	NC	NC	NC	NC

3.2.11 USB 2.0 HOST

OK335xS-II has a USB HOST interface which is derived to the USB-1 connector. Operators could use other external expansion device to expand to more USB interfaces.



3.2.12 Mini USB 2.0

J4 on the OK335xS-II represent USB2.0 OTG, adopts a standard Mini USB jack.

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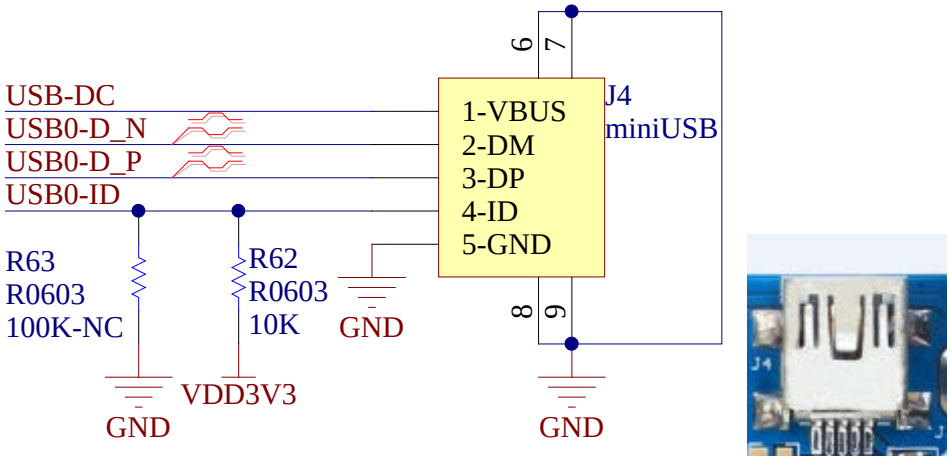
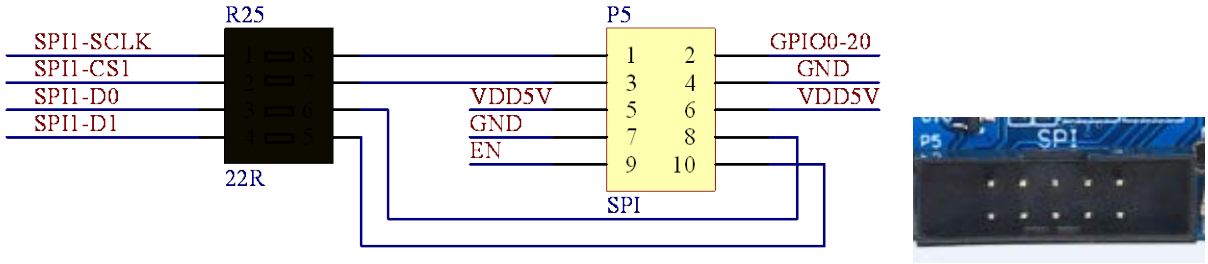


3.2.13 SPI Interface

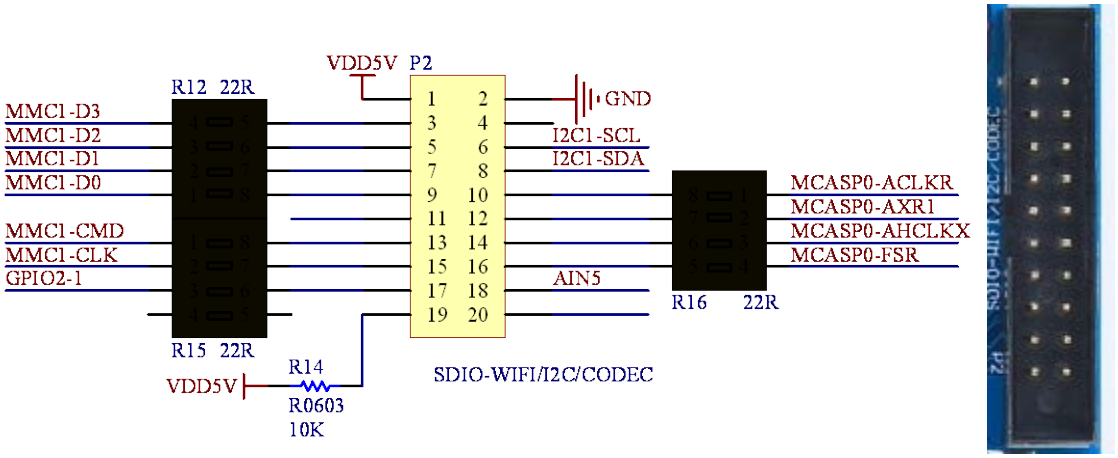
OK335xS-II is designed with 1-ch SPI.



Pin No.	Codec Pin Name	Corresponding Pins On CPU Module	Description	Type
1	SPI1-SCLK	81	SPI clock output	LVCMOS(3.3V)
2	GPIO0-20	49	SPI reserved interrupt	LVCMOS(3.3V)
3	SPI1-CS1	50	SPI chip select	LVCMOS(3.3V)
4	GND	NC	GND	GND
5	VDD5V	NC	DC5V power supply	POWER
6	VDD5V	NC	DC5V power supply	POWER
7	GND	NC	GND	GND
8	SPI1-D0	82	SPI data0	LVCMOS(3.3V)
9	EN	NC	External circuit enable	NC
10	SPI1-D1	85	SPI data1	LVCMOS(3.3V)

3.2.14 I2C

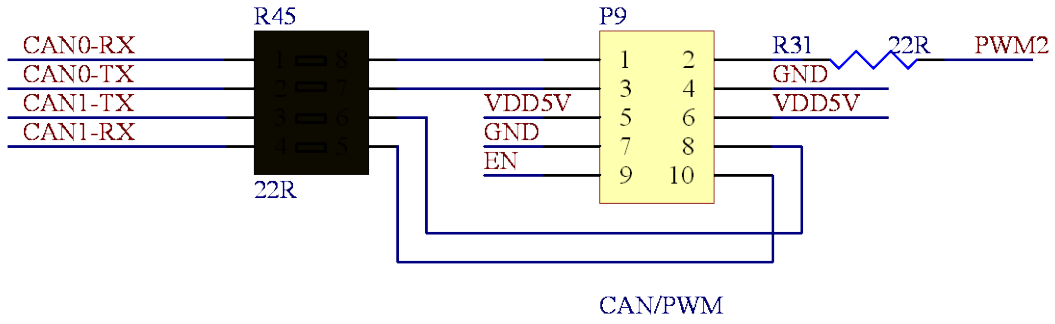
As OK335xS-II single board computer is small enough, so then some interfaces are multiplexed. I2C and SDIO-WIFI,CODEC are derived to one interface. If some pins are not needed, operators just need to leave them as NC. Here we only introduce relevant functions about I2C interface.



Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	VDD5V	DC5V	DC5V power supply	POWER
2	GND	GND	GND	GND
6	I2C1-SCL	I2C1_SCL	I2C serial clock output	LVCMOS(3.3V)
8	I2CSDA	I2C1_SDA	I2C serial data	LVCMOS(3.3V)

3.2.15 CAN

OK335xS-II has 2-ch CAN interface without transceiver, respectively are the AM335x CAN0, CAN1.CAN and PWM are multiplexed and shares one connector.



Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
5,6	VDD5V	VDD5V	DC5V power supply	POWER
1	CAN0-RX	CAN0_RX（Pin24）	CAN0receive data	LVCMOS(3.3V)
3	CAN0-TX	CAN0_TX（Pin23）	CAN0transmit data	LVCMOS(3.3V)
8	CAN1-TX	CAN1_TX（Pin22）	CAN1transmit data	LVCMOS(3.3V)
10	CAN1-RX	CAN1_RX（Pin21）	CAN1recieve data	LVCMOS(3.3V)

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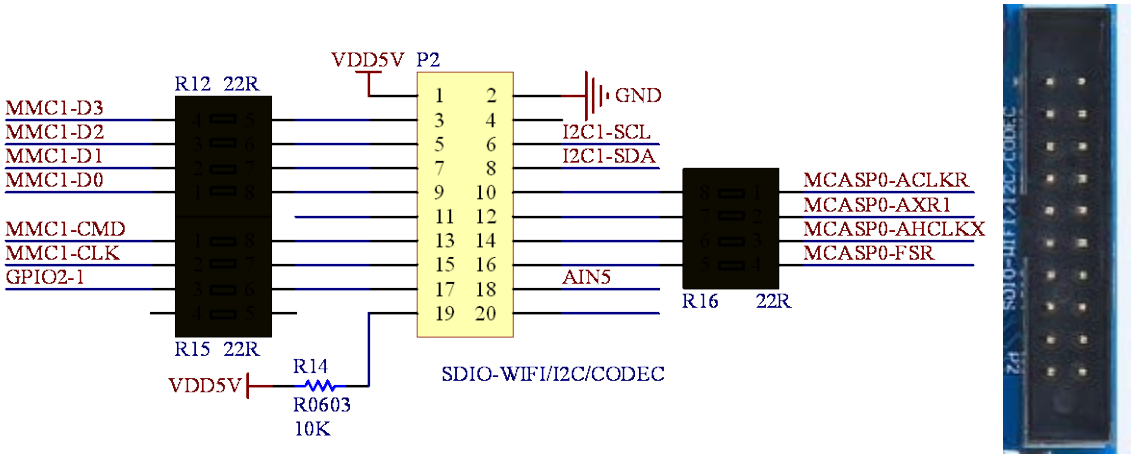
9	EN	NC	External Circuit Enable	NC
4,7	GND	GND	Ground	GND

3.2.16 SDIO WIFI



OK335xS-II single board computer derive s SD/MMC1 as 1-ch SDIO interface. It is designed to work with SDIO WIFI module manufactured by Forlinx. Operators could connect your SDIO modules based on pin definition and also could directly connect SD card, MMC card.I2C and CODEC also use could be derived from this connector.

Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	VDD5V	VDD5V	DC5V Power supply	POWER
2	GND	GND	GND	GND
3	MMC1-D3	LCD_B1（Pin111）	SDIO data3	LVCMOS(3.3V)
5	MMC1-D2	LCD_R0（Pin112）	SDIO data2	LVCMOS(3.3V)
7	MMC1-D1	LEC_G0（Pin113）	SDIO data1	LVCMOS(3.3V)
9	MMC1-D0	LCD_B0（Pin114）	SDIO data0	LVCMOS(3.3V)
13	MMC1-CMD	GPIO1_31（Pin35）	SDIO command	LVCMOS(3.3V)
15	MMC1-CLK	GPIO1_30（Pin56）	SDIO clock	LVCMOS(3.3V)
17	GPIO2-1	GPIO2_1（Pin57）	SDIO interrupt signal(reserved)	LVCMOS(3.3V)
19	EN	NC	SDIO enable（reserved）	5V(Higher voltage level)

3.2.17 100M Ethernet Interface

AM335x provides 2-ch gigabyte Ethernet interface, while OK335xS-II only derive 1×100M Ethernet with RMII interface on the Base board considering limit space, and use DP83848 to realize PHY connection.

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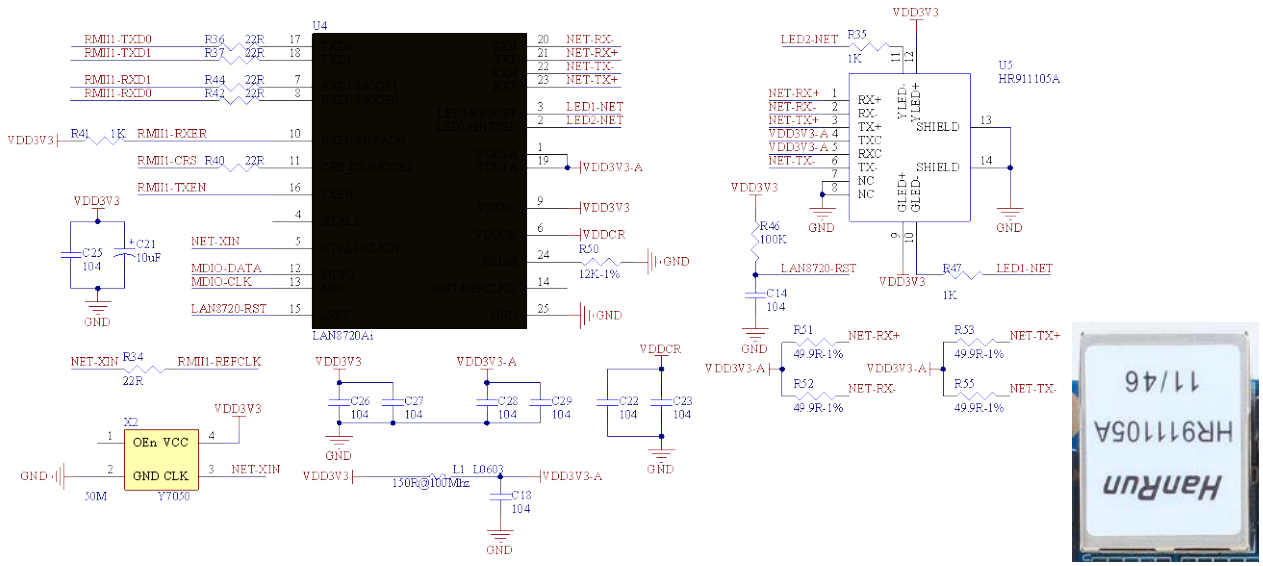
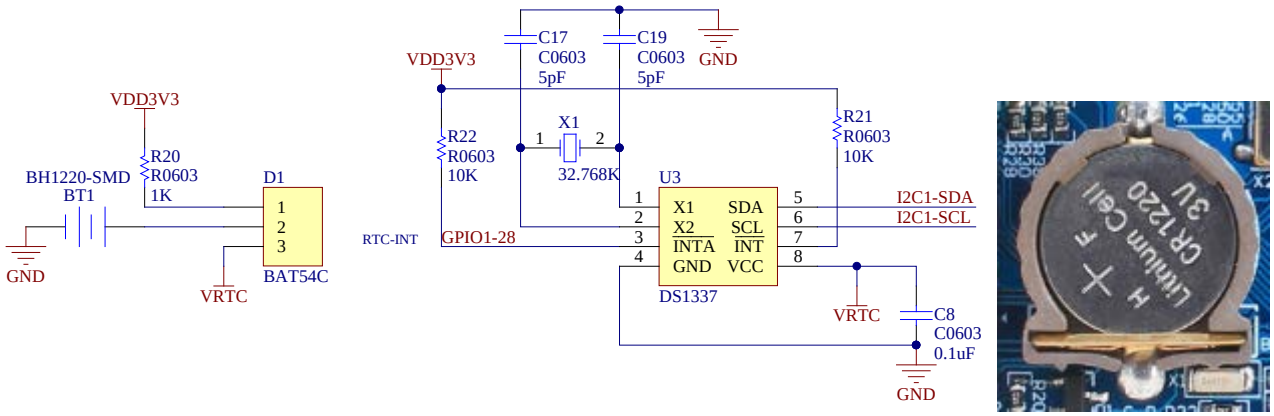


At present, new base board adopt LAN8720 chip to realize PHY connection, which will be simultaneously supported in Linux and WinCE OS.

For other more details please refer to OK335xS-II schematics.

3.2.18 On-board RTC

In order to make OK335xS-II more practical and make up the inadequacy of AM335x, OK335xS-II is designed with 1-ch RTC (DS1337).so then built-in AM335x RTC and DS1337 RTC will both are available.



3.2.19 PWM

OK335xS-II has 1-ch PWM interface (PWM2 on CPU module) to connect other external devices.
OK335xS-II is designed as a compact structure; PWM is multiplexed with CAN. We only introduce the PWM relevant pin functions here. Other details is recommended to check the CAN section in AM335X datasheet.

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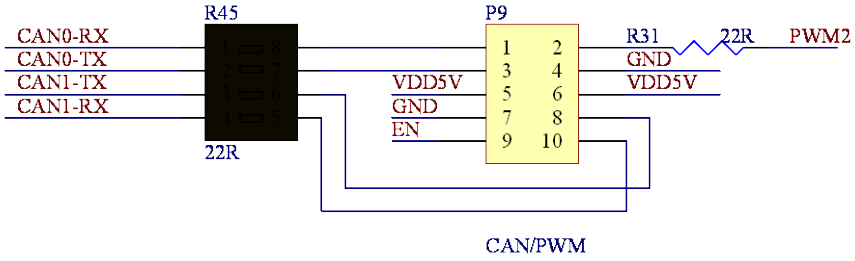
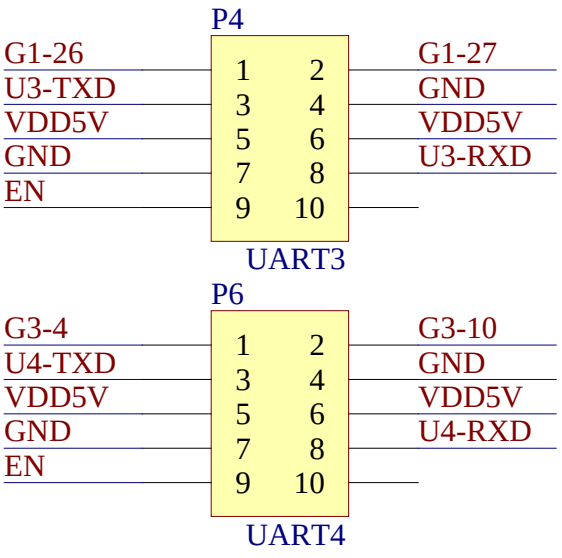


Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
1	VDD5V	VDD5V	DC5V power signal	POWER
2	PWM2	RGMII2_TXD2（Pin130）	PWM output	LVCMOS(3.3V)
6,8,10	GND	GND	GND	GND

3.2.20 GPIO

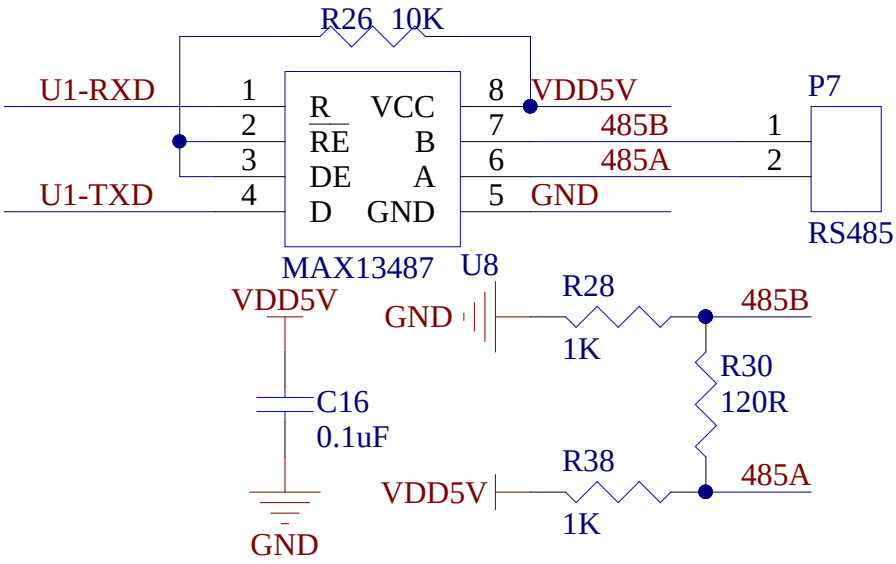
For easy controlling or connection with other devices, OK335xS-II single board computer provides 8-ch GPIO interfaces, could be connected with external LEDs, keys, electronic power switches, etc.

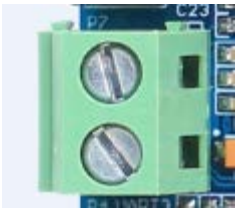


Pin No.	Signal Name	Corresponding Pins On CPU Module	Description	Type
P4-1	GPIO1-26	124	General purpose IO 1-26	LVCMOS(3.3V)
P4-2	GPIO1-27	125	General purpose IO 1-27	LVCMOS(3.3V)
P6-1	GPIO3-4	6	General purpose IO 3-4	LVCMOS(3.3V)
P6-2	GPIO3-10	10	General purpose IO 3-10	LVCMOS(3.3V)

3.2.21 RS485 Bus

OK335xS-II provides 1-ch isolated RS485 bus interface which is corresponded to UART1.MAX13487, is capable of transmitting and receiving data automatically, is used for PHY connection.





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