

# HEF4543B

## BCD to 7-segment latch/decoder/driver

Rev. 05 — 27 October 2009

Product data sheet

## 1. General description

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D0 to D3), an active LOW latch enable input ( $\overline{LE}$ ), an active HIGH blanking input (BL), an active HIGH phase input (PH) and seven buffered segment outputs (Qa to Qg).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BL) and latch enable ( $\overline{LE}$ ) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays, a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input. It is also suitable for use over the full industrial ( $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) temperature range.

## 2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Industrial

## 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4543BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4543BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

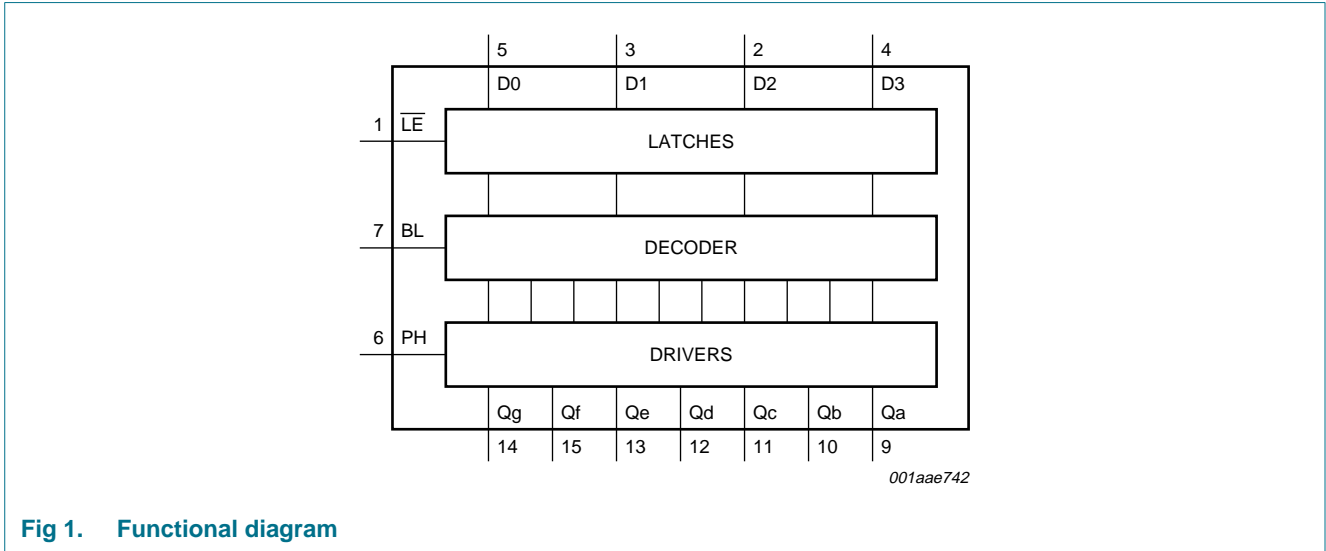
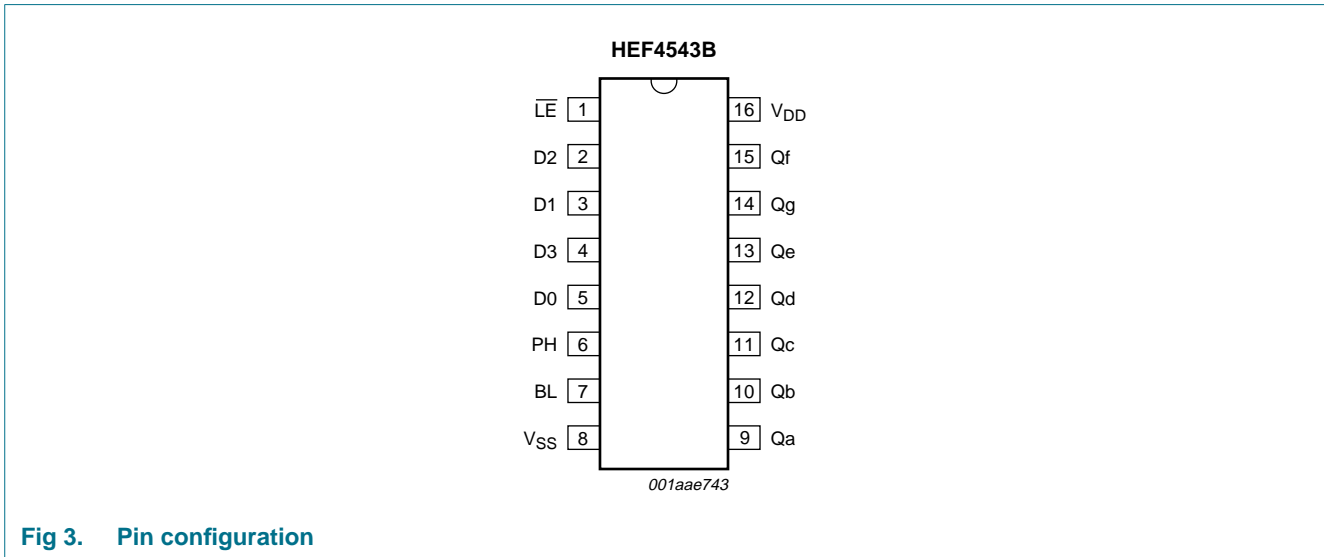


Fig 1. Functional diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

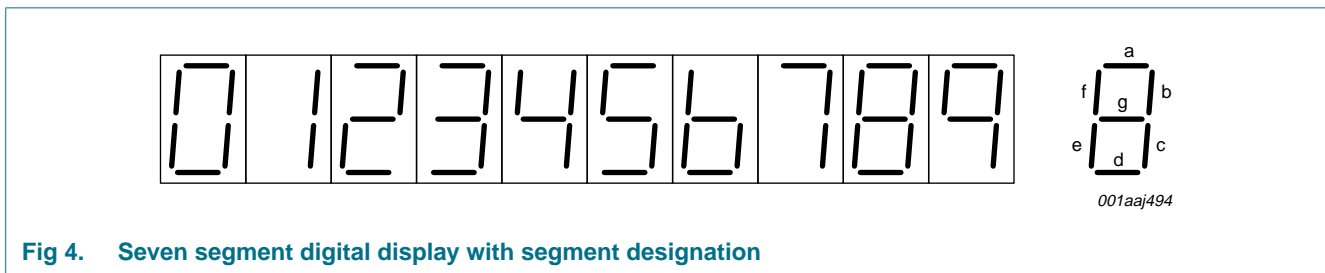
Symbol	Pin	Description
$\overline{LE}$	1	latch enable input (active LOW)
D0 to D3	5, 3, 2, 4	address (data) input
PH	6	phase input (active HIGH)
BL	7	blanking input (active HIGH)
$V_{SS}$	8	ground supply voltage
Qa to Qg	9, 10, 11, 12, 13, 15, 14	segment output
$V_{DD}$	16	supply voltage

## 7. Functional description

Table 3. Function table [1]

Inputs							Outputs							Display
$\overline{LE}$	BL	PH [2]	D3	D2	D1	D0	Qa	Qb	Qc	Qd	Qe	Qf	Qg	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	L	L	H	H	9
H	L	L	H	L	H	X	L	L	L	L	L	L	L	blank
H	L	L	H	H	X	X	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X	n.c.							n.c
as above		H	as above				inverse of above							as above

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care; n.c. = no change.
- [2] For liquid crystal displays, apply a square-wave to PH;  
 For common cathode LED displays, select PH = LOW;  
 For common anode LED displays, select PH = HIGH.



## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	DIP16 package	[1] -	750	mW
		SO16 package	[2] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage		3	-	15	V
V <sub>I</sub>	input voltage		0	-	V <sub>DD</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>DD</sub> = 5 V	-	-	3.75	μs/V
		V <sub>DD</sub> = 10 V	-	-	0.5	μs/V
		V <sub>DD</sub> = 15 V	-	-	0.08	μs/V

## 10. Static characteristics

**Table 6. Static characteristics**

V<sub>SS</sub> = 0 V; V<sub>I</sub> = V<sub>SS</sub> or V<sub>DD</sub> unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level output voltage		5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		V <sub>O</sub> = 4.6 V	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		V <sub>O</sub> = 9.5 V	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		V <sub>O</sub> = 13.5 V	15 V	-3.6	-	-3.0	-	-2.4	-	mA

**Table 6. Static characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; For test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	Dn to Qn; see <a href="#">Figure 5</a>	5 V	$153\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	180	360	ns
			10 V	$64\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	75	150	ns
			15 V	$47\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	55	110	ns
		$\overline{LE}$ to Qn; see <a href="#">Figure 5</a>	5 V	$143\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	170	340	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	80	160	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	60	120	ns
		BL to Qn; see <a href="#">Figure 5</a>	5 V	$118\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	145	290	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	65	130	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	45	90	ns
$t_{PLH}$	LOW to HIGH propagation delay	Dn to Qn; see <a href="#">Figure 5</a>	5 V	$153\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	180	360	ns
			10 V	$64\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	75	150	ns
			15 V	$47\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	55	110	ns
		$\overline{LE}$ to Qn; see <a href="#">Figure 5</a>	5 V	$163\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	190	380	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	80	160	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	60	120	ns
		BL to Qn; see <a href="#">Figure 5</a>	5 V	$98\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	125	250	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	40	80	ns
$t_t$	transition time	pin Qn; see <a href="#">Figure 5</a>	5 V	$10\text{ ns} + (1.00\text{ ns/pF}) C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF}) C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF}) C_L$	-	20	40	ns
$t_{su}$	set-up time	Dn to $\overline{LE}$ ; see <a href="#">Figure 6</a>	5 V		40	20	-	ns
			10 V		20	5	-	ns
			15 V		15	0	-	ns

**Table 7. Dynamic characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; For test circuit see [Figure 7](#); unless otherwise specified.

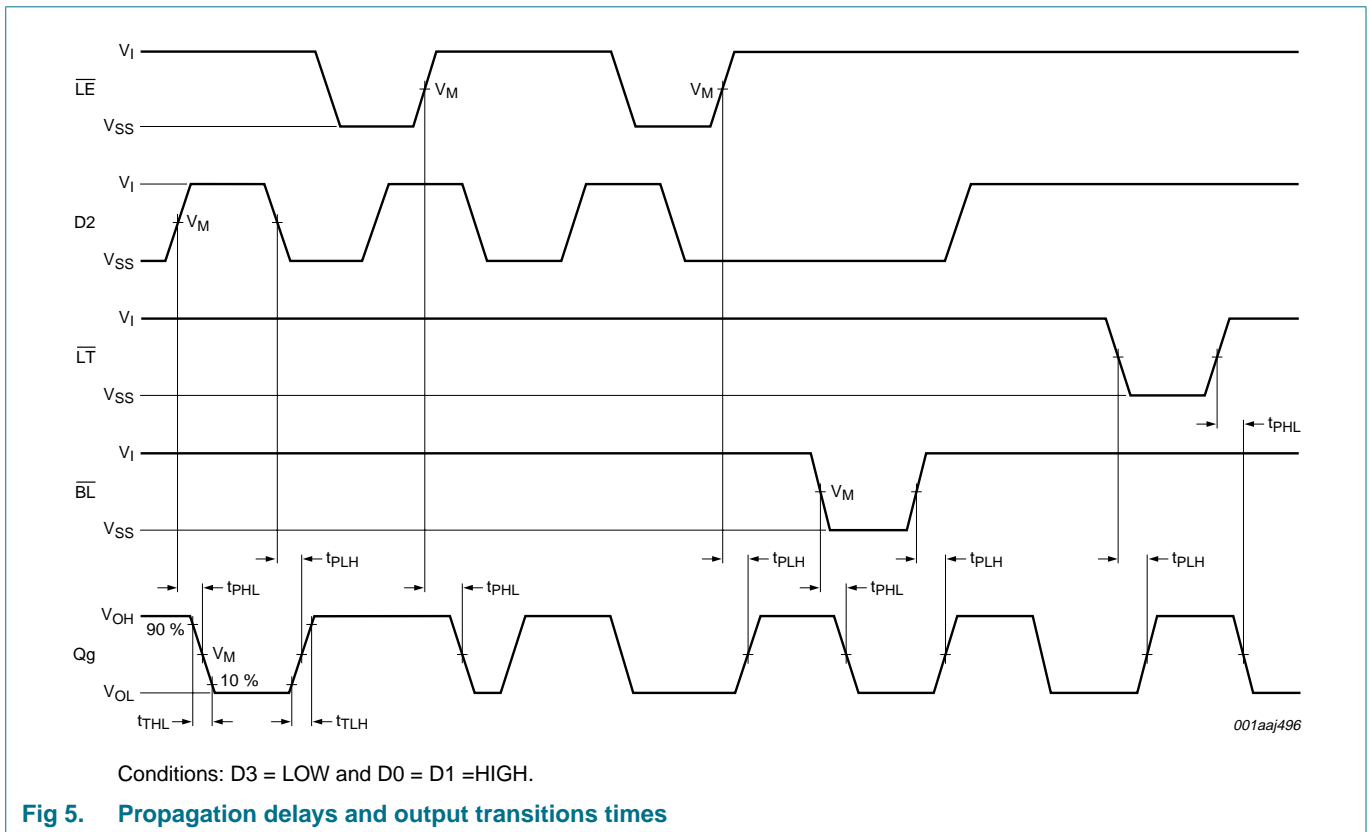
Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_h$	hold time	$D_n$ to $\overline{LE}$ ; see <a href="#">Figure 6</a>	5 V		0	-15	-	ns
			10 V		15	0	-	ns
			15 V		20	5	-	ns
$t_w$	pulse width	pin $\overline{LE}$ HIGH; minimum width; see <a href="#">Figure 6</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 8. Dynamic power dissipation  $P_D$**   
 $P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

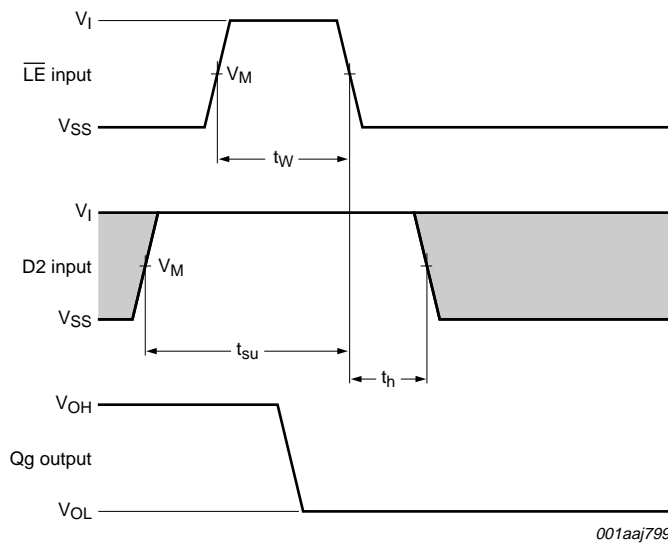
Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 2200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz,
		10 V	$P_D = 10400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz,
		15 V	$P_D = 33000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(C_L \times f_o)$ = sum of the outputs.

## 12. Waveforms



**Fig 5. Propagation delays and output transitions times**



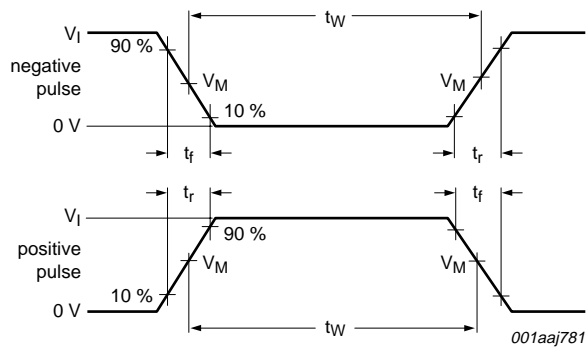


001aaj799

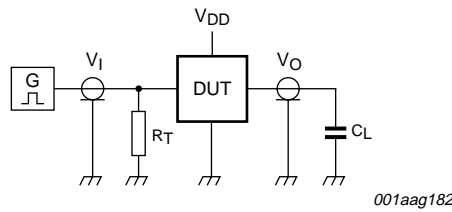
Conditions:

D3 = BL = LOW; D0 = D1 =  $\overline{LE}$  = HIGH

Fig 6. Waveforms showing minimum  $\overline{LE}$  pulse width, set-up, and hold time for DC to  $\overline{LE}$



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 7. Test circuit for switching times

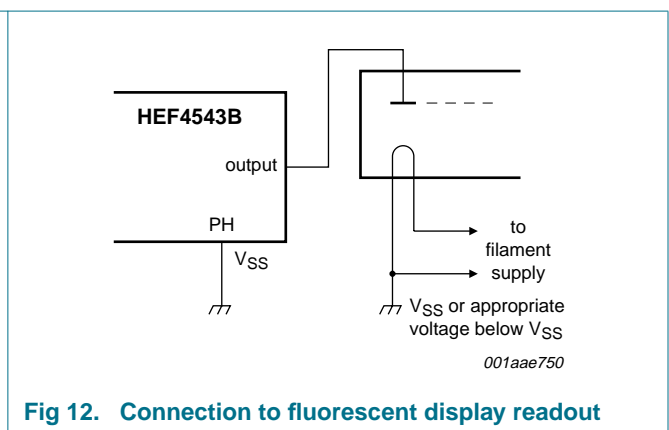
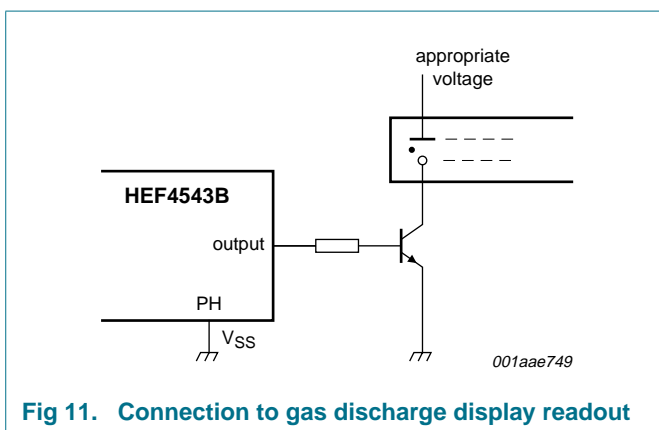
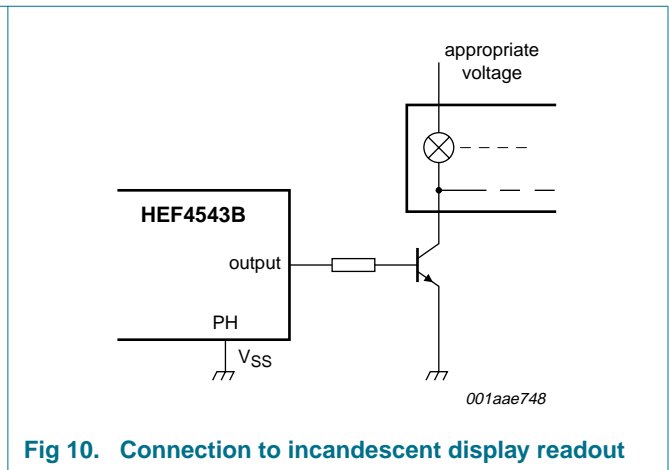
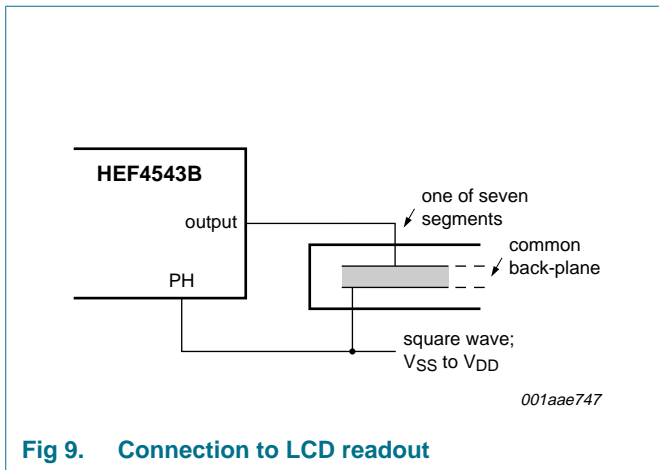
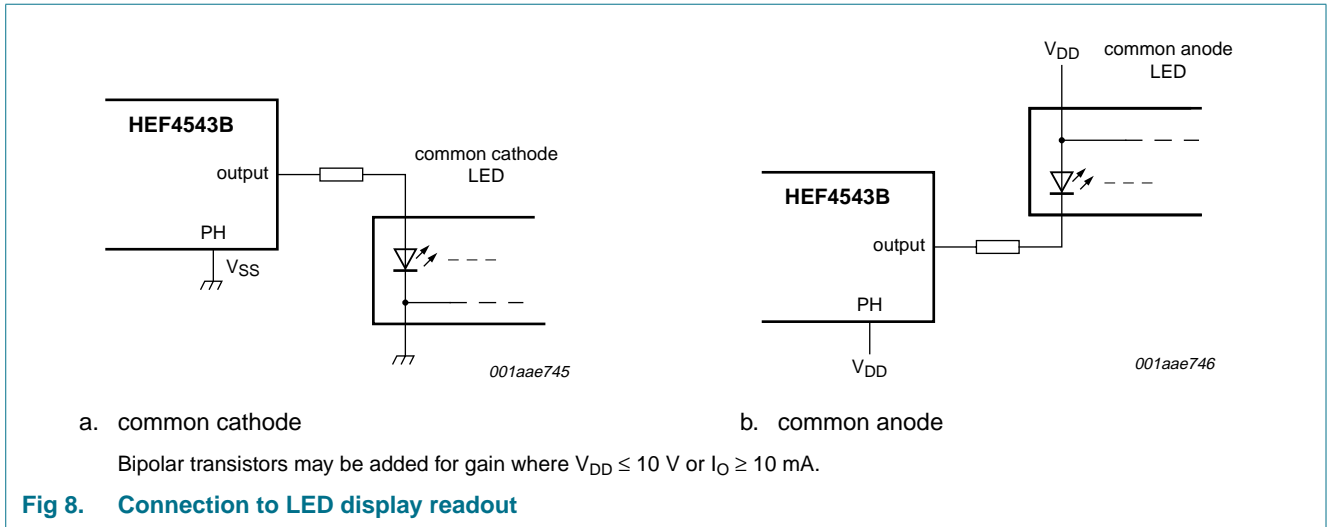
Table 9. Test data

Supply voltage	Input			Load
	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF

### 13. Application information

Some examples of applications for the HEF4543B are:

- Driving LCD displays
- Driving LED displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays



14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

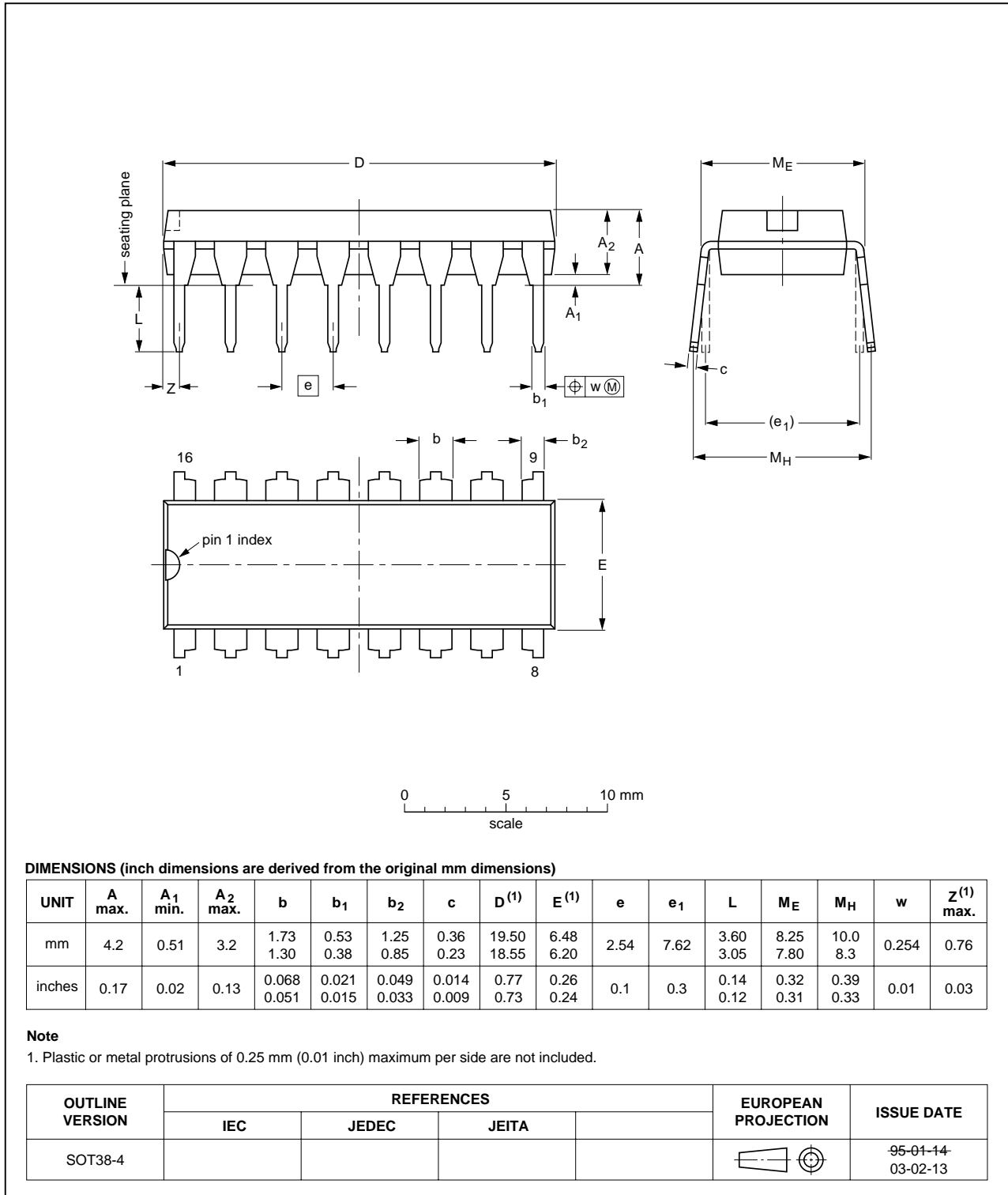


Fig 13. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

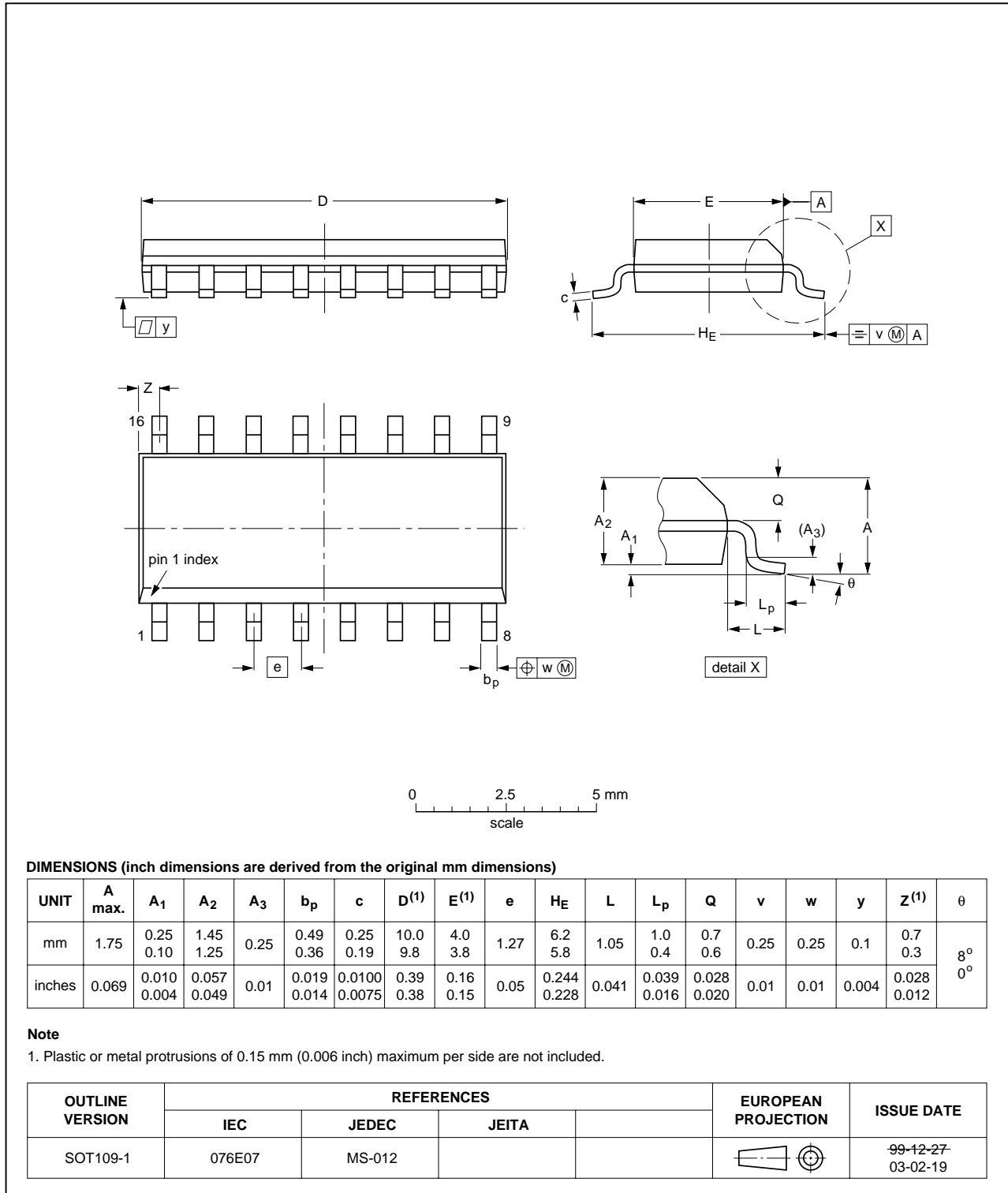


Fig 14. Package outline SOT109-1 (SO16)

## 15. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test

## 16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4543B_5	20091027	Product data sheet	-	HEF4543B_4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2 "Features"</a> ESD entry removed.</li> <li>• <a href="#">Section 9 "Recommended operating conditions"</a> <math>\Delta t/\Delta V</math> values updated.</li> <li>• <a href="#">Section 15 "Abbreviations"</a> ESD entries removed.</li> </ul>			
HEF4543B_4	20090317	Product data sheet	-	HEF4543B_CNV_3
HEF4543B_CNV_3	19950101	Product specification	-	HEF4543B_CNV_2
HEF4543B_CNV_2	19950101	Product specification	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 17.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 17.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

### 17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

**19. Contents**

1 **General description** . . . . . 1

2 **Features** . . . . . 1

3 **Applications** . . . . . 1

4 **Ordering information** . . . . . 1

5 **Functional diagram** . . . . . 2

6 **Pinning information** . . . . . 4

6.1 Pinning . . . . . 4

6.2 Pin description . . . . . 4

7 **Functional description** . . . . . 5

8 **Limiting values** . . . . . 5

9 **Recommended operating conditions** . . . . . 6

10 **Static characteristics** . . . . . 6

11 **Dynamic characteristics** . . . . . 7

12 **Waveforms** . . . . . 8

13 **Application information** . . . . . 10

14 **Package outline** . . . . . 12

15 **Abbreviations** . . . . . 14

16 **Revision history** . . . . . 14

17 **Legal information** . . . . . 15

17.1 Data sheet status . . . . . 15

17.2 Definitions . . . . . 15

17.3 Disclaimers . . . . . 15

17.4 Trademarks . . . . . 15

18 **Contact information** . . . . . 15

19 **Contents** . . . . . 16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 27 October 2009

Document identifier: HEF4543B\_5