OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC373P NON-INVERTING
TC74HC533P INVERTING
TC74HC563P INVERTING
TC74HC573P NON-INVERTING

The TC74HC373, TC74HC533, TC74HC563 and TC74HC573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The application designer has a choise of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

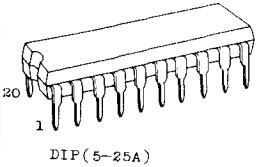
The TC74HC373 and the TC74HC573, the TC74HC533 and The TC74HC563 have the same function and the same characteristics respectively, but have the different pin layouts.

The three-state output configuration and the wide choise of outline will make the bus-organized system simple.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

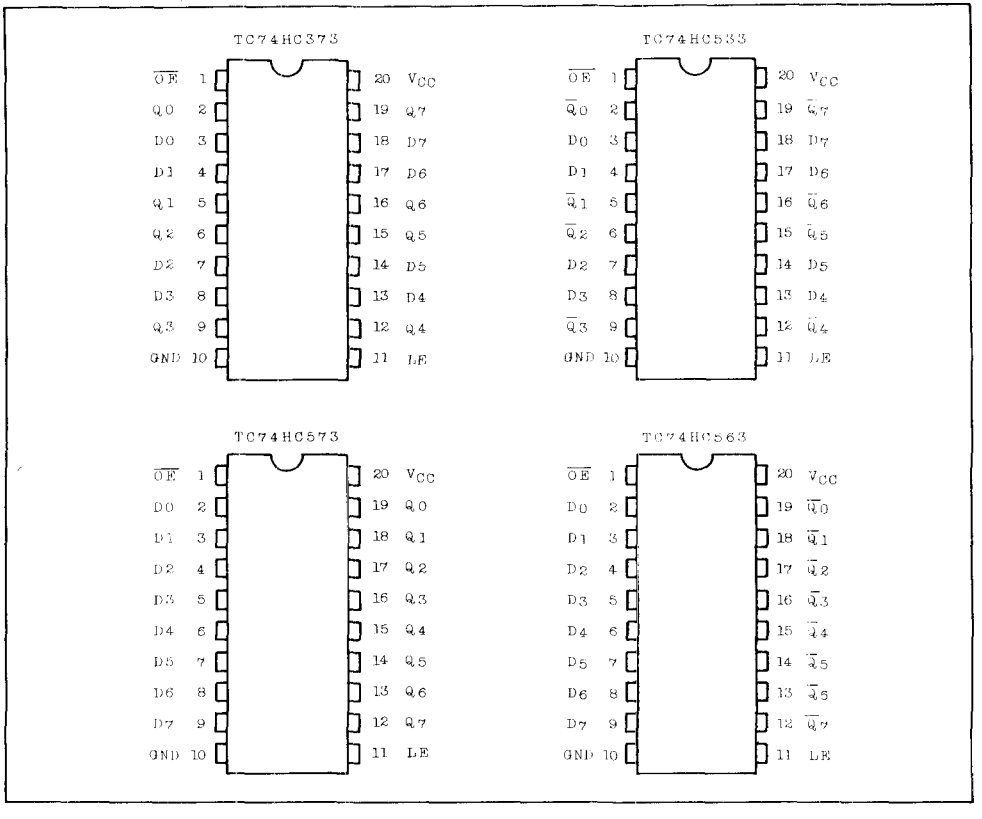
FEATURES:

- High Speed.....t_{pd}=15ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance...$|I_{OH}|$=I_{OL}=6mA
- Balanced Propagation Delays....t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range...$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS373/533/563/573



DIP(5-25A)

PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

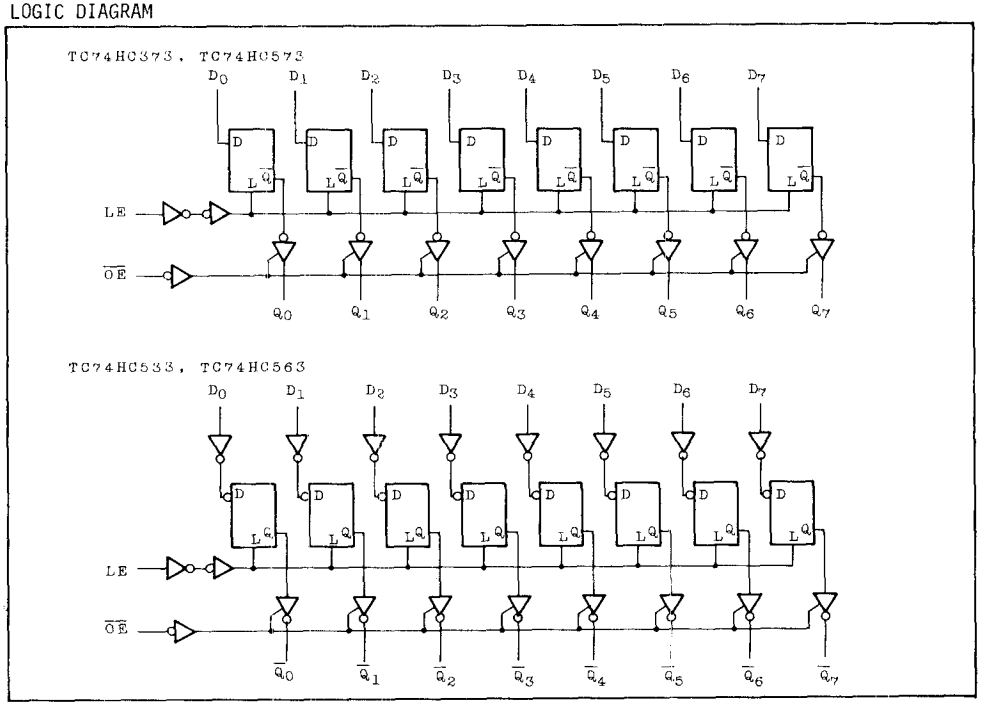
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373,HC573)	$\overline{Q}$ (HC533,HC563)
H	X	X	Z	Z
L	L	X	No change*	No change*
L	H	L	L	H
L	H	H	H	L

X : Don't care

Z : High impedance

* : Q/$\overline{Q}$ outputs are latched at the time when the LE input is taken low logic level.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

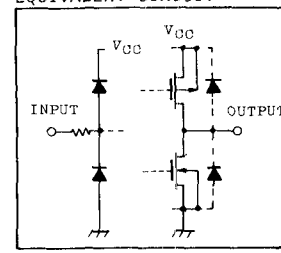
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V)	ns
		0 ~ 500 (V_{CC}=4.5V)	
		0 ~ 400 (V_{CC}=6.0V)	

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.32	-	0.37	
			I_{OL}=7.8mA	6.0	-	0.18	0.32	-	0.37	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

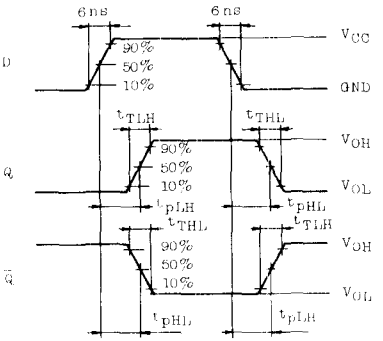
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	24	60	-	75	ns
			4.5	-	8	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (LE - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	82	175	-	210	
			4.5	-	22	35	-	42	
			6.0	-	19	30	-	36	
Propagation Delay Time (D - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	66	145	-	175	
			4.5	-	18	29	-	35	
			6.0	-	16	25	-	30	
Minimum Pulse Width (LE)	$t_{w(H)}$		2.0	-	30	75	-	90	
			4.5	-	8	15	-	18	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	75	-	90	
			4.5	-	2	15	-	18	
			6.0	-	2	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	50	-	60	
			4.5	-	-	10	-	12	
			6.0	-	-	9	-	11	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	62	145	-	175	
			4.5	-	18	29	-	35	
			6.0	-	16	25	-	30	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	50	175	-	210	
			4.5	-	22	35	-	42	
			6.0	-	20	30	-	36	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	41	-	-	-	

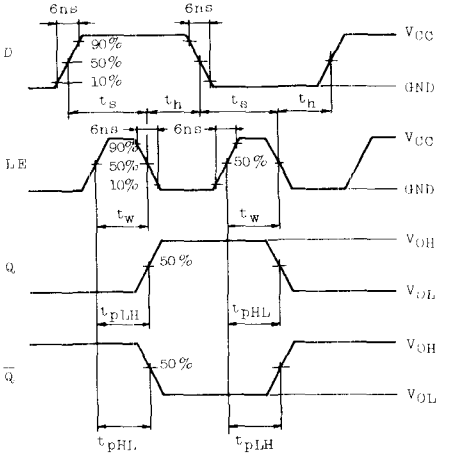
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/8$ (per Latch)

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL} (D - Q,$\overline{Q}$)



t_{pLH}, t_{pHL} (LE - Q,$\overline{Q}$), t_s, th, tw

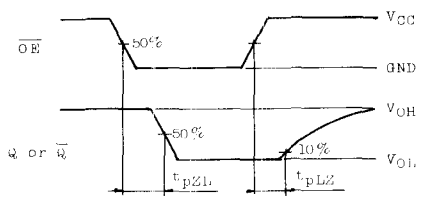


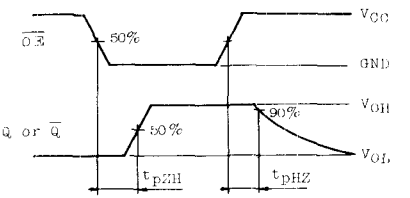
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

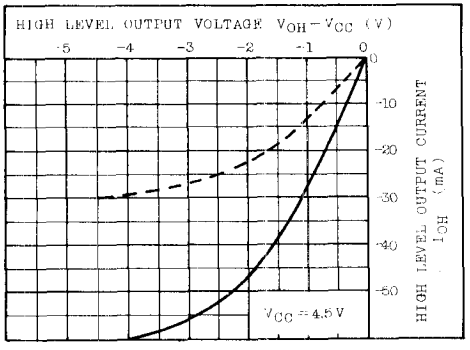
t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.

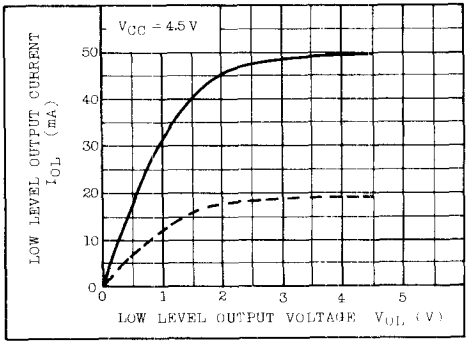




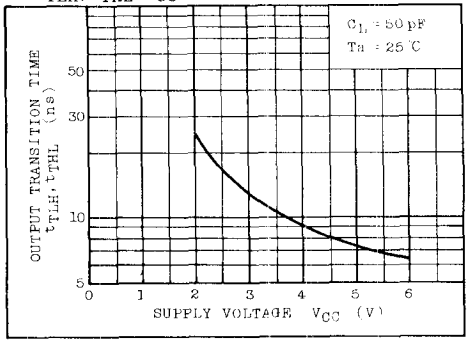
I_{OH} CHARACTERISTICS



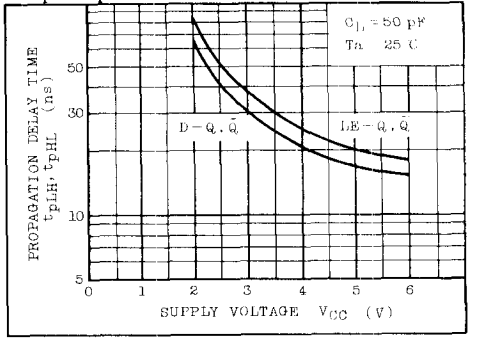
I_{OL} CHARACTERISTICS



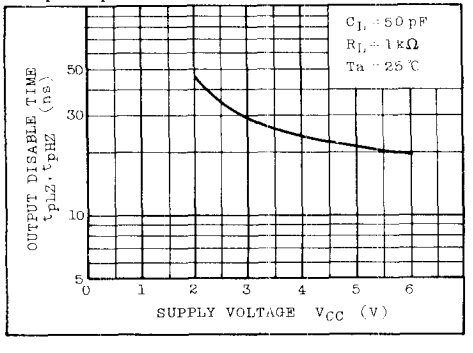
t_{TLH}, t_{THL}-V_{CC} CHARACTERISTICS (TYP.)



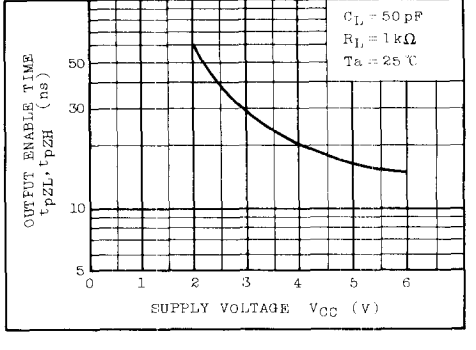
t_{pLH}, t_{pHL}-V_{CC} CHARACTERISTICS (TYP.)



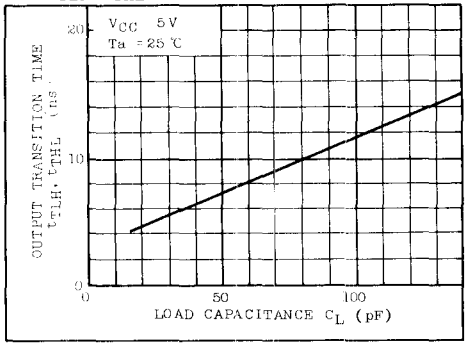
t_{pLZ}, t_{pHZ}-V_{CC} CHARACTERISTICS (TYP.)



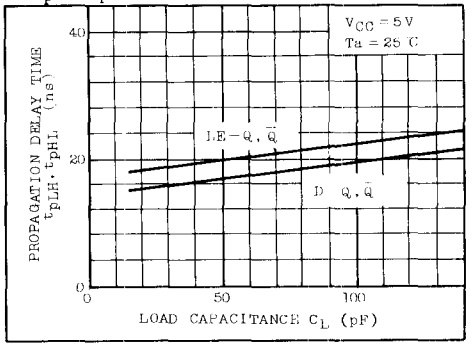
t_{pZL}, t_{pZH}-V_{CC} CHARACTERISTICS (TYP.)



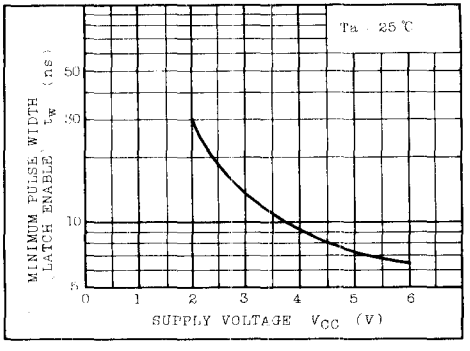
t_{TLH}, t_{THL}-C_L CHARACTERISTICS (TYP.)



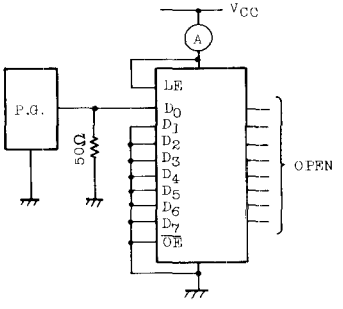
t_{pLH}, t_{pHL}-C_L CHARACTERISTICS (TYP.)



t_W(LE)-V_{CC} CHARACTERISTICS (TYP.)



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.