

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC7292AP, TC74HC7292AF

PROGRAMMABLE DIVIDER / TIMER

The TC74HC7292A is a high speed CMOS PROGRAMMABLE DIVIDER / TIMER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The TC74HC7292A can divide from 2² to 2³¹.

CK1 and CK2 are clock inputs, either one may be used for clock gating.

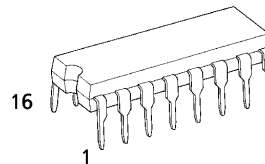
It features an active-low clear input to initialize the state of all flip-flops.

To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3)

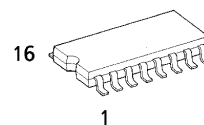
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{MAX} = 70\text{MHz}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS292

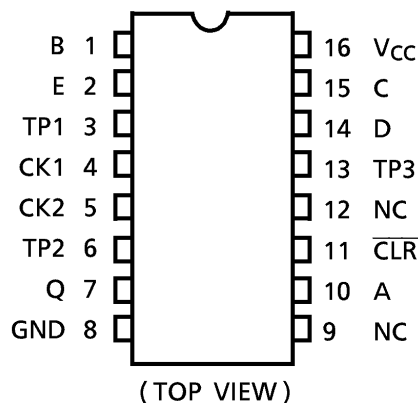


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

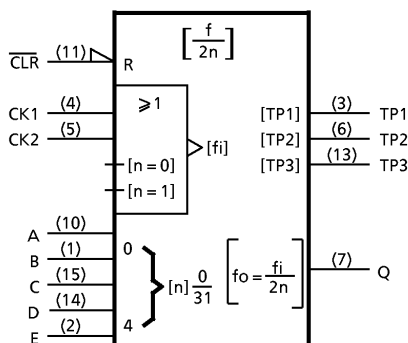


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



980508EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

TRUTH TABLE

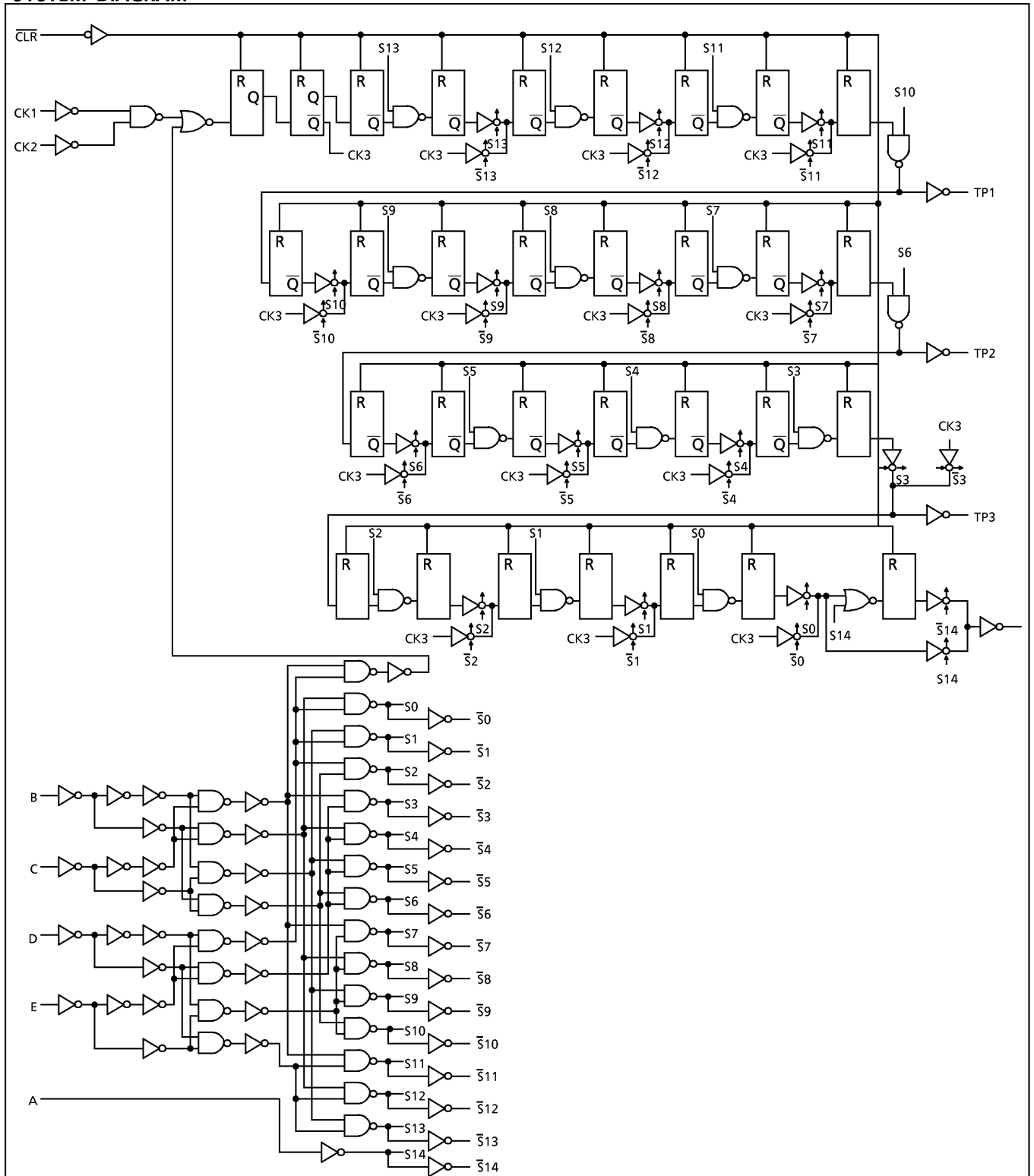
CLR	CK1	CK2	Q OUTPUT MODE
L	X	X	Cleared to L
H		L	UP Count
H	L		
H	H	X	NO Change
H	X	H	

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2 ²	4	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	L	H	H	2 ³	8	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	L	L	2 ⁴	16	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	L	H	2 ⁵	32	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	H	L	2 ⁶	64	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	H	H	2 ⁷	128	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	H	L	L	L	2 ⁸	256	2 ⁹	512	2 ¹⁷	131,072	2 ²	4
L	H	L	L	H	2 ⁹	512	2 ⁹	512	2 ¹⁷	131,072	2 ²	4
L	H	L	H	L	2 ¹⁰	1,024	2 ⁹	512	2 ¹⁷	131,072	2 ⁴	16
L	H	L	H	H	2 ¹¹	2,048	2 ⁹	512	2 ¹⁷	131,072	2 ⁴	16
L	H	H	L	L	2 ¹²	4,096	2 ⁹	512	2 ¹⁷	131,072	2 ⁶	64
L	H	H	L	H	2 ¹³	8,192	2 ⁹	512	2 ¹⁷	131,072	2 ⁶	64
L	H	H	H	L	2 ¹⁴	16,384	2 ⁹	512	Disabled Low		2 ⁸	256
L	H	H	H	H	2 ¹⁵	32,768	2 ⁹	512	Disabled Low		2 ⁸	256
H	L	L	L	L	2 ¹⁶	65,536	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H	L	L	L	H	2 ¹⁷	131,072	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H	L	L	H	L	2 ¹⁸	262,144	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H	L	L	H	H	2 ¹⁹	524,288	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H	L	H	L	L	2 ²⁰	1,048,576	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H	L	H	L	H	2 ²¹	2,097,152	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H	L	H	H	L	2 ²²	4,194,304	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H	L	H	H	H	2 ²³	8,388,608	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H	H	L	L	L	2 ²⁴	16,777,216	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H	H	L	L	H	2 ²⁵	33,554,432	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H	H	L	H	L	2 ²⁶	67,108,864	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H	H	L	H	H	2 ²⁷	134,217,728	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H	H	H	L	L	2 ²⁸	268,435,456	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H	H	H	L	H	2 ²⁹	536,870,912	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H	H	H	H	L	2 ³⁰	1,073,741,824	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
H	H	H	H	H	2 ³¹	2,147,483,648	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216

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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage (Q)	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
Low - Level Output Voltage (Q)	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	±0.1	—	±1.0	μA	
			6.0	—	—	4.0	—	40.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	μA	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time (CLR)	$t_{W(L)}$		2.0	—	175	220	
			4.5	—	35	44	
			6.0	—	30	37	
Minimum Removal Time	t_{rem}		2.0	—	5	5	
			4.5	—	5	5	
			6.0	—	5	5	
Clock Frequency	f		2.0	—	5	4	MHz
			4.5	—	27	22	
			6.0	—	32	26	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Q)	t_{TLH}		—	4	8	ns
	t_{THL}					
Output Transition Time (TP)	t_{TLH}		—	25	44	
	t_{THL}					
Propagation Delay Time (CK-Q)	t_{pLH}		—	42	75	
	t_{pHL}					
Propagation Delay Time ($\overline{\text{CLR}}$ -Q)	t_{pHL}		—	36	62	
Maximum Clock Frequency	f_{MAX}		30	70	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	—	27	75	—	95	ns
			4.5	—	9	15	—	19	
			6.0	—	8	13	—	16	
Output Transition Time (TP)	t_{TLH} t_{THL}		2.0	—	90	250	—	315	
			4.5	—	30	50	—	63	
			6.0	—	25	43	—	54	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		2.0	—	150	425	—	530	
			4.5	—	48	85	—	106	
			6.0	—	41	72	—	90	
Propagation Delay Time ($\overline{\text{CLR}}$ -Q)	t_{pHL}		2.0	—	130	350	—	440	
			4.5	—	42	70	—	88	
			6.0	—	36	60	—	75	
Maximum Clock Frequency	f_{MAX}		2.0	5	20	—	4	—	MHz
			4.5	27	64	—	22	—	
			6.0	32	75	—	26	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	Note (1)		—	22	—	—	—	

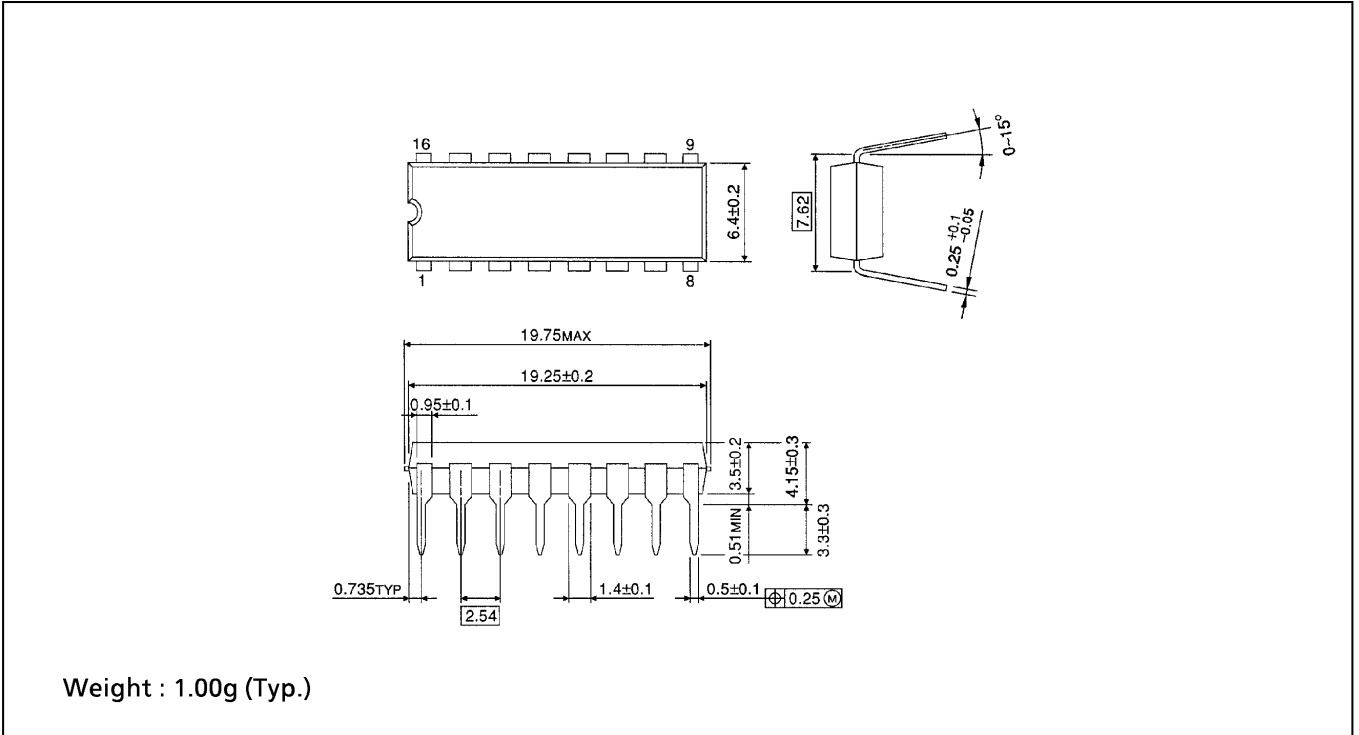
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

