

SN54HC107, SN74HC107
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH CLEAR

D2884, DECEMBER 1982 — REVISED JUNE 1989

T4607-07

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

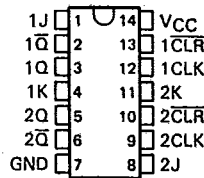
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the CLR input resets the outputs regardless of the levels of the other inputs. When CLR is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC107 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC107 is characterized for operation from -40°C to 85°C.

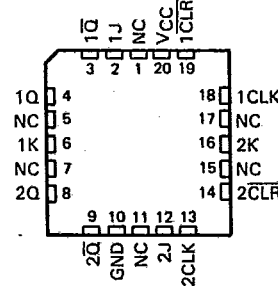
FUNCTION TABLE

| INPUTS | | | | OUTPUT | |
|--------|-----|---|---|----------------|-------------|
| CLR | CLK | J | K | Q | \bar{Q} |
| L | X | X | X | L | H |
| H | I | L | L | Q ₀ | \bar{Q}_0 |
| H | I | H | L | H | L |
| H | I | L | H | L | H |
| H | I | H | H | TOGGLE | TOGGLE |
| H | H | X | X | Q ₀ | \bar{Q}_0 |

SN54HC107 . . . J PACKAGE
 SN74HC107 . . . D OR N PACKAGE
 (TOP VIEW)



SN54HC107 . . . FK PACKAGE
 (TOP VIEW)

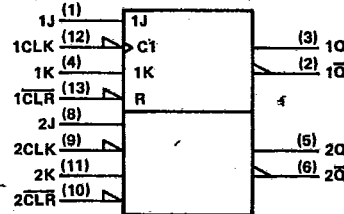


NC—No internal connection

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HC MOS Devices

logic symbols†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

NOTICE
 SEE ORDER OF DATA FOR ERRATA INFORMATION

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



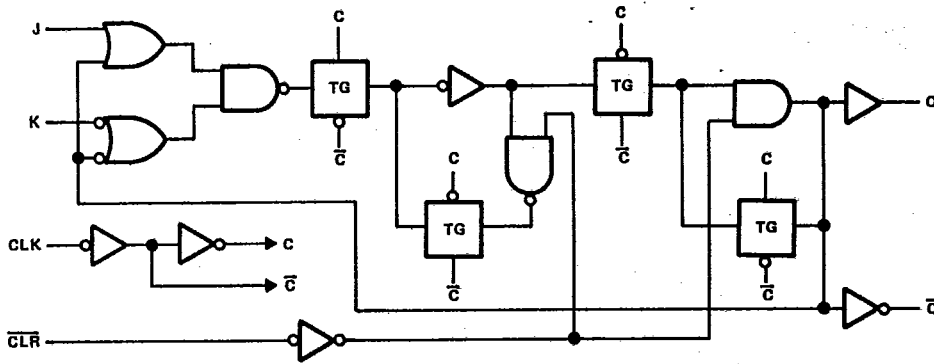
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logic diagram, each flip-flop (positive logic)



2 HCMOS Devices

absolute maximum ratings over operating free-air temperature †

| | |
|-----------------------------------------------------------------------------|----------------|
| Supply voltage, V_{CC} | -0.5 V to 7 V |
| Input clamp current, $I_{IK}(V_i < 0 \text{ or } V_i > V_{CC})$ | ± 20 mA |
| Output clamp current, $I_{OK}(V_O < 0 \text{ or } V_O > V_{CC})$ | ± 20 mA |
| Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$ | ± 25 mA |
| Continuous current through V_{CC} or GND pins | ± 50 mA |
| Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package | 300°C |
| Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package | 260°C |
| Storage temperature range | -65°C to 150°C |

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| Symbol | Parameter | Conditions | SN54HC107 | | | SN74HC107 | | | UNIT |
|----------|----------------------------------------|--------------------------|-----------|----------|-----|-----------|----------|-----|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2 \text{ V}$ | 1.5 | | | 1.5 | | | V |
| | | $V_{CC} = 4.5 \text{ V}$ | 3.15 | | | 3.15 | | | |
| | | $V_{CC} = 6 \text{ V}$ | 4.2 | | | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2 \text{ V}$ | 0 | 0.3 | | 0 | 0.3 | | V |
| | | $V_{CC} = 4.5 \text{ V}$ | 0 | 0.9 | | 0 | 0.9 | | |
| | | $V_{CC} = 6 \text{ V}$ | 0 | 1.2 | | 0 | 1.2 | | |
| V_i | Input voltage | | 0 | V_{CC} | | 0 | V_{CC} | V | |
| V_O | Output voltage | | 0 | V_{CC} | | 0 | V_{CC} | V | |
| t_t | Input transition (rise and fall) times | $V_{CC} = 2 \text{ V}$ | 0 | 1000 | | 0 | 1000 | | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 0 | 500 | | 0 | 500 | | |
| | | $V_{CC} = 6 \text{ V}$ | 0 | 400 | | 0 | 400 | | |
| T_A | Operating free-air temperature | | -55 | 125 | | -40 | 85 | °C | |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54HC107 | | SN74HC107 | | UNIT |
|-----------------|---------------------------------------------------------------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | V _I = V _{IH} or V _{IL} , I _{OH} = -4 mA | 4.5 V | 3.98 | 4.30 | | 3.7 | | 3.84 | | |
| | V _I = V _{IH} or V _{IL} , I _{OH} = -5.2 mA | 6 V | 5.48 | 5.80 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | V _I = V _{IH} or V _{IL} , I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | V _I = V _{IH} or V _{IL} , I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 4 | | 80 | | 40 | μA |
| C _I | | 2 to 6 V | | 3 | 10 | | 10 | | 10 | pF |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | V _{CC} | T _A = 25°C | | | SN54HC107 | | SN74HC107 | | UNIT |
|-------------------------------------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| f _{clock} Clock frequency | 2 V | 0 | 6 | 0 | 4.2 | 0 | 5 | MHz | |
| | 4.5 V | 0 | 31 | 0 | 21 | 0 | 25 | | |
| | 6 V | 0 | 36 | 0 | 25 | 0 | 29 | | |
| t _w Pulse duration | CLR low | 2 V | 100 | | 150 | | 125 | ns | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 25 | | 21 | | |
| | CLK high or low | 2 V | 80 | | 120 | | 100 | | |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} Setup time before CLKI | Data (J, K) | 2 V | 100 | | 150 | | 125 | ns | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 25 | | 21 | | |
| | CLR inactive | 2 V | 100 | | 150 | | 125 | | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 25 | | 21 | | |
| t _h Hold time, data after CLKI | 2 V | 0 | | 0 | | 0 | ns | | |
| | 4.5 V | 0 | | 0 | | 0 | | | |
| | 6 V | 0 | | 0 | | 0 | | | |

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Note 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC107 | | SN74HC107 | | UNIT |
|------------------|--------------|----------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 6 | 9 | | 4.2 | | 5 | MHz | |
| | | | 4.5 V | 31 | 45 | | 21 | | 25 | | |
| | | | 6 V | 36 | 53 | | 25 | | 29 | | |
| t _{pd} | CLR | Q or \bar{Q} | 2 V | | 126 | 155 | | 235 | | 195 | ns |
| | | | 4.5 V | | 25 | 31 | | 47 | | 39 | |
| | | | 6 V | | 21 | 26 | | 40 | | 32 | |
| t _{pd} | CLK | Q or \bar{Q} | 2 V | | 100 | 125 | | 185 | | 160 | ns |
| | | | 4.5 V | | 20 | 25 | | 37 | | 32 | |
| | | | 6 V | | 17 | 21 | | 32 | | 27 | |
| t _t | | Q or \bar{Q} | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

| | | | |
|-----------------|---------------------------------------------|--------------------------------|-----------|
| C _{pd} | Power dissipation capacitance per flip-flop | No load, T _A = 25°C | 35 pF typ |
|-----------------|---------------------------------------------|--------------------------------|-----------|

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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