Data Sheet | December 1992 | File Number 3315

CMOS Hex Buffer/Converter

The CD4049UBMS is an inverting hex buffer and features logic level conversion using only one supply (voltage (VCC). The input signal high level (VIH) can exceed the VCC supply voltage when this device is used for logic level conversions. This device is intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (VCC = 5V, VOL ≤ 0.4V, and IOL ≥ 3.3mA.

The CD4049UBMS is designated as replacement for CD4009UB. Because the CD4049UBMS requires only one power supply, it is preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB in all inverter, current driver, or logic level conversion applications. In these applications the CD4049UBMS is pin compatible with the CD4009UB, and can be substituted for this device in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UBMS, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UBMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Features

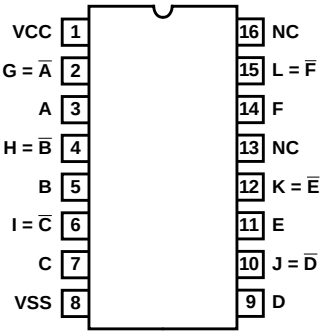
- **High Voltage Type (20V Rating)**
- **Inverting Type**
- **High Sink Current for Driving 2 TTL Loads**
- **High-to-Low Level Logic Conversion**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **5V, 10V and 15V Parametric Ratings**

Applications

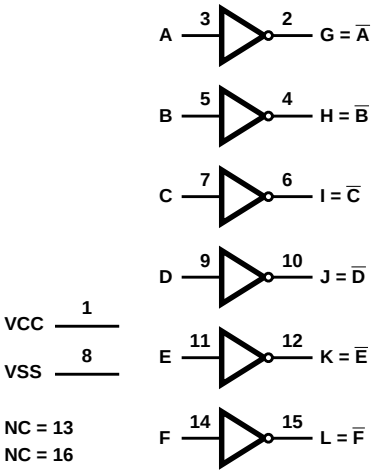
- **CMOS to DTL/TTL Hex Converter**
- **CMOS Current “Sink” or “Source” Driver**
- **CMOS High-to-Low Logic Level Converter**

Pinout

CD4049UBMS
TOP VIEW



Functional Diagram



Schematic

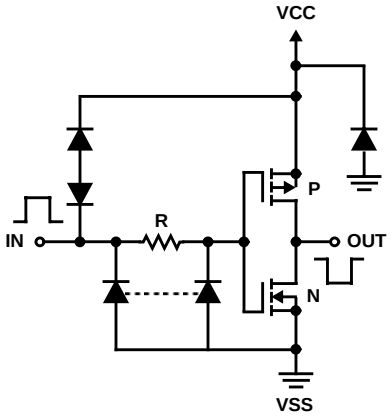


FIGURE 1. SCHEMATIC DIAGRAM, 1 OF 6 IDENTICAL UNITS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Package Types D, F, K, H
Storage Temperature Range (TSTG). . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering) . . . . . $+265^oC$
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	$80^oC/W$	$20^oC/W$
Flatpack Package	$70^oC/W$	$20^oC/W$

Maximum Package Power Dissipation (PD) at $+125^oC$
For TA = -55^oC to $+100^oC$ (Package Type D, F, K) 500mW
For TA = $+100^oC$ to $+125^oC$ (Package Type D, F, K) . . . . . Derate Linearity at 12mW/^oC to 200mW
Device Dissipation per Output Transistor. 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . $+175^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^oC$	-	2	µA
				2	$+125^oC$	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55^oC	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-100	-	nA
				2	$+125^oC$	-1000	-	nA
			VDD = 18V	3	-55^oC	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-	100	nA
				2	$+125^oC$	-	1000	nA
			VDD = 18V	3	-55^oC	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	14.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V		1	$+25^oC$	2.6	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^oC$	3.2	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^oC$	8.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^oC$	24	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^oC$	-	-0.8	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^oC$	-	-3.2	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^oC$	-	-1.8	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^oC$	-	-6.0	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	$+25^oC$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	$+25^oC$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^oC$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^oC$			
		VDD = 3V, VIN = VDD or GND		8B	-55^oC			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	12.5	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	65	ns
			10, 11	+125°C, -55°C	-	88	ns
Propagation Delay	TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	60	ns
			10, 11	+125°C, -55°C	-	81	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	160	ns
			10, 11	+125°C, -55°C	-	216	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+125°C	1.8	-	mA
				-55°C	3.3	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.4	-	mA
				-55°C	4.0	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	5.6	-	mA
				-55°C	10	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	18	-	mA
				-55°C	26	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.48	mA
				-55°C	-	-0.81	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.55	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-1.18	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-3.1	mA
				-55°C	-	-5.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL	VIN = 10V, VDD = 5V	1, 2, 3	+25^{O}C	-	30	ns
		VIN = 10V, VDD = 10V	1, 2, 3	+25^{O}C	-	40	ns
Propagation Delay	TPLH	VIN = 10V, VDD = 5V	1, 2, 3	+25^{O}C	-	90	ns
		VIN = 10V, VDD = 10V	1, 2, 3	+25^{O}C	-	65	ns
Propagation Delay	TPHL	VIN = 15V, VDD = 5V	1, 2, 3	+25^{O}C	-	20	ns
		VIN = 15V, VDD = 15V	1, 2, 3	+25^{O}C	-	30	ns
Propagation Delay	TPLH	VIN = 15V, VDD = 5V	1, 2, 3	+25^{O}C	-	90	ns
		VIN = 15V, VDD = 15V	1, 2, 3	+25^{O}C	-	50	ns
Transition Time	TTHL	VDD = 10V, VIN = VDD OR GND	1, 2, 3	+25^{O}C	-	40	ns
		VDD = 15V, VIN = VDD OR GND	1, 2, 3	+25^{O}C	-	30	ns
Transition Time	TTLH	VDD = 10V, VIN = VDD OR GND	1, 2, 3	+25^{O}C	-	80	ns
		VDD = 15V, VIN = VDD OR GND	1, 2, 3	+25^{O}C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25^{O}C	-	22.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25^{O}C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25^{O}C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10µA	1, 4	+25^{O}C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25^{O}C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10µA	1, 4	+25^{O}C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25^{O}C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25^{O}C	-	1.35 x +25^{O}C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25^{O}C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25^{O}C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 13, 15	3, 5, 7-9, 11-14	1, 16			
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			
Dynamic Burn-In (Note 3)	13	8	1, 16	2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 13, 15, 16	8	1, 3, 5, 7, 9, 11, 14			

NOTE:

1. Each pin except pin 1, pin 16, and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except pin 1, pin 16, and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Each pin except pin 1, pin 16, and GND will have a series resistor of 4.75K ± 5%, VDD = 18V ± 0.5V

Typical Performance Characteristics

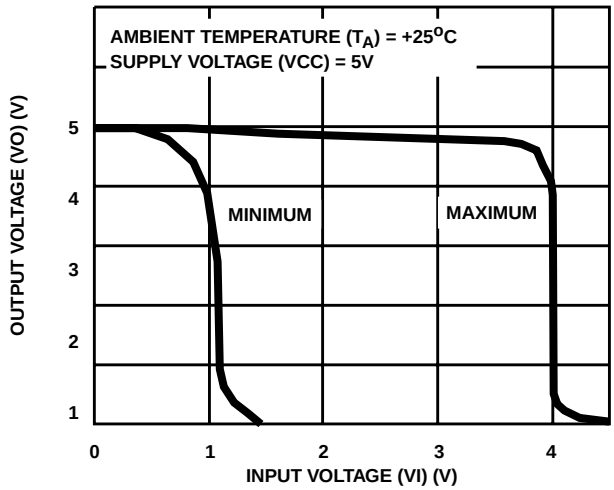


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

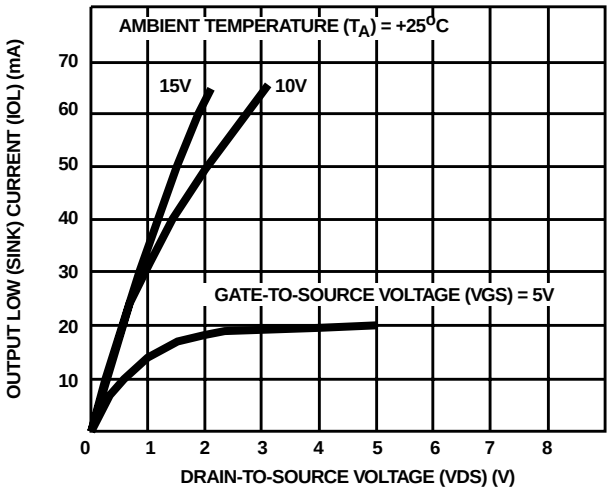


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

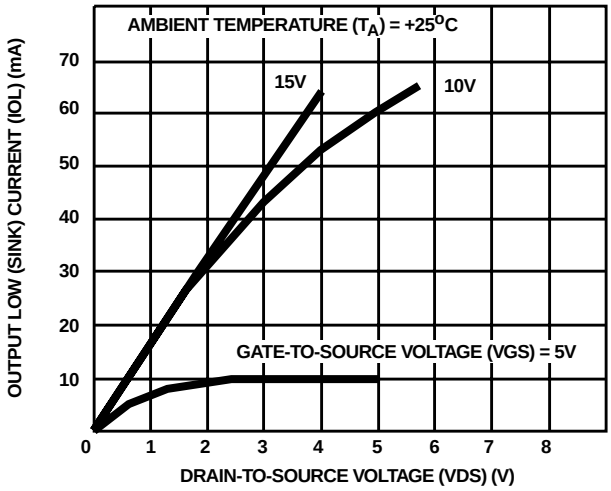


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

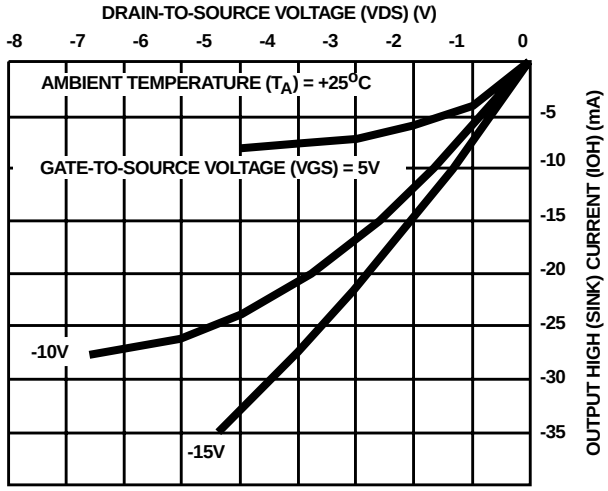


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

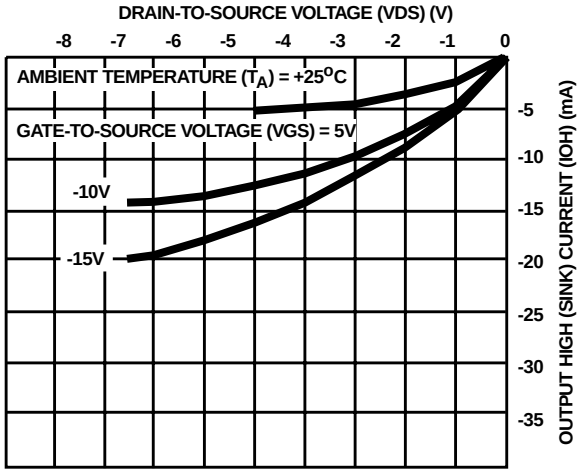


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

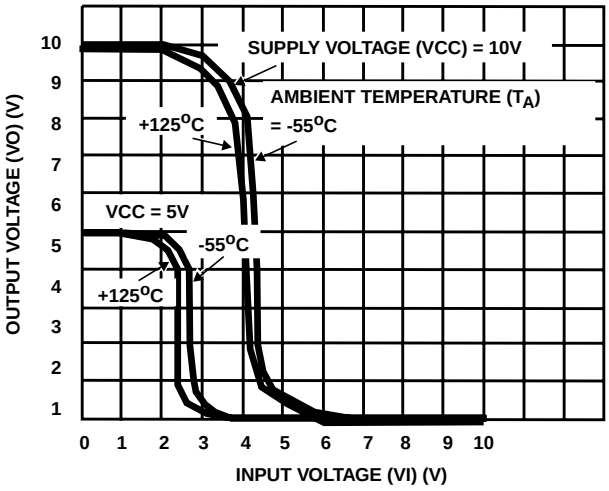


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Typical Performance Characteristics (Continued)

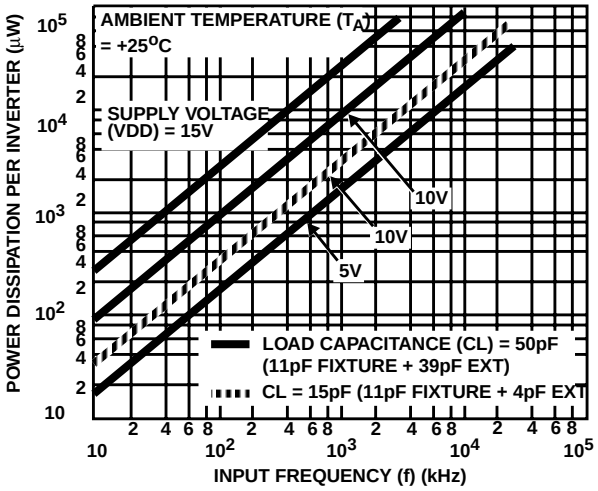


FIGURE 8. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

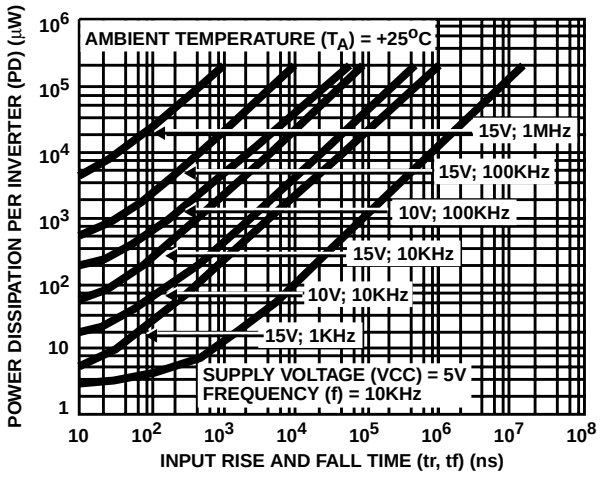
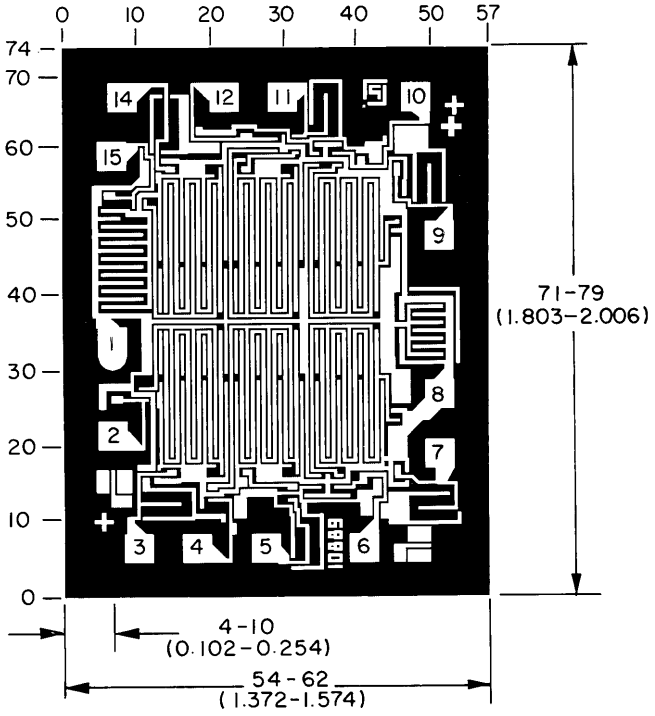


FIGURE 9. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches