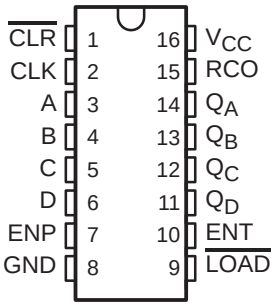
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

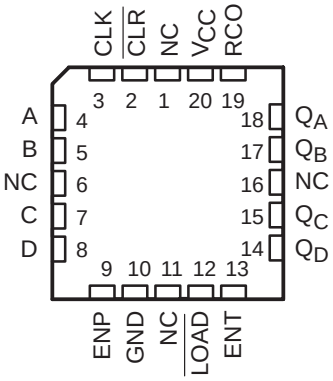
SDAS024A – D2661, APRIL 1982 – REVISED MAY 1986

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160B, 'ALS162B, 'AS160, and 'AS162 are decade counters, and the 'ALS161B, 'ALS163B, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, they may be preset to any number between 0 and 9, or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

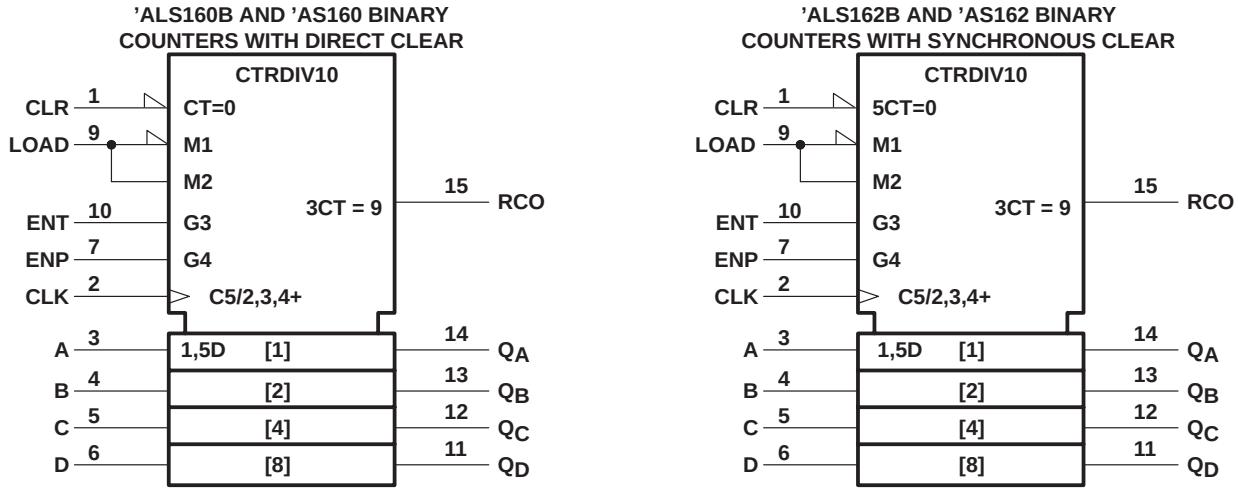
The clear function for the 'ALS160B, 'ALS161B, 'AS160, and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

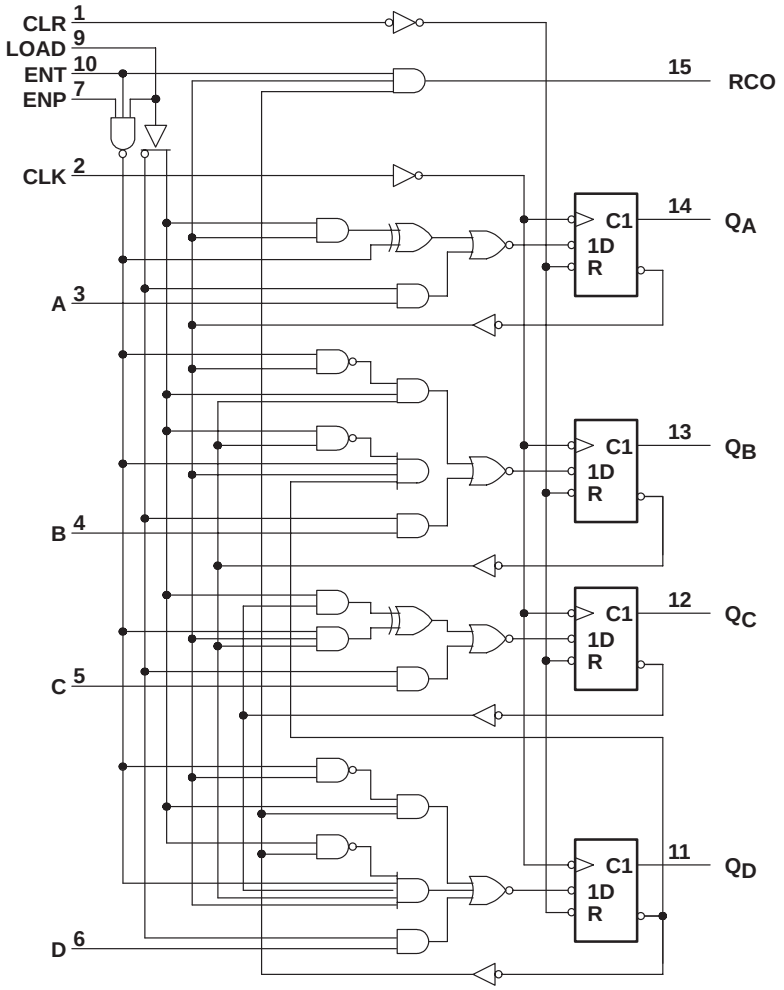
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS160B through SN54ALS163B and SN54AS160 through SN54AS163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS160B through SN74ALS163B and SN74AS160 through SN74AS163 are characterized for operation from 0°C to 70°C.

logic symbols†

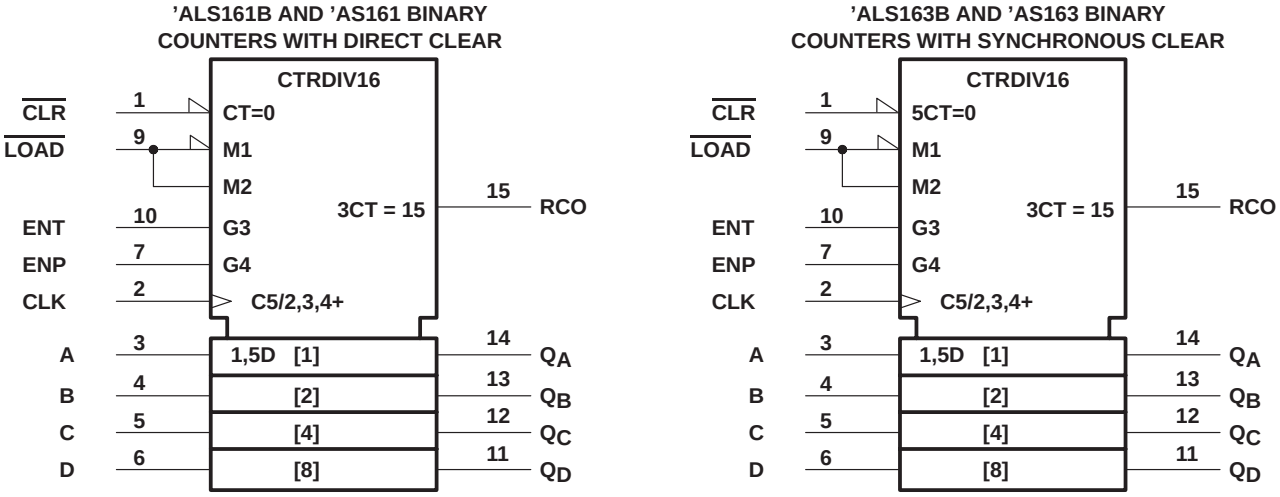


'ALS160B and 'AS160 logic diagram (positive logic)

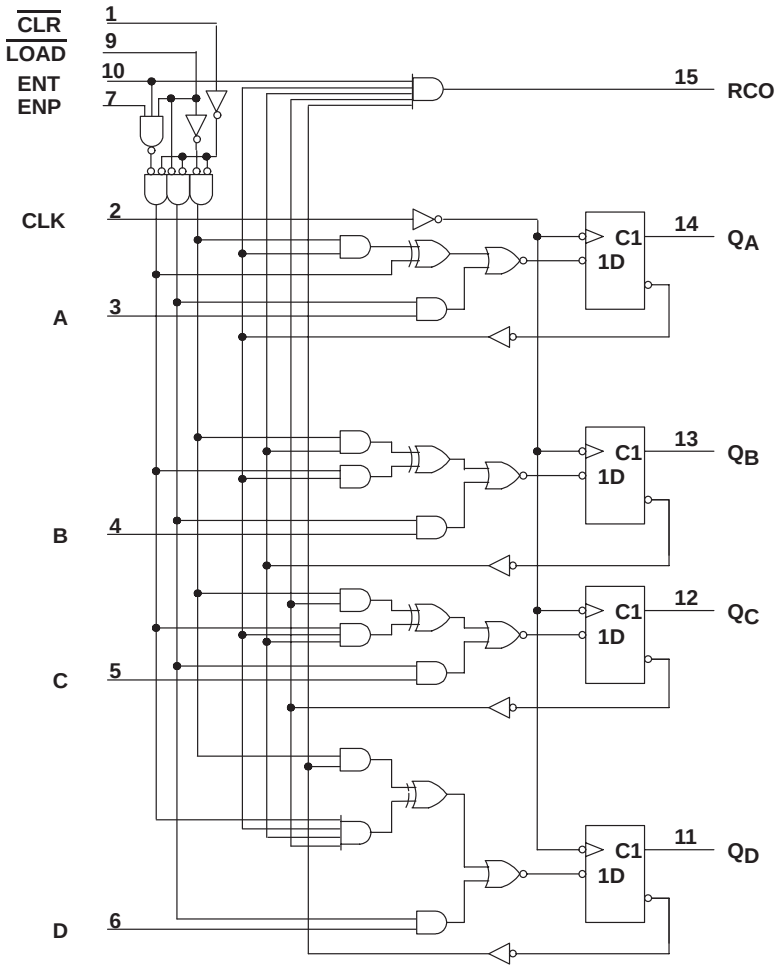


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.
'ALS162B and 'AS162 decade counters are similar; however the clear is synchronous as shown for the 'ALS163B and 'AS163 binary counters.

logic symbols†



'ALS163B and 'AS163 logic diagram (positive logic)



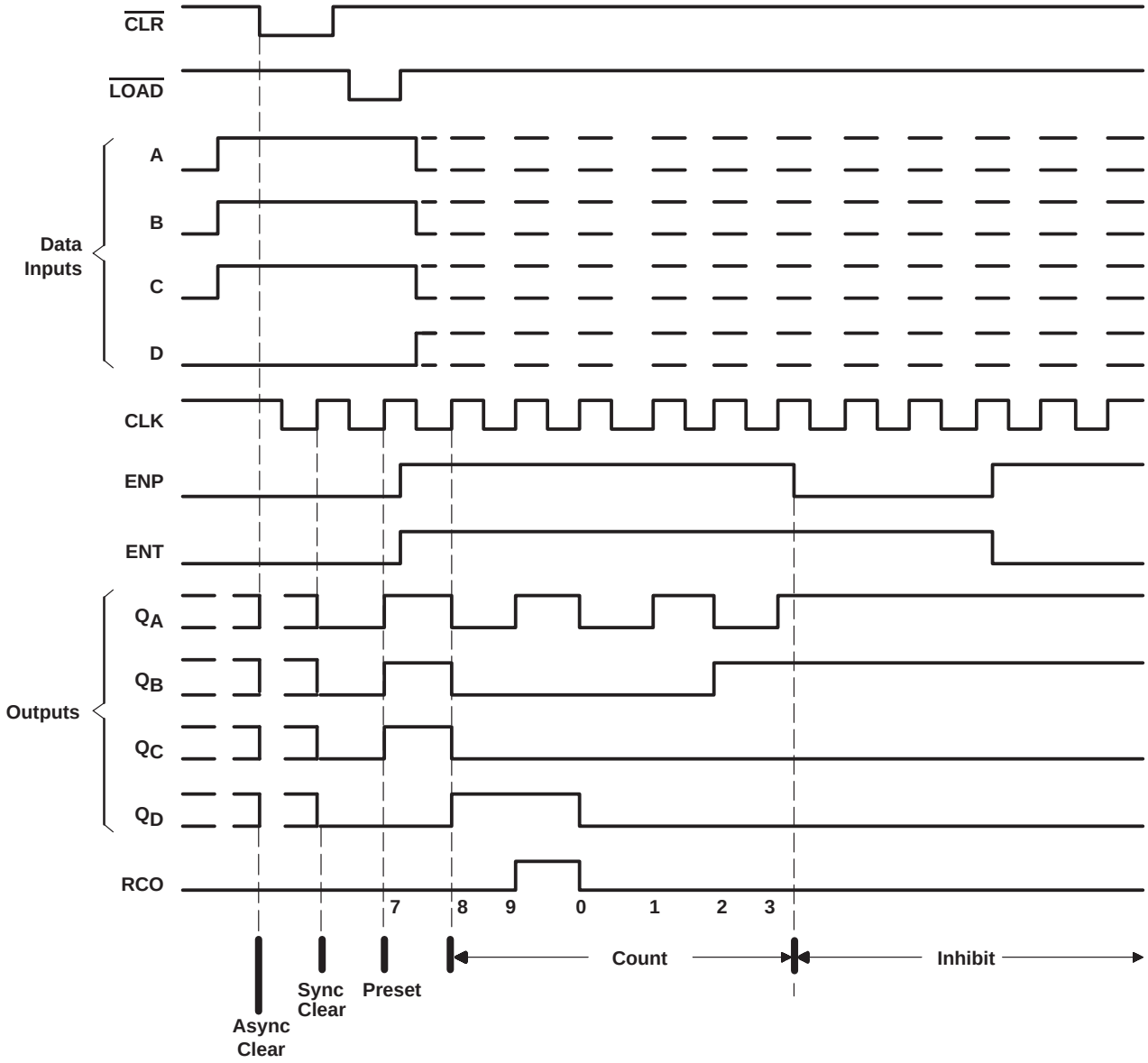
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.
'ALS161B and 'AS161 synchronous binary counters are similar; however the clear is asynchronous as shown for the 'ALS160B and 'AS160 decade counters.

typical clear, preset, count, and inhibit sequences

'ALS160B, 'AS160, 'ALS162B, 'AS162

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS160B and 'AS160 are asynchronous; 'ALS162B and 'AS1162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

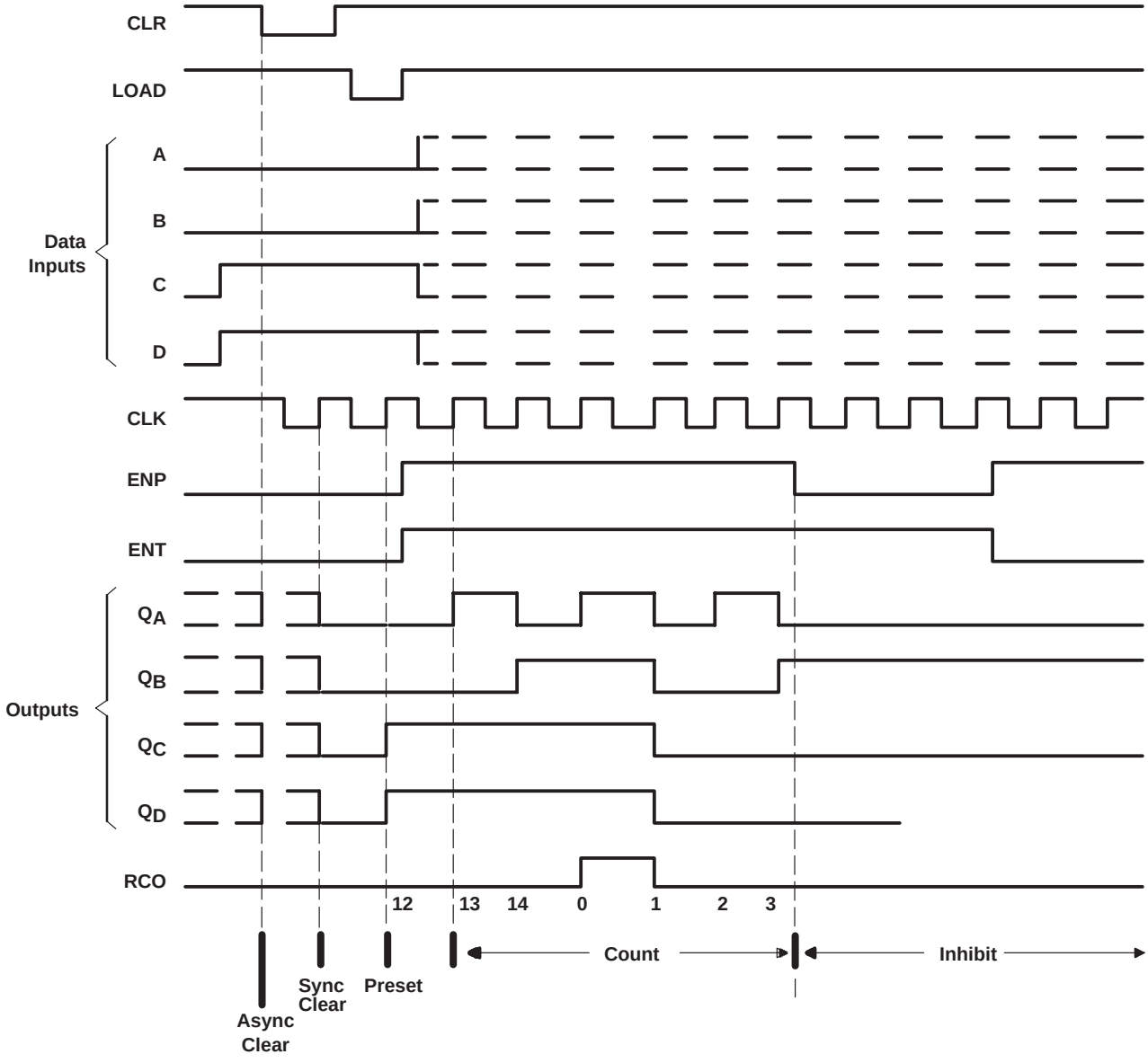


typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, 'AS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fiften, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS160B thru SN54ALS163B . . . . . –55°C to 125°C
SN74ALS160B thru SN74ALS163B . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

				SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					–0.4			–0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency			0		22	0		40	MHz
t_w	Pulse duration	CLR high or low		20			12.5			ns
		’ALS160B, ’ALS161B $\overline{CLR}$ low		20			15			
t_{su}	Setup time before CLK↑	A, B, C, D		50			15			ns
		$\overline{LOAD}$		20			15			
		ENP, ENT	’ALS160B, ’ALS161B	25			15			
			’ALS162B, ’ALS163B	20			15			
		’ALS160B, ’ALS161B	$\overline{CLR}$ inactive	10			10			
		’ALS162B, ’ALS163B	$\overline{CLR}$ low	20			15			
			$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V			12	21		12	21	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS160B, 'ALS161B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160B SN54ALS161B		SN74ALS160B SN74ALS161B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	RCO	5	34	5	20	ns
t_{PHL}			5	27	5	20	
t_{PLH}	CLK	Any Q	4	19	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	18	3	13	ns
t_{PHL}			3	17	3	13	
t_{PHL}	$\overline{CLR}$	Any Q	8	27	8	24	ns
t_{PHL}	$\overline{CLR}$	RCO	11	32	11	23	ns

'ALS162B, 'ALS163B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162B SN54ALS163B		SN74ALS162B SN74ALS163B		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLK	RCO	5	25	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	16	3	13	ns
t_{PHL}			3	16	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS160 thru SN54AS163 . . . . . –55°C to 125°C
SN74AS160 thru SN74AS163 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

				SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					–2			–2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		65	0		75	MHz
t_w	Pulse duration	CLR high or low		7.7			6.7			ns
		’ALS160, ’ALS161 $\overline{CLR}$ low		10			8			
t_{su}	Setup time before CLK↑	A, B, C, D		10			8			ns
		$\overline{LOAD}$		10			8			
		ENP, ENT		10			8			
		’ALS160, ’ALS161 $\overline{CLR}$ inactive		10			8			
		’ALS162, ’ALS163	$\overline{CLR}$ low	14			12			
			$\overline{CLR}$ high (inactive)	10			9			
t_h	Hold time, all synchronous inputs after CLK↑			2			0			ns
T_A	Operating free-air temperature			–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	ENT					0.2			0.2	
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	µA
	ENT					40			40	
	All other					20			20	
I_{IL}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			–1.5			–1.5	mA
	ENT					–1			–1	
	All other					–0.5			–0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V			35	53		35	53	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

’AS160, ’AS161 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS160 SN54AS161		SN74AS160 SN74AS161		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PHL}	$\overline{CLR}$	Any Q	2	14	2	13	ns
t_{PHL}	$\overline{CLR}$	RCO	2	14	2	12.5	ns

’AS162, ’AS163 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS162 SN54AS163		SN74AS162 SN74AS163		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

N–bit synchronous counters

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The ’ALS160B, ’AS160, ’ALS162B, and ’AS162 will count in BCD and the ’ALS161B, ’AS161, ’ALS163B, and ’AS163 will count in binary. When additional stages are added, the f_{MAX} decreases in Figure 1 , but remains unchanged in Figure 2.

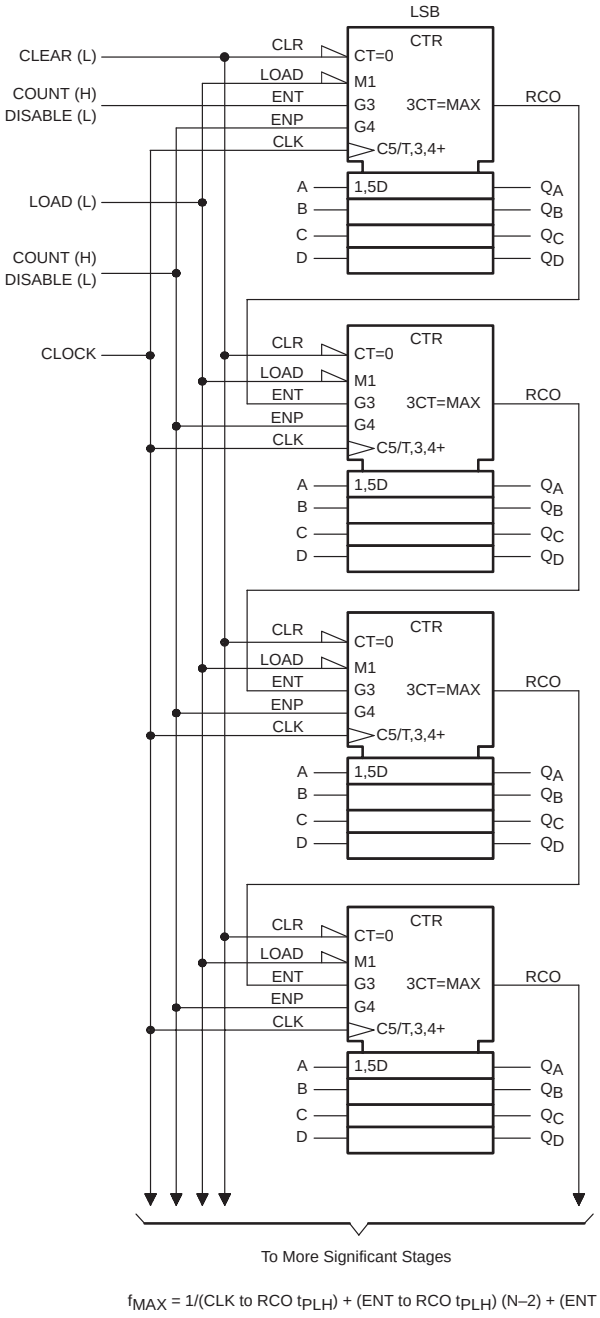


Figure 1. Ripple Mode Carry Circuit

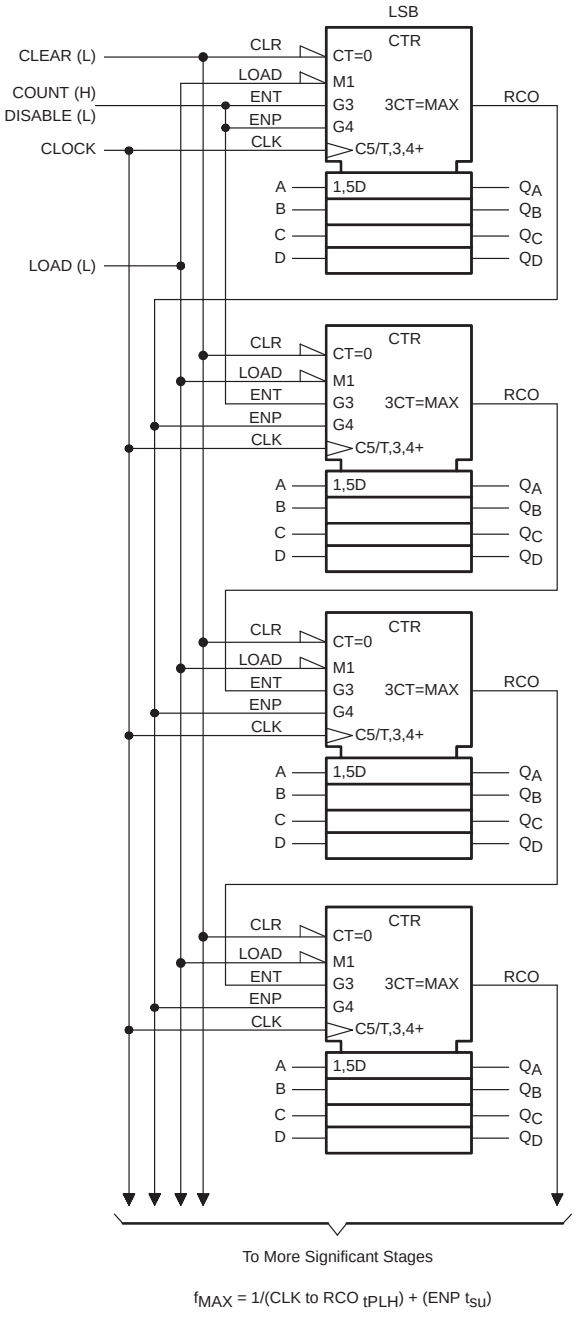


Figure 2. Carry-Look-Ahesd Circuit

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