

MAX14850

Six-Channel Digital Isolator

General Description

The MAX14850 is a six-channel digital isolator utilizing Maxim's proprietary process technology, whose monolithic design provides a compact and low-cost transfer of digital signals between circuits with different power domains. The technology enables low power consumption and stable high-temperature performance.

The four unidirectional channels are each capable of DC to 50Mbps, with two of the four channels passing data across the isolation barrier in each direction. The two bidirectional channels are open drain and each is capable of data rates from DC to 2Mbps.

Independent 3.0V to 5.5V supplies on each side of the isolator also make it suitable for use as a level translator. The MAX14850 can be used for isolating SPI busses, I²C busses with clock stretching, RS-232, RS-485/RS-422 busses, and general-purpose isolation. When used as a bus isolator, extra channels are available for power monitoring and reset signals.

The MAX14850 is available in a narrow body, 16-pin SO (10mm x 4mm) package. The SO package is specified over the -40°C to +125°C automotive temperature range.

Applications

Industrial Control Systems
I²C, SPI, SMBus, PMBus™ Interfaces
Isolated RS-232, RS-485/RS-422
Telecommunication Systems
Battery Management
Medical Systems

For related parts and recommended products to use with this part, refer to: www.maxim-ic.com/MAX14850.related

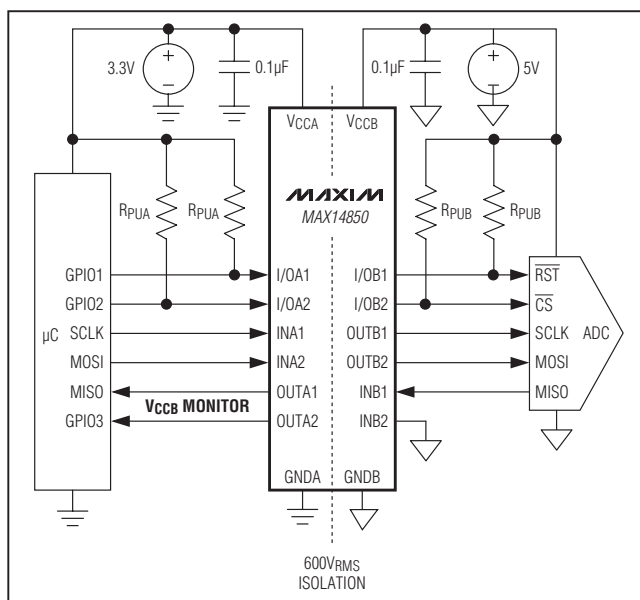
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Benefits and Features

- ◆ **Protection from High-Voltage Environments**
 - ◇ 600V_{RMS} Isolation for 60 Seconds
 - ◇ Short-Circuit Protection on Unidirectional Outputs
- ◆ **Complete Digital Isolation Solution**
 - ◇ Four Unidirectional Signal Paths: 2-In/2-Out
 - ◇ Two Bidirectional Open-Drain Signal Paths
 - ◇ 50Mbps (max) Unidirectional Data Rate
 - ◇ 2Mbps (max) Bidirectional Data Rate
- ◆ **Compatible with Many Interface Standards**
 - ◇ I²C With Clock Stretching
 - ◇ SPI
 - ◇ RS-232, RS-422/RS-485
 - ◇ SMBus, PMBus Interfaces

Ordering Information appears at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V_{CCA} to GNDA	-0.3V to +6V
V_{CCB} to GNDB	-0.3V to +6V
OUTA1, OUTA2 to GNDA	-0.3V to ($V_{CCA} + 0.3V$)
OUTB1, OUTB2 to GNDB	-0.3V to ($V_{CCB} + 0.3V$)
INB1, INB2, I/OA1, I/OA2 to GNDA	-0.3V to +6V
INA1, INA2, I/OB1, I/OB2 to GNDB	-0.3V to +6V
Short-Circuit Duration (OUTA_ to GNDA or V_{CCA} , OUTB_ to GNDB or V_{CCB})	Continuous
Continuous Current (I/OA_, I/OB_) Pin	$\pm 50mA$

Continuous Power Dissipation ($T_A = +70^\circ C$)	
SO (derate 13.3mW/ $^\circ C$ above $+70^\circ C$)	1067mW
Operating Temperature Range	$-40^\circ C$ to $+125^\circ C$
Junction Temperature	$+150^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$
Soldering Temperature (reflow)	$+260^\circ C$

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SO

Junction-to-Ambient Thermal Resistance (θ_{JA})	$75^\circ C/W$
Junction-to-Case Thermal Resistance (θ_{JC})	$24^\circ C/W$

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CCA} - V_{GNDA} = 3.0V$ to $5.5V$, $V_{CCB} - V_{GNDB} = 3.0V$ to $5.5V$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $V_{CCA} - V_{GNDA} = 3.3V$, $V_{CCB} - V_{GNDB} = 3.3V$, and $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNIT
DC CHARACTERISTICS									
Supply Voltage	V _{CCA}	Relative to GNDA				3.0		5.5	V
	V _{CCB}	Relative to GNDB				3.0		5.5	
Supply Current	I _{CCA} , I _{CCB}	Unidirectional inputs at DC or 2Mbps; bidirectional inputs at DC or switching at 2Mbps. No load.	V _{CCA} = +5V, V _{CCB} = +5V			7.2		11	mA
			V _{CCA} = +3.3V, V _{CCB} = +3.3V			6.2		9.5	
		All inputs switching at max data rate. No load. (Note 3)	V _{CCA} = +5V, V _{CCB} = +5V	T _A = +25°C		15		22	
				T _A = +125°C		17		24	
			V _{CCA} = +3.3V, V _{CCB} = +3.3V	T _A = +25°C		10		16	
				T _A = +125°C		11		18	
Undervoltage Lockout Threshold	V _{UVLO}	V _{CCA} - V _{GNDA} , V _{CCB} - V _{GNDB} (Note 4)					2		V
Undervoltage Lockout Hysteresis	V _{UVLOHYS}	V _{CCA} - V _{GNDA} , V _{CCB} - V _{GNDB} (Note 4)					0.1		V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CCA} - V_{GNDA} = 3.0V$ to $5.5V$, $V_{CCB} - V_{GNDB} = 3.0V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{CCA} - V_{GNDA} = 3.3V$, $V_{CCB} - V_{GNDB} = 3.3V$, and $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ISOLATION CHARACTERISTICS						
Isolation Voltage	V_{ISO}	$t = 60s$ (Note 5)	600			V_{RMS}
Working Isolation Voltage	V_{IOWM}	$V_{GNDB} - V_{GNDA}$ continuous (Note 3), 50-year life expectancy (Figure 4)			200	V_{RMS}
ESD Protection		All pins		± 2.5		kV
LOGIC INPUTS AND OUTPUTS						
Input Threshold Voltage	V_{IT}	I/OA1, I/OA2, relative to GNDA	0.5		0.7	V
Input Logic-High Voltage	V_{IH}	INA1, INA2, relative to GNDA	$0.7 \times V_{CCA}$			V
		INB1, INB2, relative to GNDB	$0.7 \times V_{CCB}$			
		I/OA1, I/OA2, relative to GNDA	0.7			
		I/OB1, I/OB2, relative to GNDB	$0.7 \times V_{CCB}$			
Input Logic-Low Voltage	V_{IL}	INA1, INA2, relative to GNDA			0.8	V
		INB1, INB2, relative to GNDB			0.8	
		I/OA1, I/OA2, relative to GNDA			0.5	
		I/OB1, I/OB2, relative to GNDB			$0.3 \times V_{CCB}$	
Output Logic-High Voltage	V_{OH}	OUTA1, OUTA2, relative to GNDA, source current = 4mA	$V_{CCA} - 0.4$			V
		OUTB1, OUTB2, relative to GNDB, source current = 4mA	$V_{CCB} - 0.4$			
Output Logic-Low Voltage	V_{OL}	OUTA1, OUTA2, relative to GNDA, sink current = 4mA			0.8	V
		OUTB1, OUTB2, relative to GNDB, sink current = 4mA			0.8	
		I/OA1, I/OA2, relative to GNDA, sink current = 10mA	0.6		0.9	
		I/OA1, I/OA2, relative to GNDA, sink current = 0.5mA	0.6		0.85	
		I/OB1, I/OB2, relative to GNDB, sink current = 30mA			0.4	
Input/Output Logic-Low Threshold Difference	ΔV_{TOL}	I/OA1, I/OA2 (Note 6)	50			mV
Input Capacitance	C_{IN}	INA1, INA2, INB1, INB2, $f = 1MHz$		2		pF
DYNAMIC SWITCHING CHARACTERISTICS						
Common-Mode Transient Immunity	dV_{ISO}/dt	$V_{IN} = V_{CC-}$ or V_{GND-} (Notes 3, 7)		1.5		kV/ μs

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CCA} - V_{GNDA} = 3.0V$ to $5.5V$, $V_{CCB} - V_{GNDB} = 3.0V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{CCA} - V_{GNDA} = 3.3V$, $V_{CCB} - V_{GNDB} = 3.3V$, and $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Data Rate (Note 3)	DR_{MAX}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2	50			Mbps
		I/OA1 to I/OB1, I/OA2 to I/OB2, I/OB1 to I/OA1, I/OB2 to I/OA2	2			
Minimum Pulse Width	PW_{MIN}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2 (Note 3)	20			ns
Propagation Delay (Note 3)	t_{DPLH} t_{DPHL}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2, $R_L = 1M\Omega$, $C_L = 15pF$, Figure 1		20	30	ns
				18	26	
		I/OA1 to I/OB1, I/OA2 to I/OB2, $R_1 = 1.6k\Omega$, $R_2 = 180\Omega$, $C_{L1} = C_{L2} = 15pF$, Figure 2		30	100	
				30	100	
		I/OB1 to I/OA1, I/OB2 to I/OA2, $R_1 = 1k\Omega$, $R_2 = 120\Omega$, $C_{L1} = C_{L2} = 15pF$, Figure 2		60	100	
				60	100	
Pulse-Width Distortion $ t_{DPLH} - t_{DPHL} $ (Notes 3, 8)	PWD	INA1 TO OUTB1, INA2 TO OUTB2, INB1 TO OUTA1, INB2 TO OUTA2, $R_L = 1M\Omega$, $C_L = 15pF$, Figure 1			7	ns
					7	
		I/OA1 to I/OB1, I/OA2 to I/OB2, $R_1 = 1.6k\Omega$, $R_2 = 180\Omega$, $C_{L1} = C_{L2} = 15pF$, Figure 2			12	
					12	
		I/OB1 to I/OA1, I/OB2 to I/OA2, $R_1 = 1k\Omega$, $R_2 = 120\Omega$, $C_{L1} = C_{L2} = 15pF$, Figure 2			60	
					50	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CCA} - V_{GND A} = 3.0V$ to $5.5V$, $V_{CCB} - V_{GND B} = 3.0V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{CCA} - V_{GND A} = 3.3V$, $V_{CCB} - V_{GND B} = 3.3V$, and $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Channel-to-Channel Skew (Notes 3, 8)	$t_{DSKEWCC}$	OUTB1 to OUTB2 output skew, Figure 1	$V_{CCA} = V_{CCB} = +3.3V$			3	ns
			$V_{CCA} = V_{CCB} = +5V$			3	
		OUTA1 to OUTA2 output skew, Figure 1	$V_{CCA} = V_{CCB} = +3.3V$			3	
			$V_{CCA} = V_{CCB} = +5V$			3	
		I/OB1 to I/OB2 output skew, Figure 2	$V_{CCA} = V_{CCB} = +3.3V$			6	
			$V_{CCA} = V_{CCB} = +5V$			5	
		I/OA1 to I/OA2 output skew, Figure 2	$V_{CCA} = V_{CCB} = +3.3V$			20	
			$V_{CCA} = V_{CCB} = +5V$			20	
Part-to-Part Skew (Notes 3, 8)	$t_{DSKEWPP}$	$\Delta t_{DPLH}, \Delta t_{DPHL}$				8	ns
Rise Time (Note 3)	t_R	OUTA1, OUTA2, OUTB1, OUTB2, 10% to 90%, Figure 1				5	ns
Fall Time (Note 3)	t_F	OUTA1, OUTA2, OUTB1, OUTB2, 90% to 10%, Figure 1				5	ns
		I/OA1, I/OA2, 90% to 10%, $R_1 = 1.6k\Omega$, $R_2 = 180\Omega$, $C_{L1} = C_{L2} = 15pF$, Figure 2	$V_{CCA} = V_{CCB} = +3.3V$		30	60	
			$V_{CCA} = V_{CCB} = +5V$		40	80	
		I/OB1, I/OB2, 90% to 10%, $R_1 = 1k\Omega$, $R_2 = 120\Omega$, $C_{L1} = C_{L2} = 15pF$, Figure 2	$V_{CCA} = V_{CCB} = +3.3V$		3	6	
			$V_{CCA} = V_{CCB} = +5V$		3	5	

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INSULATION AND SAFETY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
IEC INSULATION AND SAFETY RELATED FOR SPECIFICATIONS FOR SOIC-16				
External Tracking (Creepage)	CPG	IEC 60664-1	4.2	mm
External Air Gap (Clearance)	CLR	IEC 60664-1	4.2	mm
Minimum Internal Gap		Insulation thickness	0.0026	mm
Tracking Resistance (Comparative Tracking Index)	CTI	IEC 112/VDE 030 Part 1	175	V
Insulation Resistance Across Barrier	R _{ISO}		1	GΩ
Capacitance Across Isolation Barrier	C _{IO}	f = 1MHz	12	pF
VDE IEC INSULATION CHARACTERISTICS				
Surge Isolation Voltage	V _{IOSM}	IEC 60747-17, section 5.3.1.6 and 5.4.6 for basic insulation	1	kV _{PEAK}
Repetitive Peak Isolation Voltage	V _{IORM}	IEC 60747-17, section 5.3.1.3	282	V _{PEAK}
Rated Transient Isolation Voltage	V _{IOTM}	IEC 60747-17, section 5.3.1.4	850	V _{PEAK}
Safety Limiting Temperature	T _S	IEC 60747-17, section 7.2.1	+150	°C
Safety Limiting Side A Power Dissipation	P _{SA}	IEC 60747-17, section 7.2.1	0.75	W
Safety Limiting Side B Power Dissipation	P _{SB}	IEC 60747-17, section 7.2.1	0.75	W
Apparent Charge Method	q _{pd}	IEC 60747-17, section 7.4, method a and b	5	pC
Overvoltage Category		IEC 60664-1, single- or three-phase 50V DC or AC	I, II	—
Overvoltage Category		IEC 60664-1, single- or three-phase 100V DC or AC	I	—
Climatic Category			40/125/21	—
Pollution Degree		DIN VDE 0110, Table 1	2	—

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. All voltages of side A are referenced to GNDA. All voltages of side B are referenced to GNDB, unless otherwise noted.

Note 3: Guaranteed by design. Not production tested.

Note 4: The undervoltage lockout threshold and hysteresis guarantee that the outputs are in a known state during a slump in the supplies. See the [Detailed Description](#) section for more information.

Note 5: The isolation is guaranteed for t = 60s, and tested at 120% of the guaranteed value for 1s.

Note 6: $\Delta V_{TOL} = V_{OL} - V_{IL}$. This is the minimum difference between the output logic-low voltage and the input logic threshold for the same I/O pin. This ensures that the I/O channels are not latched low when any of the I/O inputs are driven low (see the [Bidirectional Channels](#) section).

Note 7: The common-mode transient immunity guarantees that the device will hold its outputs stable when the isolation voltage changes at the specified rate.

Note 8: Pulse-width distortion is defined as the difference in propagation delay between low-to-high and high-to-low transitions on the same channel. Channel-to-channel skew is defined as the difference in propagation delay between different channels on the same device. Part-to-part skew is defined as the difference in propagation delays (for unidirectional channels) between different devices, when both devices operate with the same supply voltage, at the same temperature and have identical package and test circuits.

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Test Circuits/Timing Diagrams

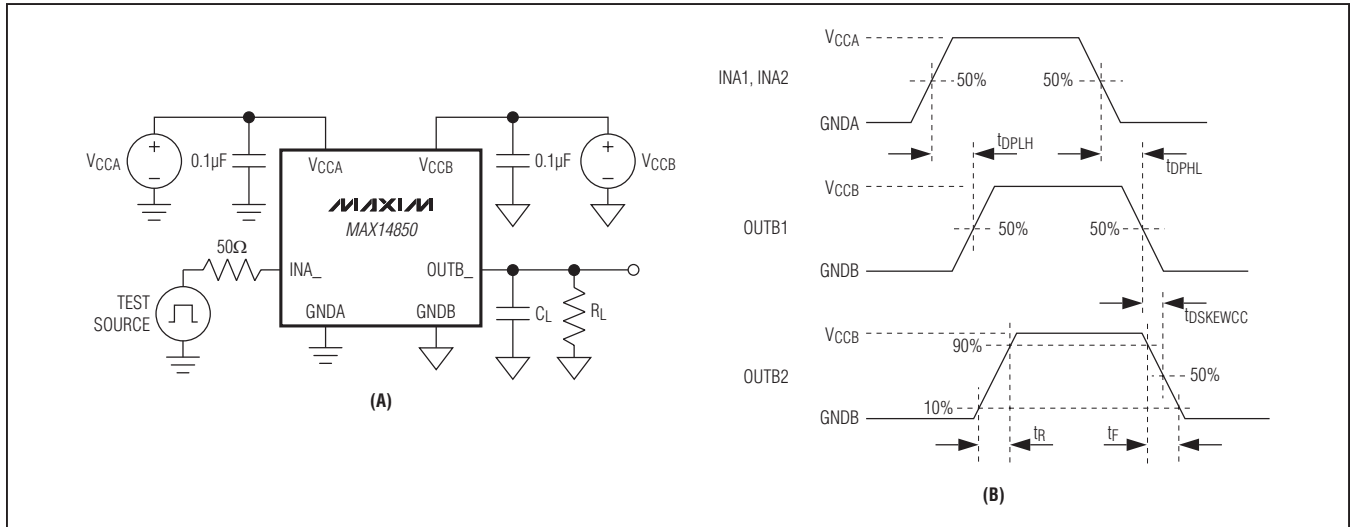


Figure 1. Test Circuit (A) and Timing Diagram (B) for Unidirectional Channels

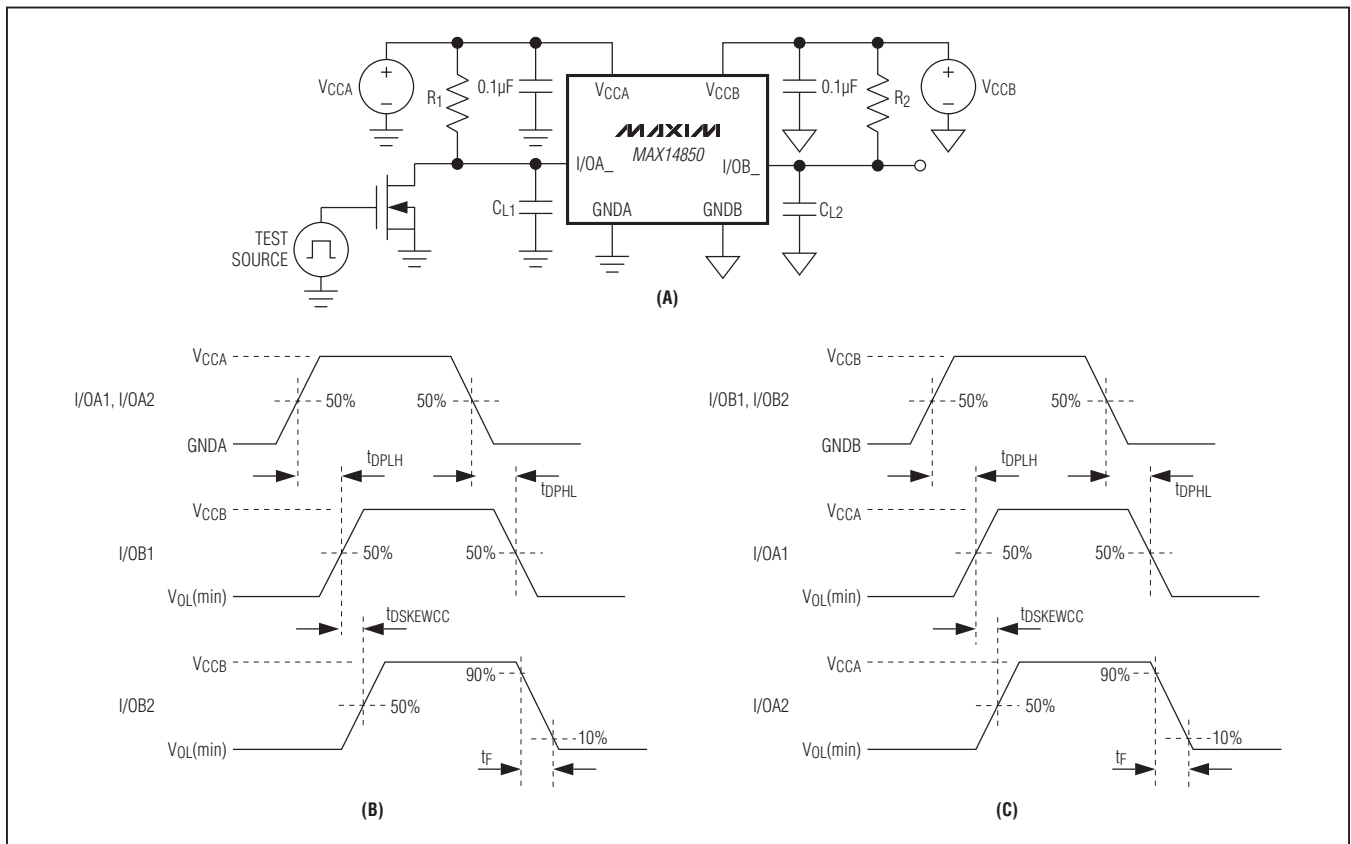
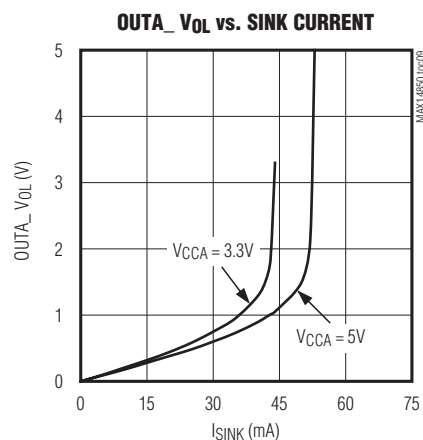
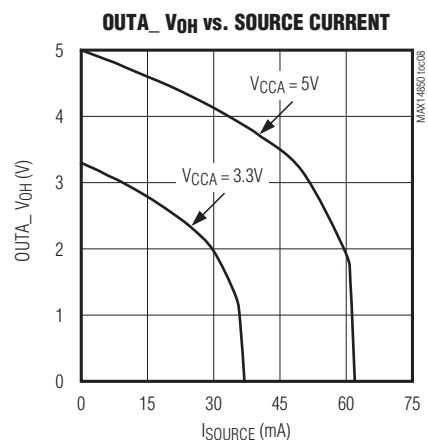
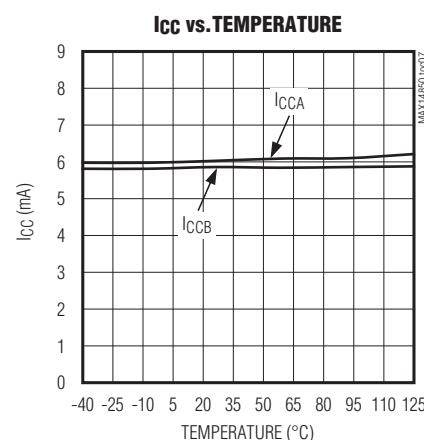
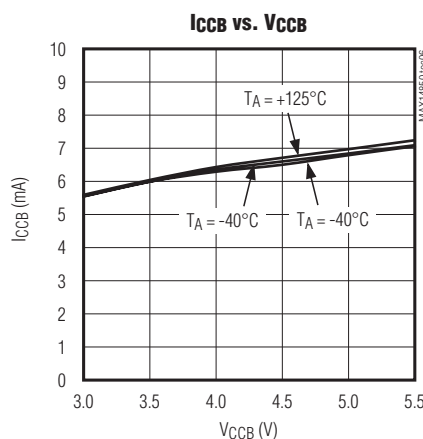
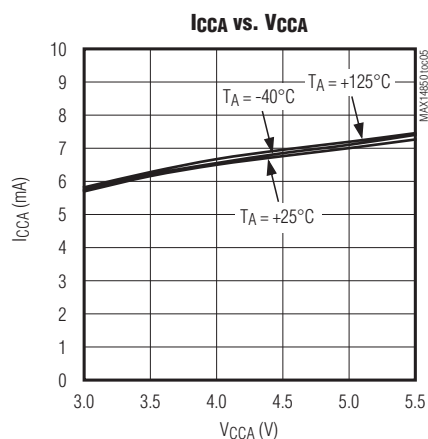
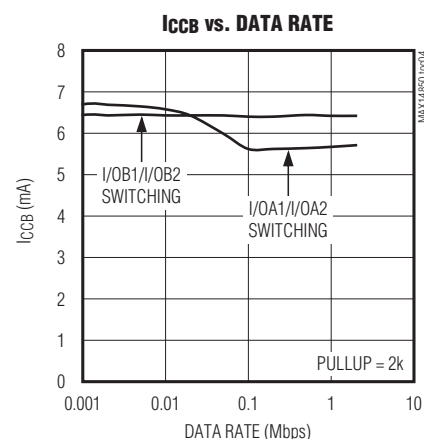
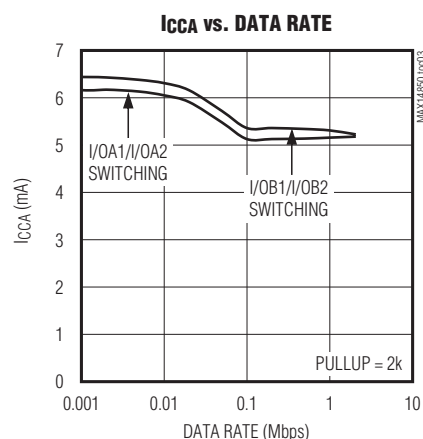
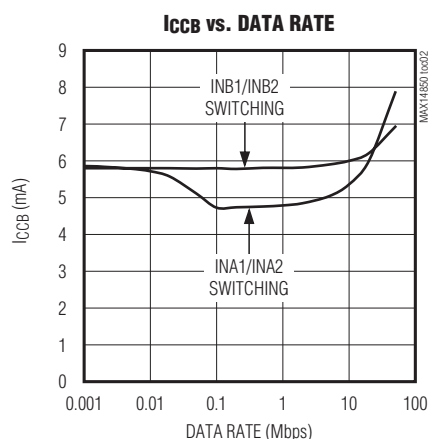
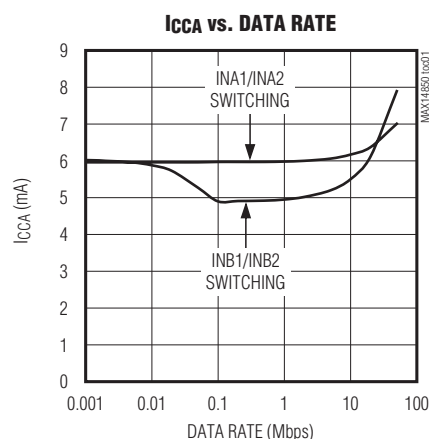


Figure 2. Test Circuit (A) and Timing Diagrams (B) and (C) for Bidirectional Channels

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Typical Operating Characteristics

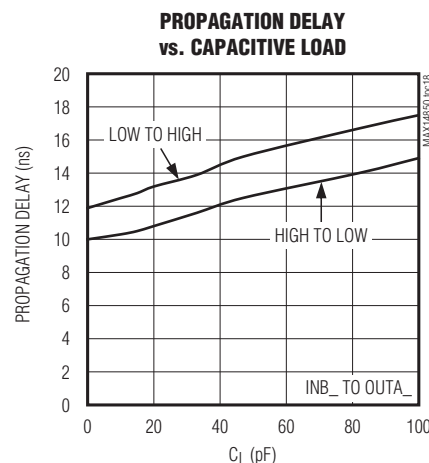
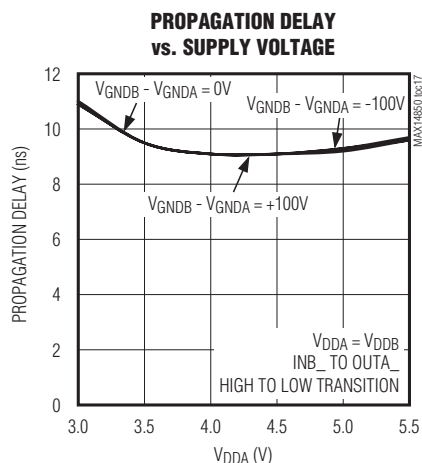
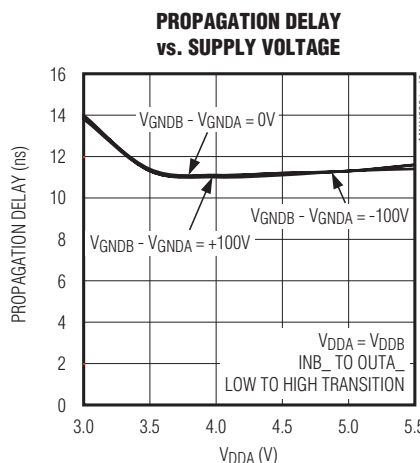
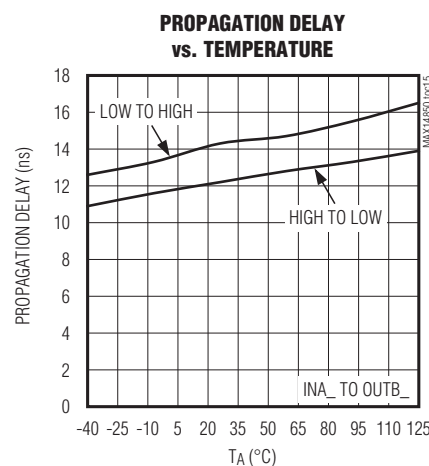
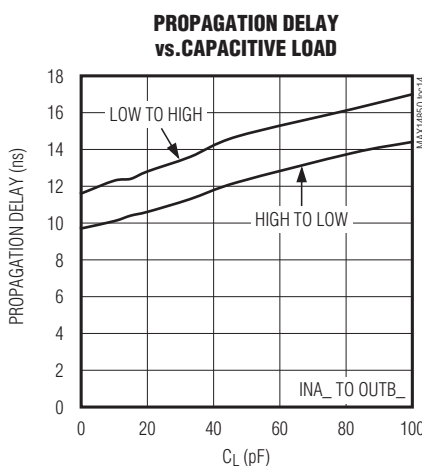
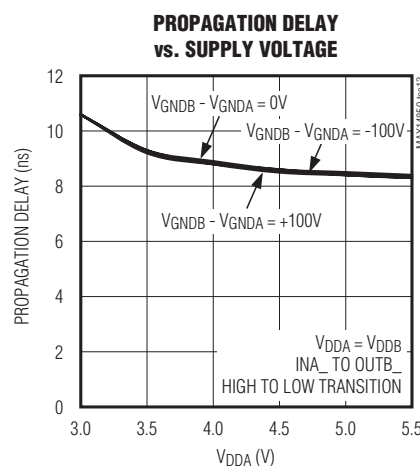
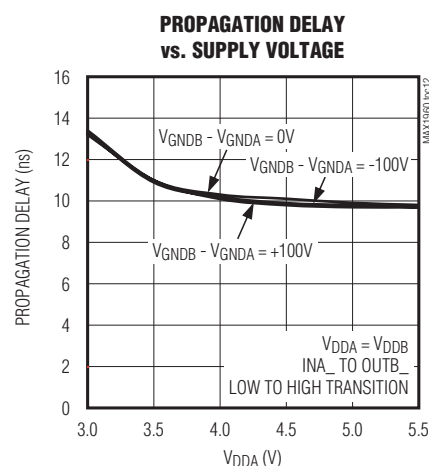
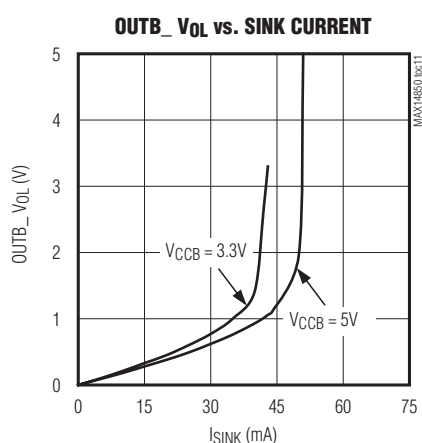
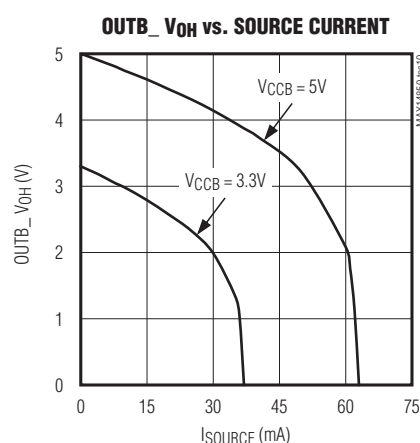
($V_{CCA} - V_{GND A} = 3.3V$, $V_{CCB} - V_{GND B} = 3.3V$, all inputs idle, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

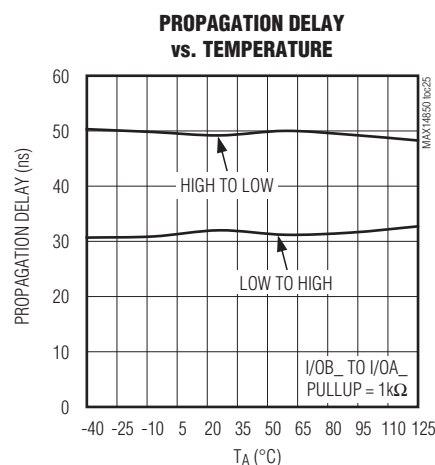
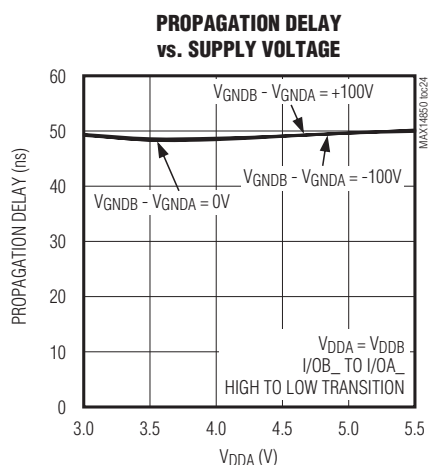
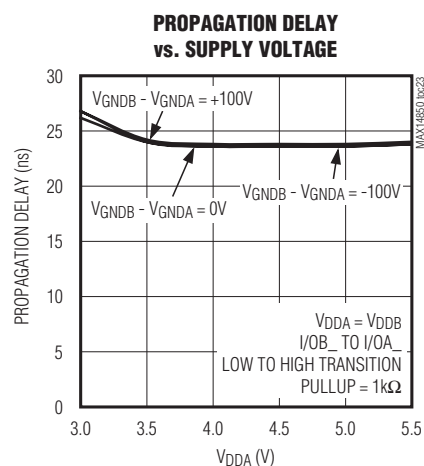
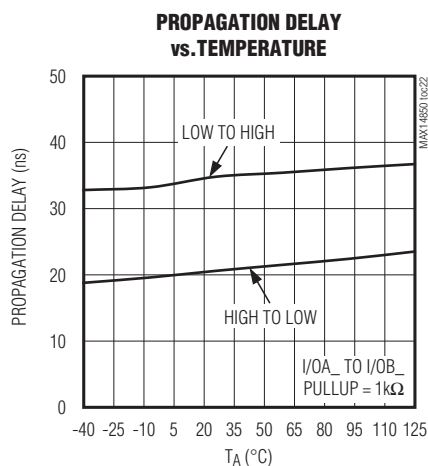
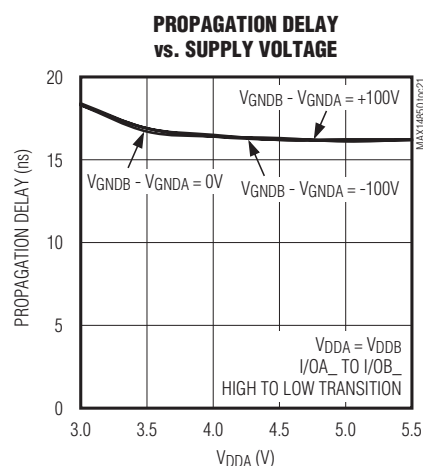
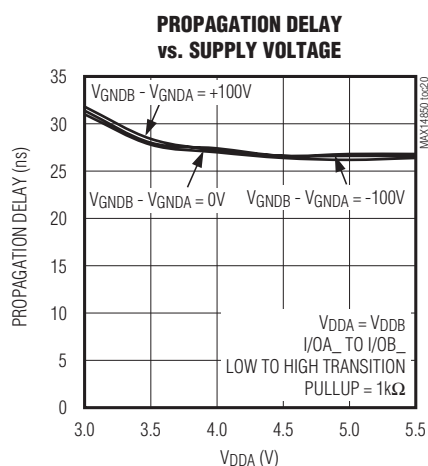
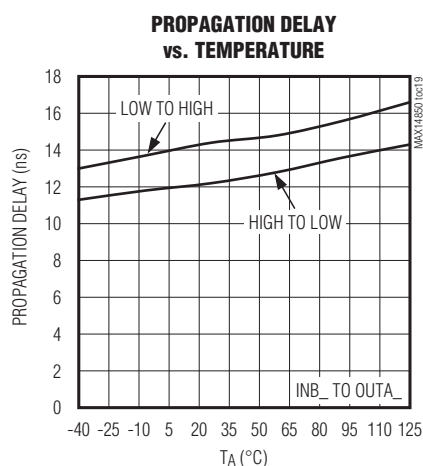
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Typical Operating Characteristics (continued)

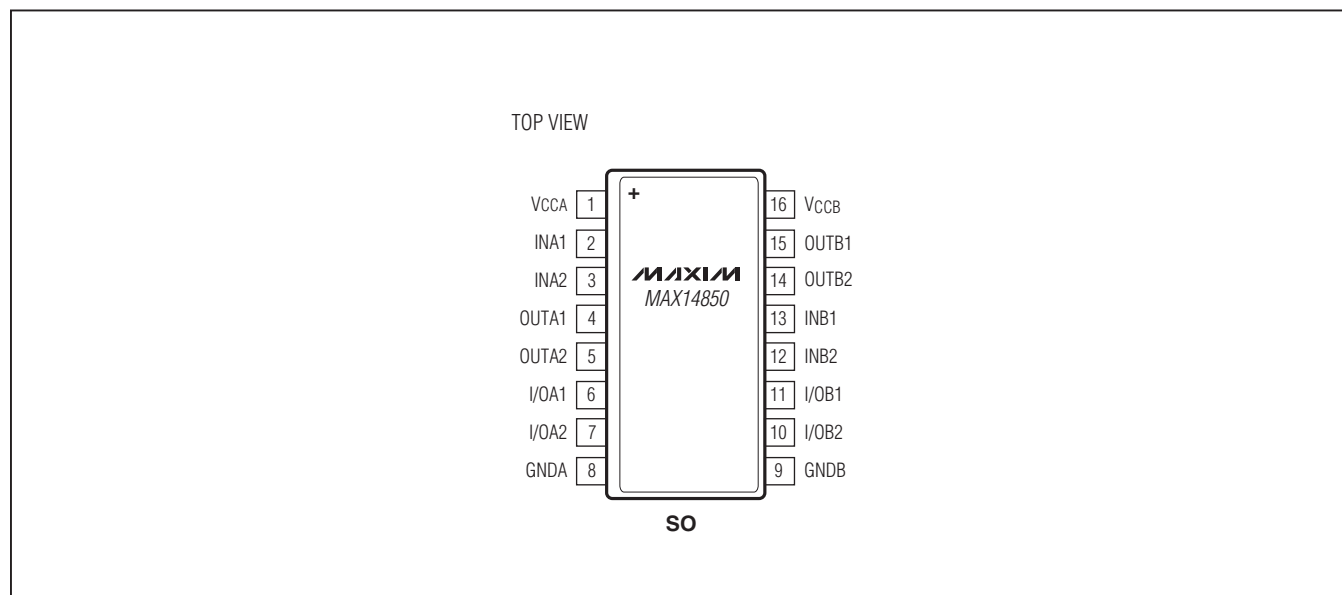
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Pin Configuration



Pin Description

PIN	NAME	FUNCTION	VOLTAGE RELATIVE TO
1	V _{CCA}	Supply Voltage of Logic Side A. Bypass V _{CCA} with a 0.1μF ceramic capacitor to GNDA.	GNDA
2	INA1	Logic Input 1 on Side A. INA1 is translated to OUTB1.	GNDA
3	INA2	Logic Input 2 on Side A. INA2 is translated to OUTB2.	GNDA
4	OUTA1	Logic Output 1 on Side A. OUTA1 is a push-pull output.	GNDA
5	OUTA2	Logic Output 2 on Side A. OUTA2 is a push-pull output.	GNDA
6	I/OA1	Bidirectional Input/Output 1 on Side A. I/OA1 is translated to/from I/OB1 and is a open-drain output.	GNDA
7	I/OA2	Bidirectional Input/Output 2 on Side A. I/OA2 is translated to/from I/OB2 and is a open-drain output.	GNDA
8	GNDA	Ground Reference for Side A	—
9	GNDB	Ground Reference for Side B	—

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Ground Isolation/Level Shifting

The MAX14850 tolerates a ground difference of 600V_{RMS}. Therefore, V_{GNDA} can be 850VDC higher or lower than V_{GNDB}. In addition, the device translates logic levels when (V_{CCA}–V_{GNDA}) is higher or lower voltage than (V_{CCB}–V_{GNDB}), as long as each is within the valid 3.0V to 5.5V range.

Unidirectional and Bidirectional Channels

The MAX14850 operates both as a unidirectional device and bidirectional device simultaneously. Each unidirectional channel can only be used in the direction shown in the functional diagram. The bidirectional channels function without requiring a direction control input.

Unidirectional Channels

The device features four unidirectional channels that operate independently with guaranteed data rates from DC to 50Mbps. The output driver of each unidirectional channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Bidirectional Channels

The device features two bidirectional channels that have open-drain outputs. The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device. The input logic-low threshold (V_{IT}) of I/OA1 and I/OA2 are at least 50mV lower than the output logic-low voltages of I/OA1 and I/OA2. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B, thus preventing a latching action.

The I/OA1, I/OA2, I/OB1, and I/OB2 pins have open-drain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 30mA for side B, and 10mA for side A (see the [Electrical Characteristics](#) table).

The bidirectional channels of the device support I²C clock stretching.

Startup and Undervoltage Lockout

The V_{CCA} and V_{CCB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a slump in the supplies. When an undervoltage event is detected on either of the supplies, all outputs on both sides are automatically controlled, regardless of the status of the inputs. The bidirectional outputs become high impedance and are pulled high by the external pullup resistor on the open-drain output. The unidirectional outputs are pulled high internally to the voltage of the V_{CCA} or V_{CCB} supply during undervoltage conditions.

When an undervoltage condition is detected on either supply, all unidirectional outputs are pulled to the supplies ([Table 1](#)). The bidirectional outputs are high impedance and pulled to the supplies by the external pullup resistors.

Safety Regulatory Approvals

The MAX14850 is safety certified by UL, CSA, and IEC 60747-5-2. Per UL1577, the MAX14850 is 100% tested at an equivalent V_{ISO} of 720V_{RMS} for one second (see [Table 2](#)).

[Figure 3](#) shows the behavior of the outputs during power-up and power-down.

Table 1. Output Behavior During Undervoltage Conditions

V _{IN}	V _{CCA}	V _{CCB}	V _{OUTA}	V _{OUTB}
1	Powered	Powered	1	1
0	Powered	Powered	0	0
X	Under Voltage	Powered	Follows V _{CCA}	1
X	Powered	Under Voltage	1	Follows V _{CCB}

Table 2. Safety Regulatory Approvals (Pending)

SAFETY AGENCY	STANDARD	ISOLATION NUMBER	FILE NUMBER
UL	UL1577 Recognized	600V _{RMS} isolation voltage for 60 seconds	Pending
VDE	Approved to 60747-17	Basic insulation, 600V _{RMS} for 60 seconds	Pending

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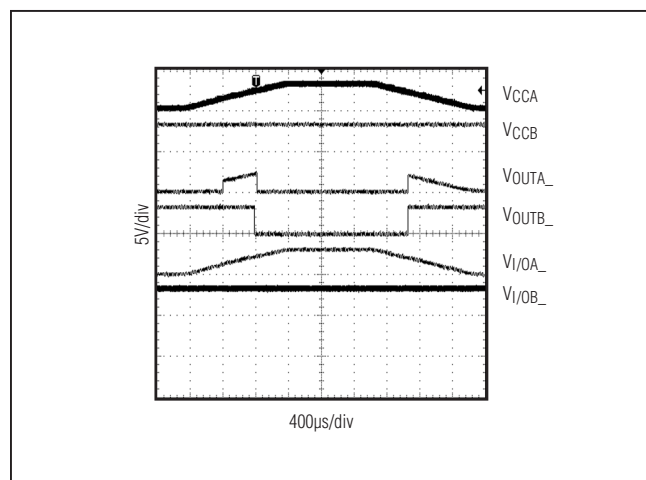


Figure 3. Undervoltage Lockout Behavior

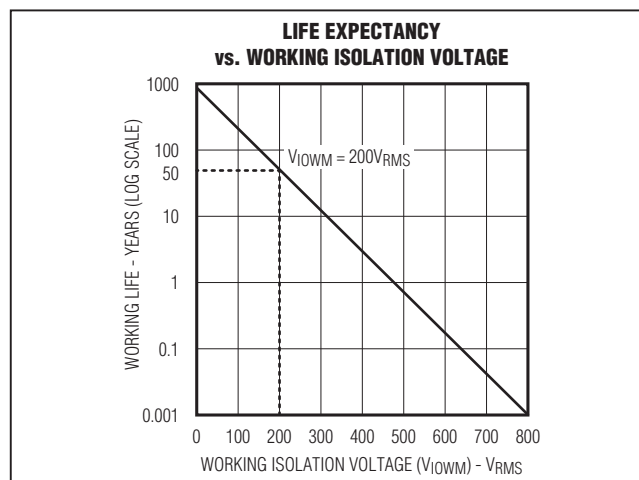


Figure 4. Life Expectancy vs. Working Isolation Voltage

Applications Information

Affect of Continuous Isolation on Lifetime

High-voltage conditions cause insulation to degrade over time. Higher voltages result in faster degradation. Even the high-quality insulating material used in the MAX14850 can degrade over long periods of time with a constant high-voltage across the isolation barrier. [Figure 4](#) shows the life expectancy of the MAX14850 vs. working isolation voltage.

Power-Supply Sequencing

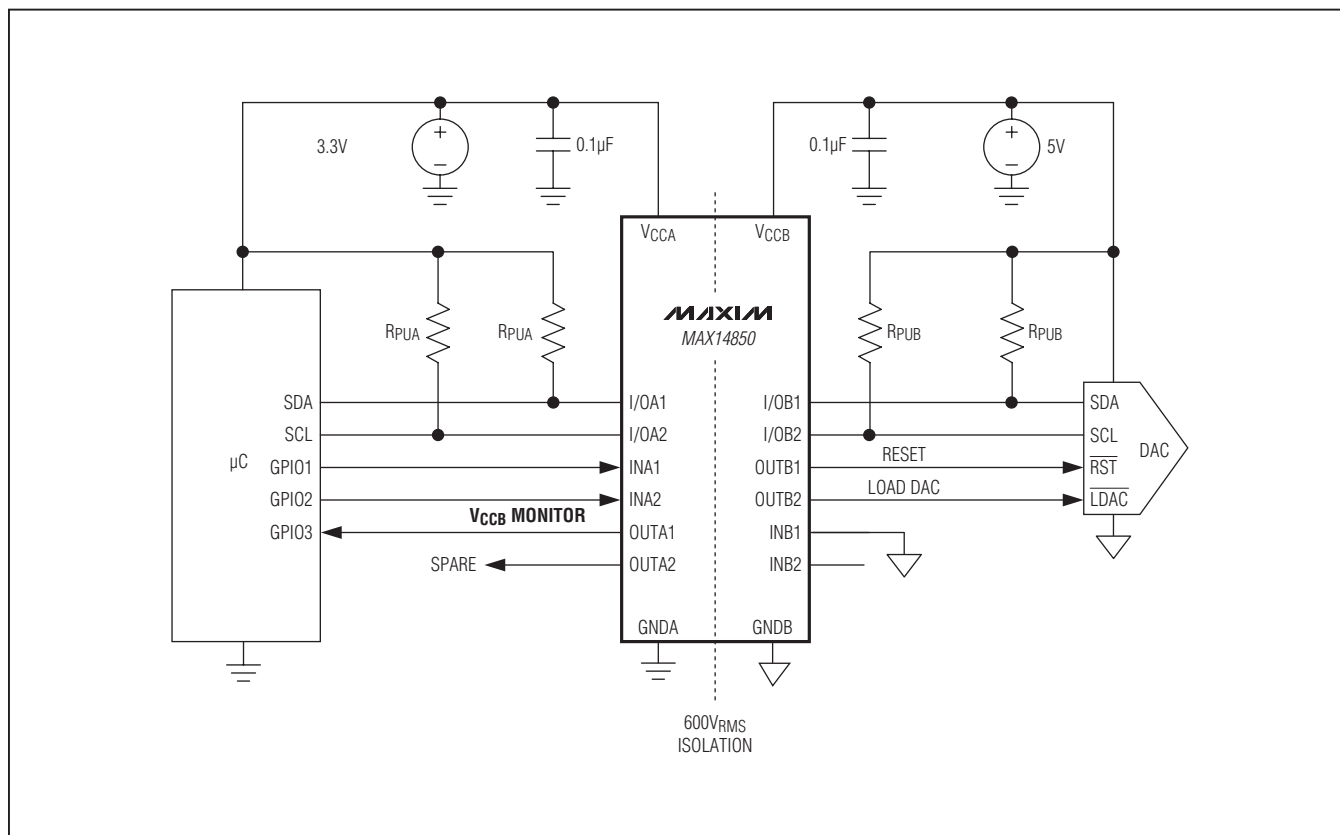
The MAX14850 does not require special power-supply sequencing. The logic levels are set independently on either side by VCCA and VCCB. Each supply can be present over the entire specified range regardless of the level or presence of the other.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass VCCA and VCCB with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

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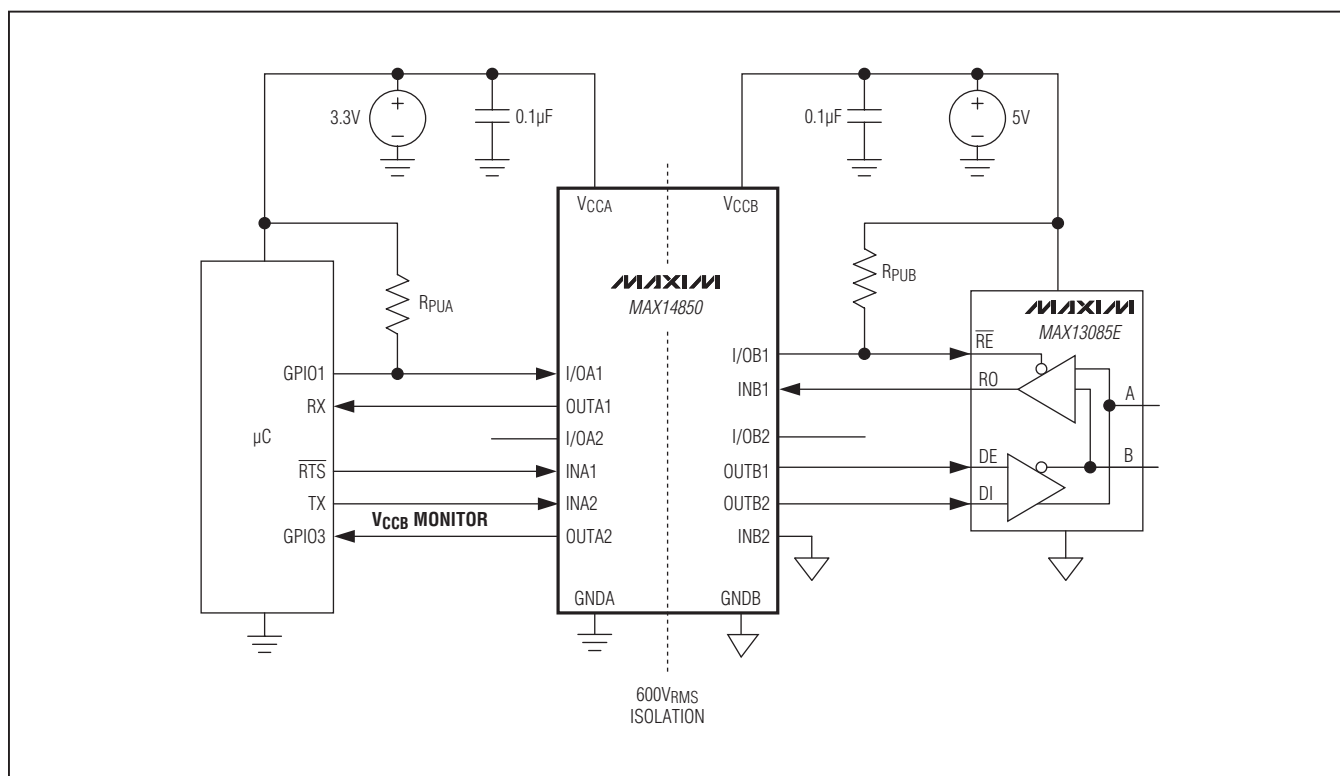
Typical Operating Circuits (continued)



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Typical Operating Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14850ASE+	-40°C to +125°C	16 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SO	S16+3	21-0041	90-0097

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/12	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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