Winbond Electronics Corp.

8K × 8 CMOS STATIC RAM

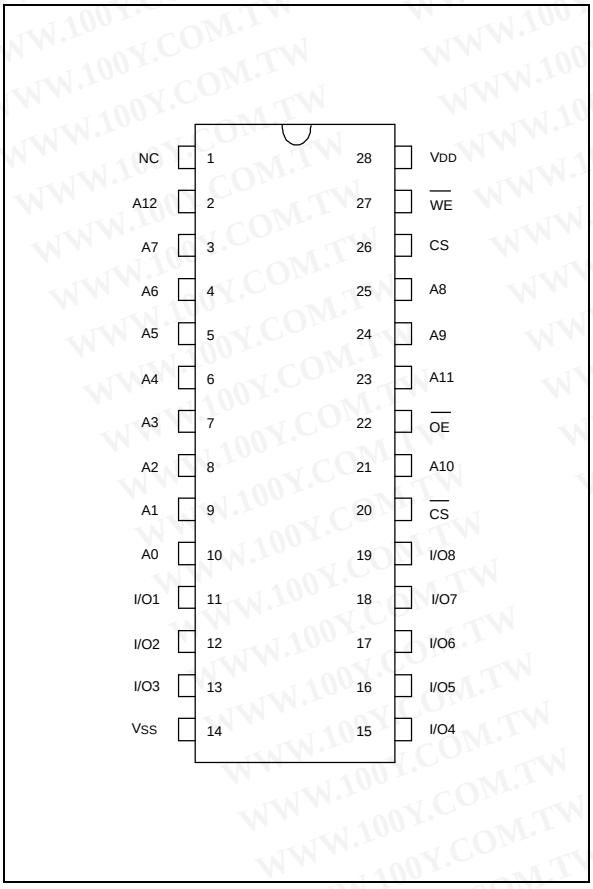
GENERAL DESCRIPTION

The W2465 is a slow-speed, low-power CMOS static RAM organized as 8192 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

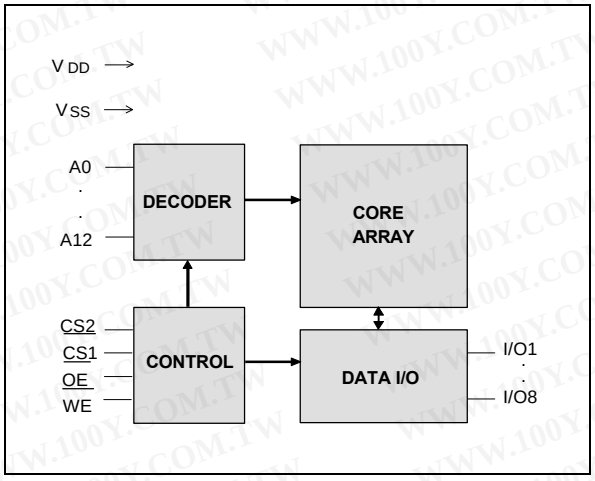
FEATURES

- Low power consumption:
  - Active: 250 mW (max.)
  - Standby: 100 µW (max.)(LL-version)
    250 µW (max.)(L-version)
- Access time: 70/100 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Available packages: 28-pin 600 mil DIP, 330 mil SOP and 300 mil skinny DIP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A12	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

Publication Release Date: April 1997
Revision A8

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1–I/O8	V_{DD} CURRENT
H	X	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Input/Output to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-2	-	+2	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} $\overline{CS1}$ = V_{IH} (min.) or CS2 = V_{IL} (max.) or $\overline{OE}$ = V_{IH} (min.) or $\overline{WE}$ = V_{IL} (max.)		-2	-	+2	µA
Output Low Voltage	V_{OL}	I_{OL} = +4.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS1}$ = V_{IL} (max.), CS2 = V_{IH} (min.) I/O = 0 mA, Cycle = min. Duty = 100%	70	-	-	70	mA
			100	-	-	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} (min.) or CS2 = V_{IL} (max.), Cycle = min. Duty = 100%		-	-	3	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{DD} -0.2V or CS2 ≤ 0.2V	LL	-	-	20	µA
			L	-	-	50	µA

Note: Typical characteristics are at V_{DD} = 5 V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

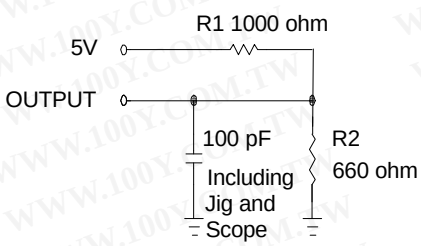
Note: These parameters are sampled but not 100% tested.

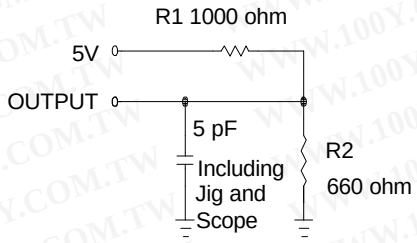
AC CHARACTERISTICS

AC Test Conditions

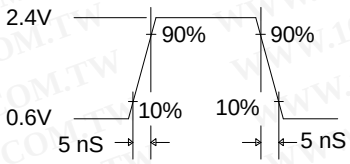
PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100 pF, I_{OH}/I_{OL} = -1 mA/4 mA

AC Test Loads and Waveform





(For T_{CLZ1},T_{CLZ2}, T_{OLZ}, T_{CHZ1},T_{CHZ2}, T_{OHZ}, T_{WHZ},T_{OW})



AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER		SYM.	W2465-70		W2465-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Read Cycle Time		T_{RC}	70	-	100	-	nS
Address Access Time		T_{AA}	-	70	-	100	nS
Chip Select Access Time	$\overline{CS1}$	T_{ACS1}	-	70	-	100	nS
	CS2	T_{ACS2}	-	70	-	100	nS
Output Enable to Output Valid		T_{AOE}	-	35	-	50	nS
Chip Selection to Output in Low Z	$\overline{CS1}$	T_{CLZ1}*	5	-	10	-	nS
	CS2	T_{CLZ2}*	5	-	10	-	nS
Output Enable to Output in Low Z		T_{OLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	$\overline{CS1}$	T_{CHZ1}*	-	30	-	35	nS
	CS2	T_{CHZ2}*	-	30	-	35	nS
Output Disable to Output in High Z		T_{OHZ}*	-	30	-	35	nS
Output Hold from Address Change		T_{OH}	10	-	10	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

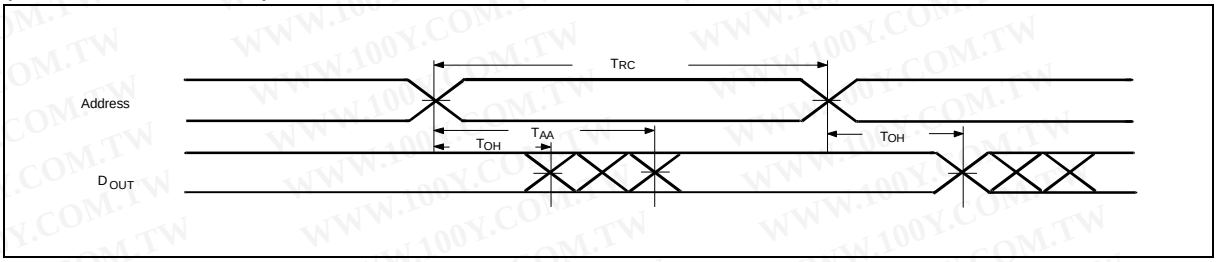
PARAMETER		SYM.	W2465-70		W2465-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	100	-	nS
Chip Selection to End of Write	$\overline{CS1}$	T_{CW1}	60	-	80	-	nS
	CS2	T_{CW2}	60	-	80	-	nS
Address Valid to End of Write		T_{AW}	60	-	80	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	45	-	60	-	nS
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	T_{WR1}	0	-	0	-	nS
	CS2	T_{WR2}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	40	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	30	-	30	nS
Output Disable to Output in High Z		T_{OHZ}*	-	30	-	30	nS
Output Active from End of Write		T_{OW}	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

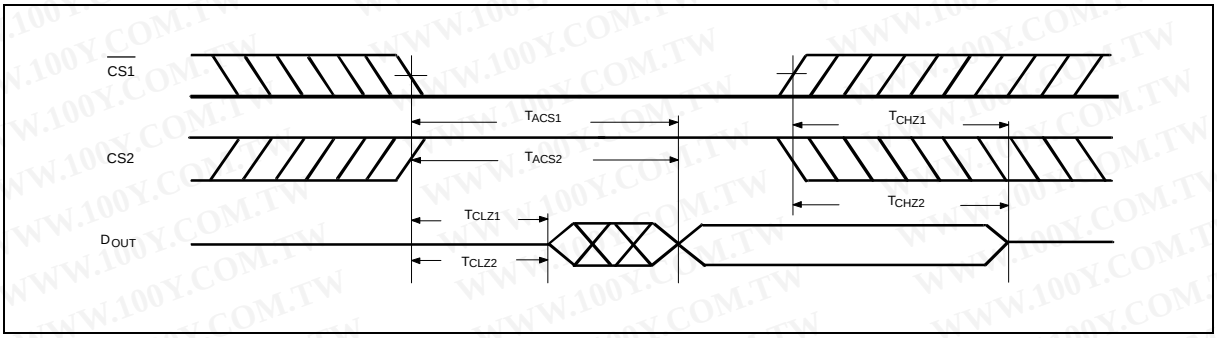
Read Cycle 1

(Address Controlled)



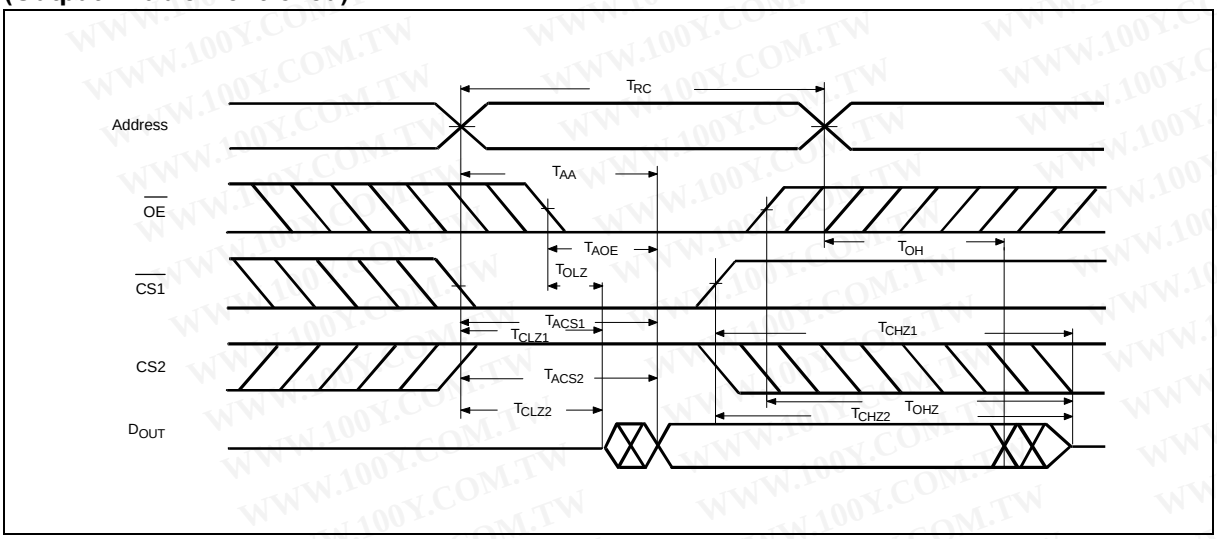
Read Cycle 2

(Chip Select Controlled)



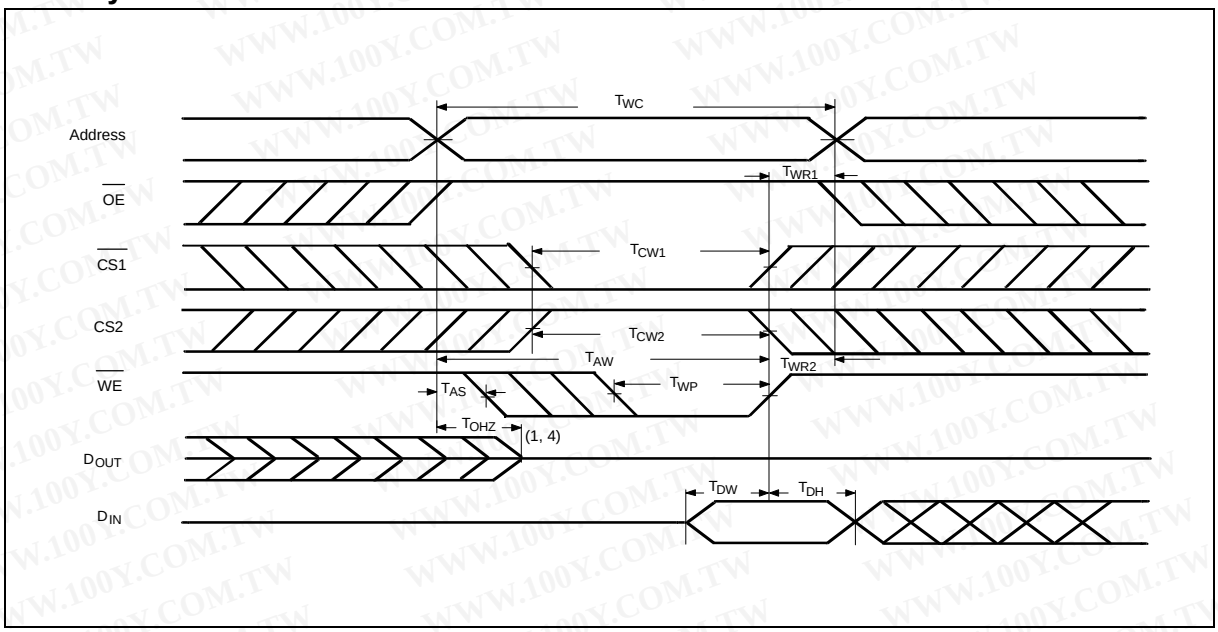
Read Cycle 3

(Output Enable Controlled)



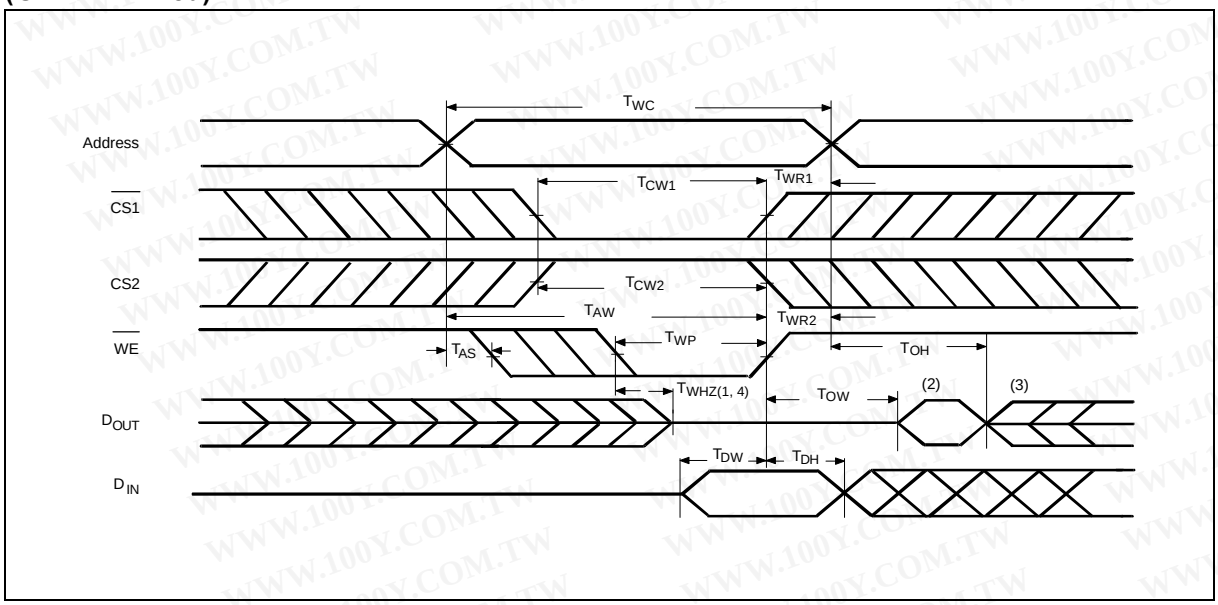
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

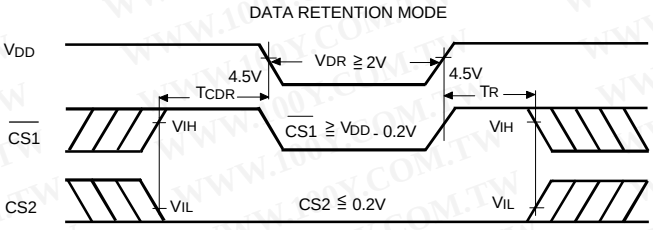
DATA RETENTION CHARACTERISTICS

(T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{DD}$ -0.2V, or CS2 ≤ 0.2V		2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS1} \geq V_{DD}$ -0.2V, or CS2 ≤ 0.2V	LL	-	-	10	µA
		V_{DD} = 3V	L	-	-	20	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention waveforms		0	-	-	nS
Operation Recovery Time	T_R			T_{RC}*	-	-	nS

T_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORMS



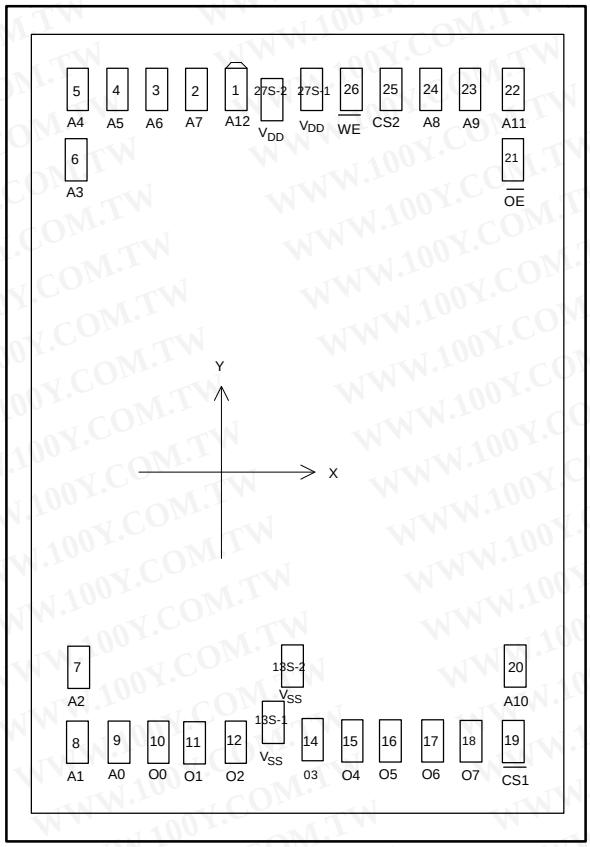
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (µA)	PACKAGE
W2465-70LL	70	70	20	600 mil DIP
W2465-10L	100	60	50	600 mil DIP
W2465S-70LL	70	70	20	330 mil SOP
W2465S-10L	100	60	50	330 mil SOP
W2465K-70LL	70	70	20	300 mil Skinny
W2465K-10L	100	60	50	300 mil Skinny

Notes:
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

Winbond Electronics Corp.

BONDING PAD DIAGRAM

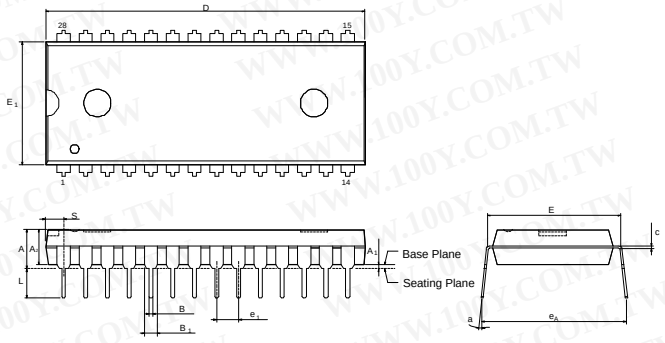


PAD NO.	X	Y
1	-226.95	1526.15
2	-350.95	1526.15
3	-484.10	1526.15
4	-608.10	1526.15
5	-739.75	1526.15
6	-741.75	1315.10
7	-741.75	-1231.85
8	-741.75	-1456.30
9	-610.60	-1456.30
10	-481.50	-1466.30
11	-343.80	-1466.30
12	-206.10	-1466.30
13S-1	-73.00	-1401.10
13S-2	-8.35	-1212.80
14	60.10	-1466.30
15	193.30	-1466.30
16	332.40	-1466.30
17	465.60	-1466.30
18	603.30	-1466.30
19	738.15	-1456.30
20	740.15	-1221.45
21	740.15	1310.80
22	738.15	1526.15
23	606.50	1526.15
24	482.50	1526.15
25	349.35	1526.15
26	225.35	1526.15
27S-1	94.20	1526.15
27S-2	-50.40	1456.10

Note: For bare chip form (C.O.B.) applications, the substrate must be connected to V_{DD} or left floating in the PCB layout.

PACKAGE DIMENSIONS

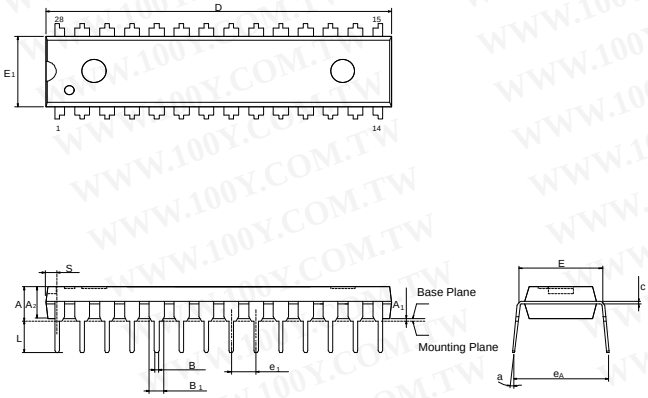
28-pin P-DIP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin P-DIP Skinny

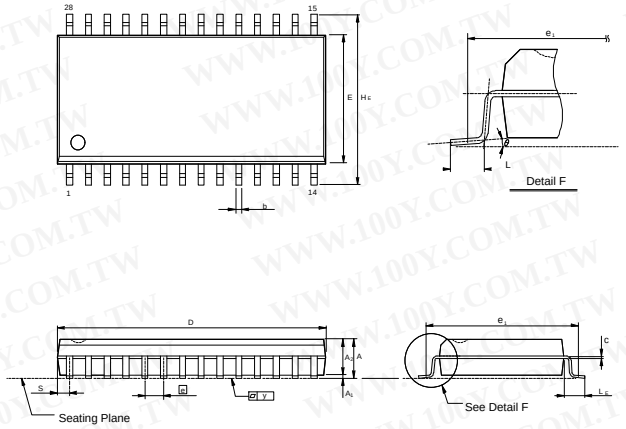


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.388	1.400	—	35.26	35.56
E	0.300	0.310	0.320	7.62	7.87	8.13
E_1	0.283	0.288	0.293	7.19	7.32	7.44
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0°	—	15°	0°	—	15°
e_A	0.330	0.350	0.370	8.38	8.89	9.40
S	—	—	0.055	—	—	1.40

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

28-pin SO Wide Body



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_E	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792647
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-7197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2730 Orchard Parkway, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668