



# MP7610

Octal 14-Bit DAC Array<sup>1M</sup>  
D/A Converter with Output Amplifier  
and Serial Data/Address  $\mu$ P Control Logic

June 1998-3

## FEATURES

- Eight Independent 14-Bit DACs with Output Amplifiers
- Low Power 320 mW (typ.)
- Serial Digital Data and Address Port (3-Wire Standard)
- 14-Bit Resolution, 12-Bit Accuracy
- Extremely Well Matched DACs
- Extremely Low Analog Ground Current (<60 $\mu$ A/Channel)
- $\pm 10$  V Output Swing with  $\pm 11.4$  V Supplies
- Zero Volt Output Preset (Data = 10 .. 00)
- Rugged Construction – Latch-Up Free
- Parallel Version: MP7611

## APPLICATIONS

- Data Acquisition Systems
- ATE
- Process Control
- Self-Diagnostic Systems
- Logic Analyzers
- Digital Storage Scopes
- PC Based Controller/DAS

## GENERAL DESCRIPTION

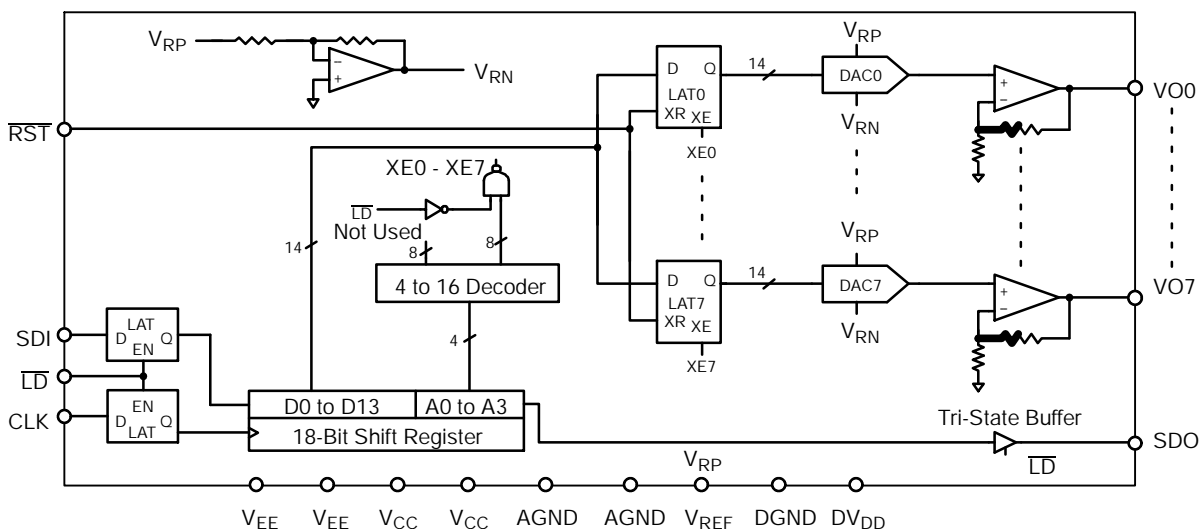
The MP7610 provides eight independent 14-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a 3-wire standard serial digital address and data port.

The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30 $\mu$ s (typ.).

The MP7610 is equipped with a serial data (3-wire standard)  $\mu$ -processor logic interface to reduce pin count, package size, and board space.

Built using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

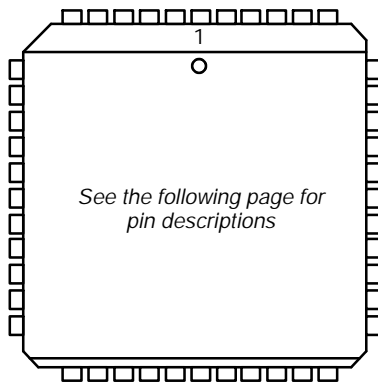
## SIMPLIFIED BLOCK DIAGRAM



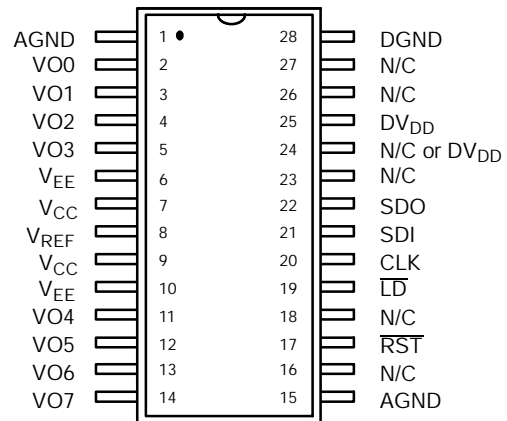
## ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PLCC	0 to +70°C	MP7610CP	14	± 2	± 2	± 16
PLCC	-40 to +85°C	MP7610BP	14	± 4	± 3	± 24
PLCC	-40 to +85°C	MP7610AP	14	± 8	± 4	± 32
SOIC	0 to +70°C	MP7610CS	14	± 4	± 3	± 24
SOIC	-40 to +85°C	MP7610BS	14	± 2	± 2	± 16
SOIC	-40 to +85°C	MP7610AS	14	± 8	± 4	± 32

## PIN CONFIGURATIONS



44 Pin PLCC



28 Pin SOIC (Jedec, 0.346")

## PIN DESCRIPTION

SOIC Pin #	PLCC Pin #	Symbol	Description
1	2	AGND	Analog Ground
2	3	VO0	DAC 0 Output
3	4	VO1	DAC 1 Output
4	5	VO2	DAC 2 Output
5	6	VO3	DAC 3 Output
6	7	V <sub>EE</sub>	Analog Negative Power Supply (-12 V)
7	9	V <sub>CC</sub>	Analog Positive Power Supply (+12 V)
8	12	V <sub>REF</sub>	Voltage Reference Input (+5 V)
9	13	V <sub>CC</sub>	Analog Positive Power Supply (+12 V)
10	15	V <sub>EE</sub>	Analog Negative Power Supply (-12 V)
11	18	VO4	DAC 4 Output
12	19	VO5	DAC 5 Output
13	20	VO6	DAC 6 Output
14	21	VO7	DAC 7 Output
15	24	AGND	Analog Ground
16		N/C	No Connection
17	26	$\overline{\text{RST}}$	Reset all DACs to 0 V Output
18		N/C	No Connection
19	29	$\overline{\text{LD}}$	Load Signal; Load Data to Selected DAC
20	31	CLK	Serial Data Clock
21	32	SDI	Serial Data Input
22	34	SDO	Shift Register Serial Output
23		N/C	No Connection
24	37	N/C	No Connection or DV <sub>DD</sub>
25	40	DV <sub>DD</sub>	Digital Positive Power Supply (+5 V)
26		N/C	No Connection
27	1, 8, 10, 11, 14, 16, 17, 22, 23, 25, 27, 28, 30, 33, 35, 36, 38, 39, 41, 42, 43	N/C	No Connection
28	44	DGND	Digital Ground

## ELECTRICAL CHARACTERISTICS

$V_{CC} = +12\text{ V}$ ,  $V_{EE} = -12\text{ V}$ ,  $V_{REF} = 5\text{ V}$ ,  $DV_{DD} = 5.0\text{ V}$ ,  $T = 25^\circ\text{C}$ , Output Load =  $5\text{ k}\Omega$  (unless otherwise noted)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
<b>STATIC PERFORMANCE</b>								
Resolution (All Grades)	N	14					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				8				
B				4				
C				2		2.5		
Differential Non-Linearity	DNL						LSB	
A				4		4		
B				3		3		
C				2		2.5		
Positive Full Scale Error	+FSE						LSB	
A			24	32		32		
B			16	24		24		
C			12	16		16		
Positive Full Scale Error Temperature Coefficient	$\Delta\text{+FSE}/\Delta\text{T}$		4				ppm/°C	0°C to 85°C
Negative Full Scale Error	-FSE						LSB	
A			24	32		32		
B			16	24		24		
C			12	16		16		
Negative Full Scale Error Temperature Coefficient	$\Delta\text{-FSE}/\Delta\text{T}$		4				ppm/°C	0°C to 85°C
Bipolar Zero Offset	ZOFS						LSB	
A				16		16		
B				12		12		
C				12		12		
Bipolar Zero Offset Temperature Coefficient	$\Delta\text{ZOFS}/\Delta\text{T}$		2				ppm/°C	0°C to 85°C
INL Matching	$\Delta\text{INL}$						LSB	
A				8		8		
B				6		6		
C				6		6		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				16		16		
B				8		8		
C				6		6		
Bipolar Zero Matching	$\Delta\text{ZOFS}$						LSB	
A				16		16		
B				12		12		
C				12		12		
Full Scale Error Matching	$\Delta\text{FSE}$						LSB	
A				16		16		
B				12		12		
C				12		12		

## ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
<b>DYNAMIC PERFORMANCE</b>								
Voltage Settling from $\overline{\text{LD}}$ to VDAC Out <sup>1</sup>	$t_{sd}$		30	50		50	$\mu\text{s}$	ZS to FS (20 V Step) 5k, 50pF load
Channel-to-Channel Crosstalk <sup>6</sup>	CT		0.04				LSB	DC
Digital Feedthrough <sup>1, 6</sup>	Q		-70				dB	CLK and Data to $V_{OUTi}$
Power Supply Rejection Ratio	PSRR			5			ppm/%	$\Delta V_{EE}$ & $\Delta V_{CC} = \pm 5\%$ , ppm of FS
<b>REFERENCE INPUTS</b>								
Impedance of $V_{REF}$	REF	350	700	1.05k	350	1.05k	$\Omega$	See Application Hints for Driving the reference input
$V_{REF}$ Voltage <sup>1, 2</sup>	$V_{REF}$	3.5		6			V	
<b>DIGITAL INPUTS<sup>3</sup></b>								
Logic High	$V_{IH}$	2.4					V	
Logic Low	$V_{IL}$			0.8			V	
Input Current	$I_L$			$\pm 10$			$\mu\text{A}$	
Input Capacitance <sup>1</sup>	$C_L$			8			pF	
<b>ANALOG OUTPUTS</b>								
Output Swing		$-V_{EE} + 1.4$	$V_{CC} - 1.4$				V	
Output Drive Current	$R_O$	-5		5			mA	
Output Impedance			1				$\Omega$	
Output Short Circuit Current	$I_{SC}$		25				mA	+FS to AGND
			30				mA	+FS to $V_{EE}$
			40				mA	-FS to AGND
			55				mA	-FS to $V_{CC}$
<b>DIGITAL OUTPUTS</b>								
Output High Voltage	$V_{OH}$		4.5				V	
Output Low Voltage	$V_{OL}$		0.5				V	
<b>POWER SUPPLIES</b>								
$V_{CC}$ Voltage <sup>5</sup>	$V_{CC}$	$V_{REF} + 1.5$	12	12.75	$V_{REF} + 1.5$	12.75	V	
$V_{EE}$ Voltage <sup>5</sup>	$V_{EE}$	-12.75	-12	-5	-12.75	-5	V	
DV <sub>DD</sub> Voltage	DV <sub>DD</sub>	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	$I_{CC}$		8	10		10	mA	Bipolar zero
Negative Supply Current	$I_{EE}$		15	20		20	mA	Bipolar zero
Digital Supply Current	$I_{DD}$			2		2	mA	Bipolar zero
Power Dissipation	PD <sub>ISS</sub>		320	420		450	mW	Bipolar zero
<b>ANALOG GROUND CURRENT</b>								
Per Channel <sup>1</sup>	$I_{AGND}$		$\pm 60$				$\mu\text{A}$	See Application Notes
<b>DIGITAL TIMING SPECIFICATIONS<sup>1,4</sup></b>								
Input Clock Pulse Width	$t_{CH}, t_{CL}$		60				ns	$V_{IL} = 0, V_{IH} = 5.0, C_L = 20 \text{ pF}$
Data Setup Time	$t_{DS}$		15				ns	
Data Hold Time	$t_{DH}$		15				ns	
CLK to SDO Propagation Delay	$t_{PD}$			40			ns	
DAC Register Load Pulse Width	$t_{LD}$		45				ns	
Preset Pulse Width	$t_{PR}$		65				ns	
Clock Edge to Load Time	$t_{CKLD1}$		140				ns	Note: $t_{LD}$ and $t_{CKLD2}$ cannot both be min. since $t_{CKLD1} = t_{CKLD2} + t_{LD}$
$\overline{\text{LD}}$ Falling Edge to SDO	$t_{CKLD2}$		0				ns	
Tri-state Enable	$t_{HZ1}$		50				ns	

## ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
<b>DIGITAL TIMING SPECIFICATIONS<sup>1, 4</sup> (CONT'D)</b>								
▮ Rising Edge to SDO Tri-state Disable	t <sub>HZ2</sub>	50					ns	
▮ Rising Edge to CLK Enable	t <sub>LDCK</sub>	50					ns	
▮ Set-up Time with Respect to CLK	t <sub>LDSU</sub>	45					ns	

### NOTES:

- <sup>1</sup> Guaranteed; not tested.
- <sup>2</sup> Specified values guarantee functionality.
- <sup>3</sup> Digital inputs should not go below digital GND or exceed DV<sub>DD</sub> supply voltage.
- <sup>4</sup> See Figures 2 and 3. All digital input signals are specified with t<sub>R</sub> = t<sub>F</sub> = 10 ns 10% to 90% and timed from a 50% voltage level.
- <sup>5</sup> For power supply values < 2V<sub>REF</sub>, the output swing is limited as specified in Analog Outputs.
- <sup>6</sup> Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)<sup>1, 2</sup>

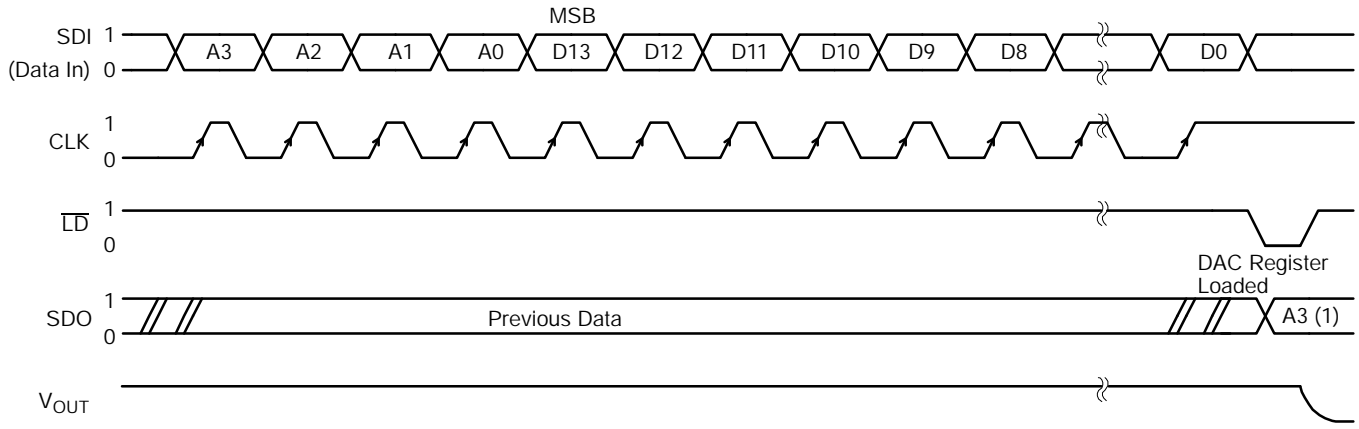
V <sub>CC</sub> to AGND	+16.5 V	Analog Inputs & Outputs	Indefinite Shorts to V <sub>CC</sub> , V <sub>EE</sub> , DV <sub>DD</sub> , AGND, DGND (provided that power dissipation of the package spec is not exceeded)
V <sub>EE</sub> to AGND	-16.5 V	Operating Temperature Range	
DV <sub>DD</sub> to DGND	+6.5 V	Extended Industrial	-40°C to +85°C
V <sub>REF</sub> to DGND	+7.0 V	Maximum Junction Temperature	-65°C to 150°C
AGND to DGND	±1 V	Storage Temperature	150°C
(Functionality guaranteed for   0.5 V only)		Lead Temperature (Soldering, 10 sec)	+300°C
Digital Input & Output Voltage		Package Power Dissipation Rating @ 75°C	
to DGND	-0.5 to DV <sub>DD</sub> +0.5V	SOIC, PLCC	1150mW
		Derates above 75°C	15mW/°C

### NOTES:

- <sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- <sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

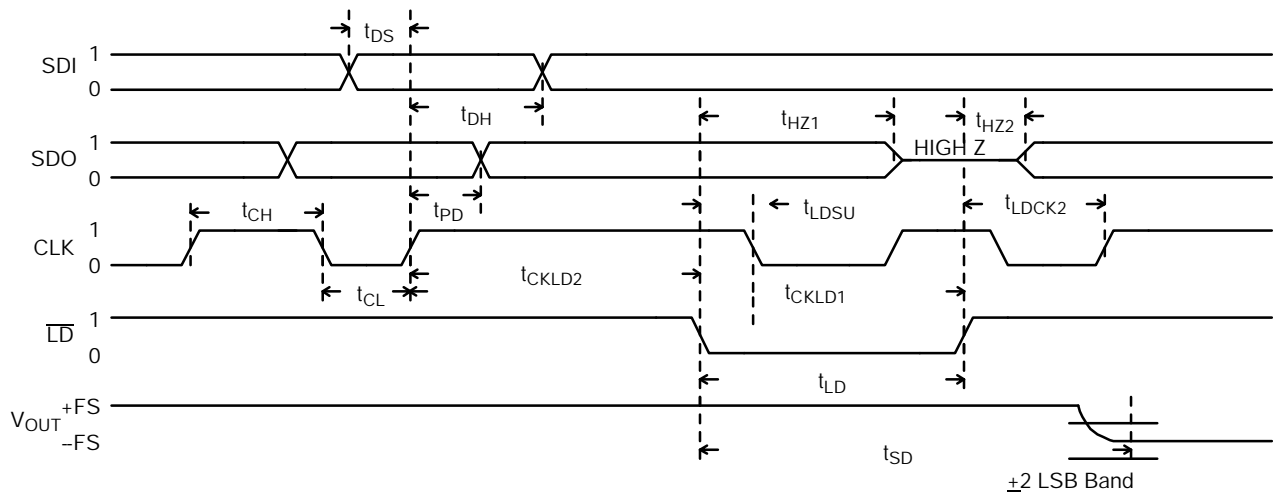
## APPLICATION NOTES

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to | 300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than | 1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.



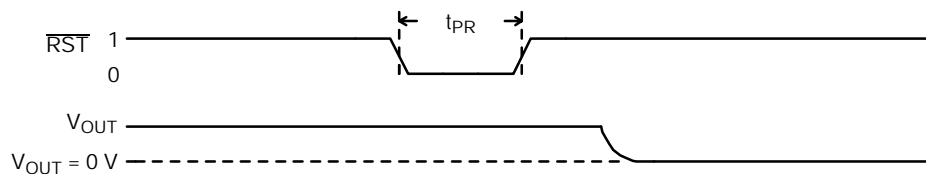
Note: (1) Because A3 is available immediately after 18th clock edge of DATA Shift-in, only 17 clock cycles are needed to complete the readback.

Figure 1. Serial Data Timing and Loading



Note: (1) CLK should be high during the falling edge of LD to insure proper function of the shift register.

Figure 2. Serial Data Input Timing (RST = "1")



Note: Reset settling time is  $\leq t_{SD}$

Figure 3. Reset Operation

The MP7610 is equipped with a serial data (3-wire standard)  $\mu$ -processor logic interface to reduce pin count, package size, and board wire (space). If the  $\overline{LD}$  signal is high, the CLK signal loads the digital input bits (SDI) into the shift register (4 bits address A3 to A0 plus 14 bits data D13 to D0 for the MP7610). The  $\overline{LD}$  signal going low loads the data into the selected DAC. The

$\overline{LD}$  signal going low also disables the serial data (SDI), output (SDO tri-stated) and the CLK input. This design tremendously reduces digital noise and glitch transients into the DACs due to free running CLK and SDI. Note also that the preset signal ( $\overline{RST}$ ) resets all analog outputs to 0 volt regardless of digital inputs.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	RST	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	1	1	1	0	No Operation	X	1	X	Hi-Z
⋮	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to 0 V	X	X	X	X	X	X	0	X	X

**Table 1. Digital Function Truth Table Serial In/Serial Out**

*Note: For timing information See Electrical Characteristics.*

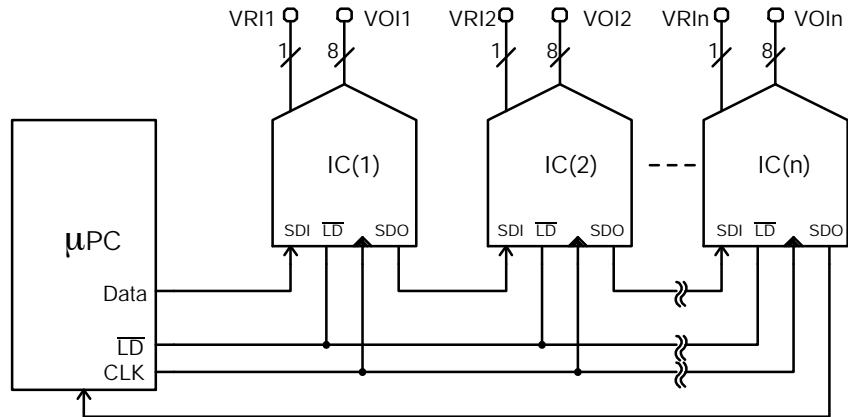
Hex Code	Binary Code	Output Voltage = $2 \cdot V_r \left(-1 + \frac{2 \cdot D}{16384}\right)$ ( $V_r = +5\text{ V}$ )
0 0 0 0	00000000000000	$10 \cdot (-1 + 0) = -10$
⋮	⋮	⋮
1 F F F	01111111111111	$10 \cdot \left(-1 + \frac{16382}{16384}\right) = -1.22\text{ mV}$
2 0 0 0	10000000000000	$10 \cdot \left(-1 + \frac{16384}{16384}\right) = 0$
2 0 0 1	10000000000001	$10 \cdot \left(-1 + \frac{16386}{16384}\right) = 1.22\text{ mV}$
⋮	⋮	⋮
3 F F F	11111111111111	$10 \cdot \left(-1 + \frac{32766}{16384}\right) = 9.99878$

**Table 2. MP7610 Ideal DAC Output vs. Input Code**

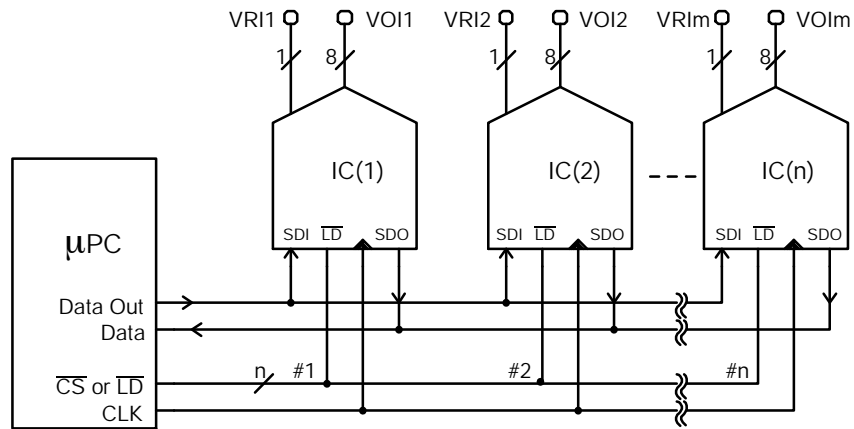
*Note: See Electrical Characteristics for real system accuracy*



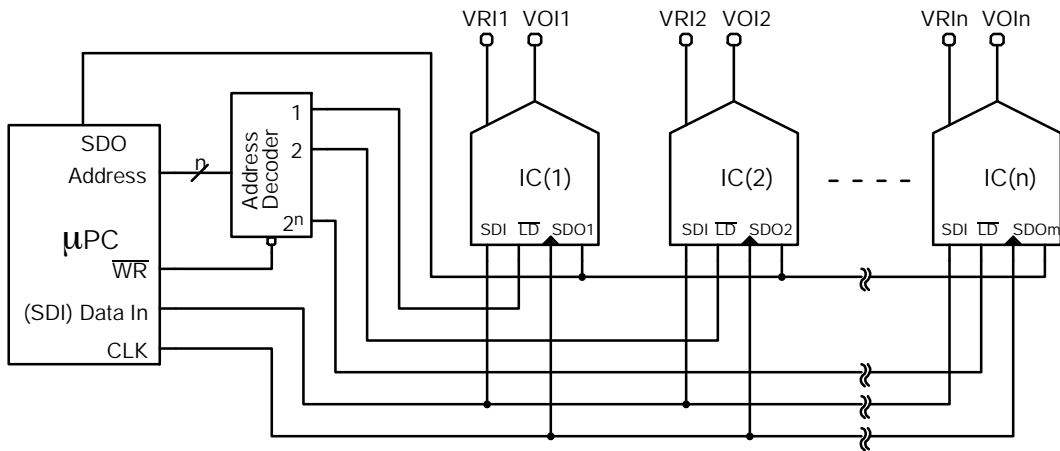
**SERIAL INTERFACE DIAGRAMS**



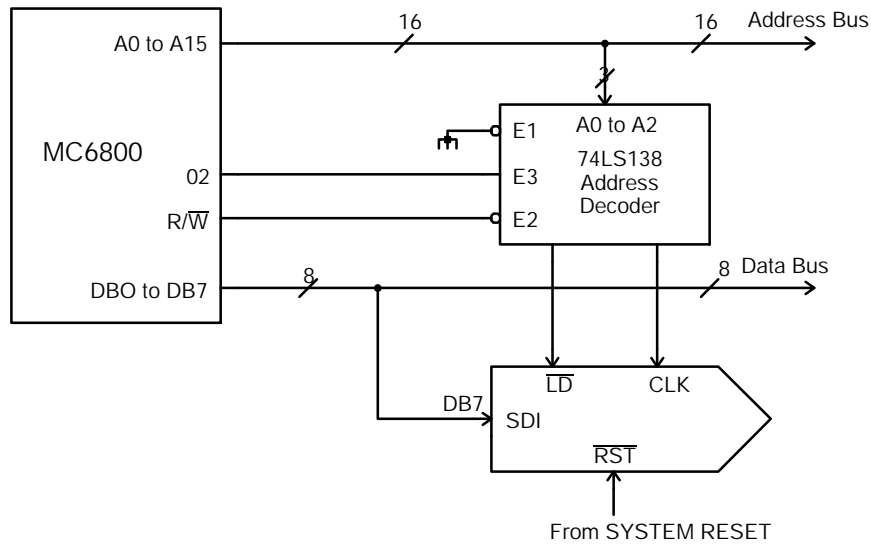
**Figure 4. Simplified Diagram**



**Figure 5. Simplified Diagram**



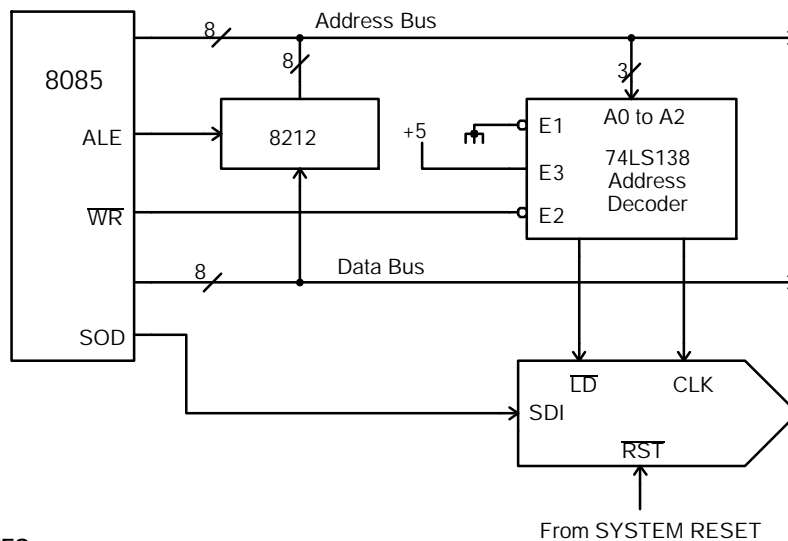
**Figure 6. Simplified Diagram**



**NOTES**

1. Execute consecutive memory write instructions while manipulating the data between WRITES so that each WRITE presents the next bit.
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE to memory location 2000, R/W, and 02. A WRITE to address 4000 transfers data from input shift register to DAC register.

**Figure 7. MC6800 Interface**



**NOTES:**

1. Clock generated by  $\overline{WR}$  and decoding address 8000.
2. Data is clocked in the DAC shift register by executing memory write instructions. The clock input is generated by decoding address 8000 and  $\overline{WR}$ . Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

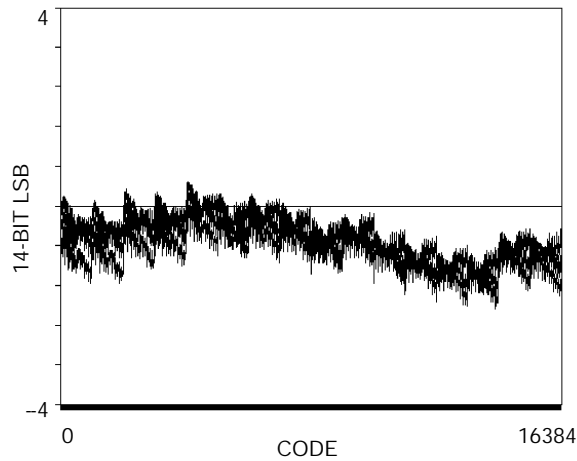
**Figure 8. 8085 Interface**

**PERFORMANCE CHARACTERISTICS**

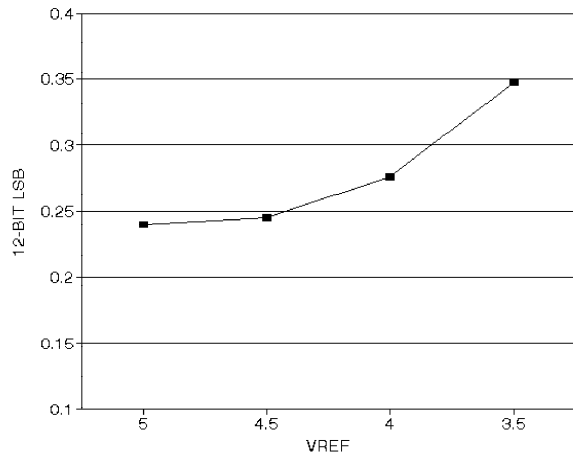


**Graph 1. Typical Output Settling Characteristic**  
 $V_{REF} = 5 \text{ V}, R_L = 5 \text{ K}, C_L = 500 \text{ pF}$

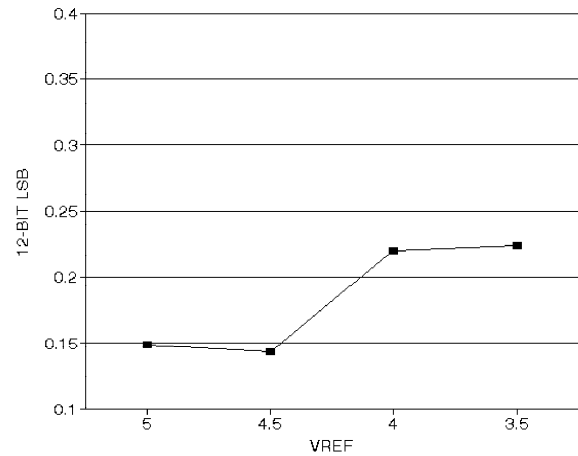
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET ! ZS! FS! ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



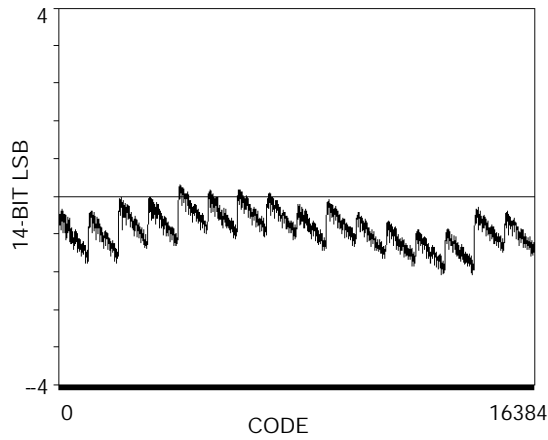
**Graph 2. Linearity with**  
 $V_{REF} = 5 \text{ V}, \text{ All DACs, All Codes}$



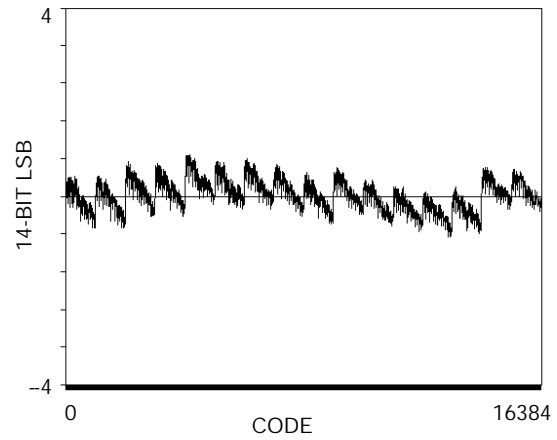
**Graph 3. DAC 0 INL vs. VREF**



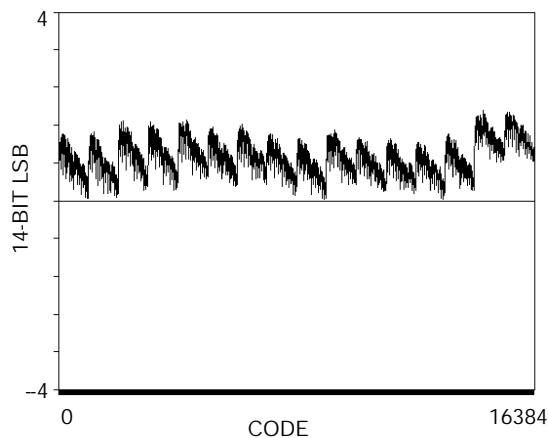
**Graph 4. DAC 0 DNL vs. VREF**



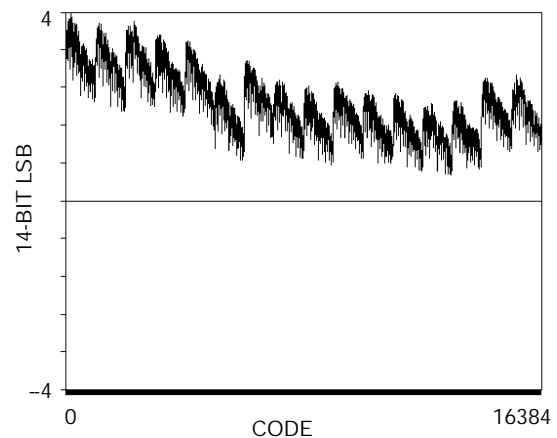
**Graph 5. DAC 0 Linearity with VREF = 5 V, VOUT = 10**



**Graph 6. DAC 0 Linearity with VREF = 4.5 V, VOUT = 9**



**Graph 7. DAC 0 Linearity with VREF = 4 V, VOUT = 8**



**Graph 8. DAC 0 Linearity with VREF = 3.5 V, VOUT = 7**

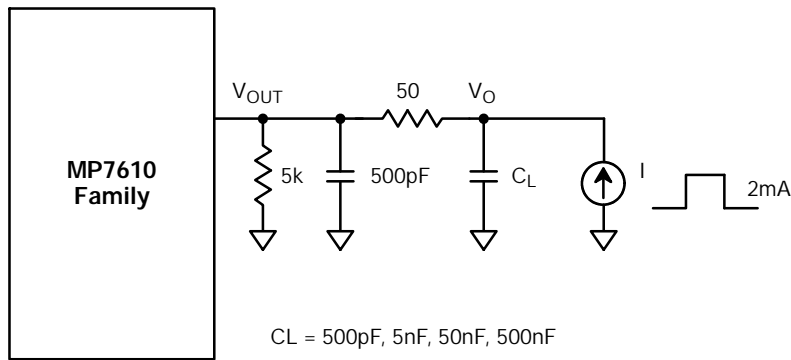
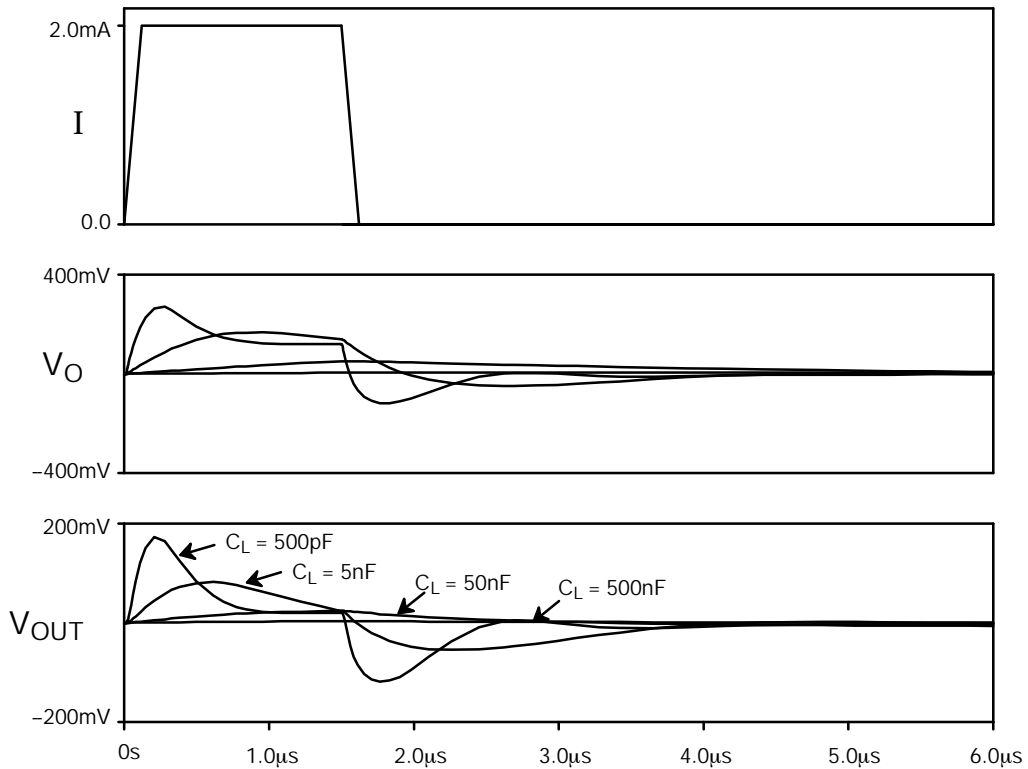


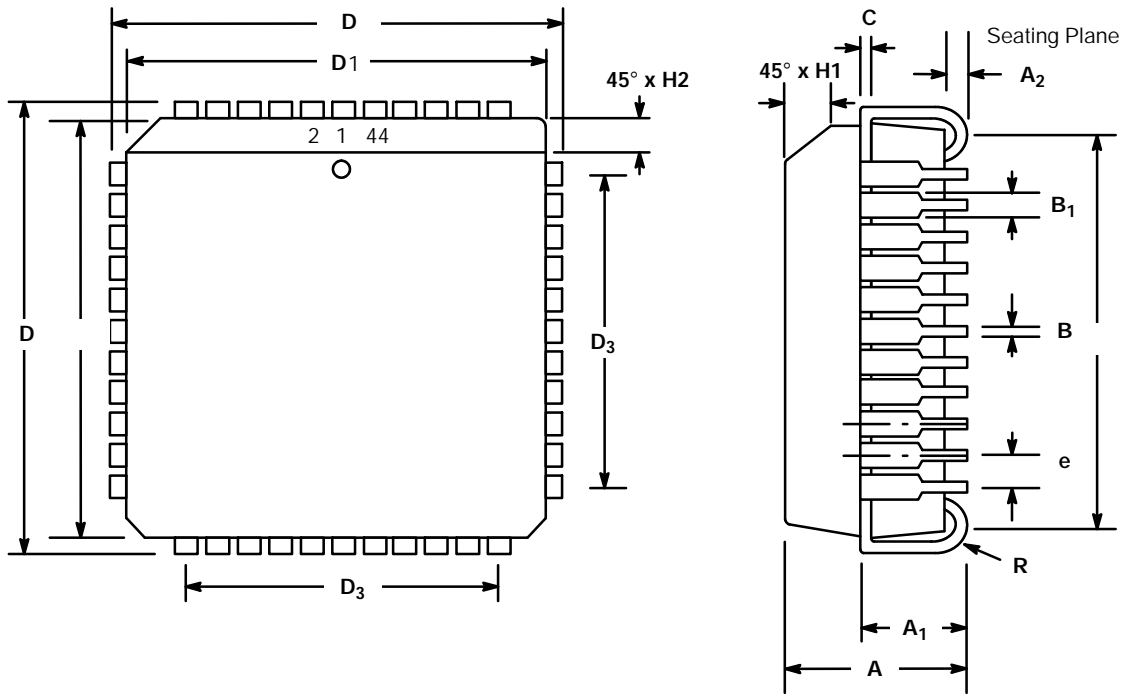
Figure 9. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with  $C_L=500\text{pF}, 5\text{nF}, 50\text{nF}, 500\text{nF}$   
(See Figure 9. above)

## 44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00

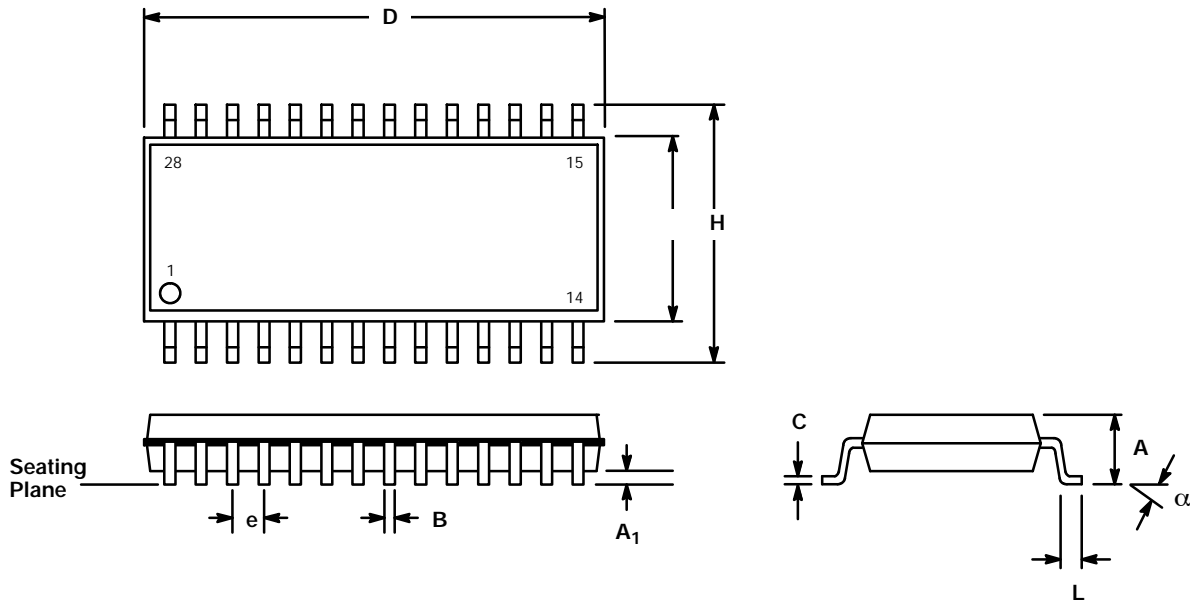


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A <sub>1</sub>	0.090	0.120	2.29	3.05
A <sub>2</sub>	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B <sub>1</sub>	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D <sub>1</sub>	0.650	0.656	16.51	16.66
D <sub>2</sub>	0.590	0.630	14.99	16.00
D <sub>3</sub>	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

**28 LEAD SMALL OUTLINE  
(350 MIL JEDEC SOIC)**

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A <sub>1</sub>	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.706	0.718	17.93	18.24
E	0.340	0.350	8.64	8.89
e	0.050 BSC		1.27 BSC	
H	0.460	0.485	11.68	12.32
L	0.016	0.050	0.40	1.27
$\alpha$	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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