The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Bipolar Memory Data Manual

SEPTEMBER 1977

TEXAS INSTRUMENTS
INCORPORATED

SCHOTTKY† PROMS

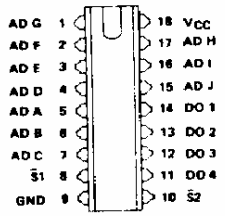
SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

- Titanium-Tungsten (Ti-W) Fuse Links for Fast Low-Voltage Reliable Programming
- Full Decoding and Chip Select Simplify System Design
- Power-Down Versions ('S450, 'S451) Can Reduce System Power Requirements
- Fast Chip Select to Simplify System Decode
- Choice of Three-State or Open Collector Outputs
- PNP Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE		
				ACCESS TIME		POWER
–55°C to 125°C	0°C to 70°C			ADDRESS	SELECT	DISSIPATION
SN54S450(J)	SN74S450(J,N)	8192 bits	three-state	45 ns	20 ns	600/100† mW
SN54S451(J)	SN74S451(J,N)	1024 W x 8 B	open-collector			
SN54S478(J)	SN74S478(J,N)	8192 bits	three-state	45 ns	20 ns	600 mW
SN54S479(J)	SN74S479(J,N)	1024 W x 8 B	open-collector			
SN54S2708(J)	SN74S2708(J,N)	8192 bits	three-state	45 ns	20 ns	600 mW
SN54S3708(J)	SN74S3708(J,N)	1024 W x 8 B	open-collector			
SN54S476(J)	SN74S476(J,N)	4096 bits	three-state	35 ns	15 ns	475 mW
SN54S477(J)	SN74S477(J,N)	1024 W x 4 B	open-collector			

†Power down

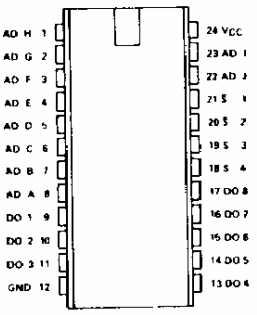
SN54S/74S476 3-S OUTPUTS
SN54S/74S477 0-C OUTPUTS
4096 BITS
(1024 WORDS BY 4 BITS)
'S476, 'S477



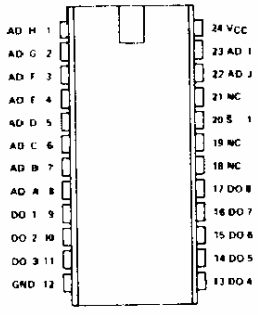
MAXIMUM DELAY TIMES

TYPE	ADDRESS	EN	DISABLE
SN54S'	75 ns	40 ns	40 ns
SN74S'	60 ns	30 ns	30 ns

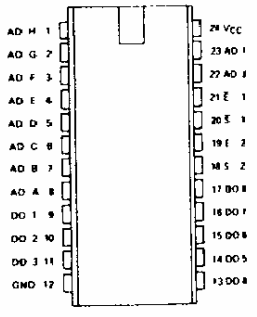
SN54S/74S478 3-S OUTPUTS
SN54S/74S479 0-C OUTPUTS
8192 BITS
(1024 WORDS BY 8 BITS)
'S478, 'S479



SN54S/74S2708 3-S OUTPUTS
SN54S/74S3708 0-C OUTPUTS
8192 BITS
(1024 WORDS BY 8 BITS)
'S2708, 'S3708



SN54S/74S450 3-S OUTPUTS
SN54S/74S451 0-C OUTPUTS
8192 BITS
(1024 WORDS BY 8 BITS)
'S450, 'S451



description

These monolithic TTL programmable read-only memories (PROM's) features titanium-tungsten (Ti-W) fuse links with each link designed to program with a 100 microsecond pulse. They offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, and choice of bus-driving three-state or open-collector outputs. Additionally, the 'S450, 'S451 features dual enable/disable inputs which power-down or power-up the PROM providing additional cost effectiveness in power-sensitive applications. The power-down and power-up functions are sequenced to occur with the outputs at a high impedance.

Data can be electrically programmed, as desired, at any bit location in accordance with the programming procedure specified. These new PROM's are supplied with a high logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U. S. Patent Number 3,463,975.

ıcedure is irreversible. Once altered, the output for that bit location is permanently programmed. Outputs never ıing been altered may later be programmed to supply the opposite output level. Operation of the unit within the ommended operating conditions will not alter the memory content. Active level(s) at the chip-select(s) or memory ıble (E) input(s) activates all of the outputs, and the 'S450, 'S451 memory enable will initiate a power-up sequence. inactive level at any chip-select or memory enable input causes all outputs to be off, and the memory enable will ıiate a power-down sequence. The three-state output offers the convenience of an open-collector output with the ıed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time ıracteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a a line having a passive pull-up.

te maximum ratings over operating free-air temperature range (unless otherwise noted)

upply voltage . . . . . 7 V
ıput voltage . . . . . 5.5 V
ff-state output voltage . . . . . 5.5 V
ıperating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
torage temperature range . . . . . −65°C to 150°C

mended conditions for programming

PARAMETER		'S450, 'S451			ALL OTHER TYPES			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
voltage, V_{CC} (See Note 1)	Steady state	5.8	6	6.25	4.75	5	5.25	V
	During programming	6.8	7	7.25	5.75	6	6.25	
s input voltage	High level, V_{IH}	2.4		5	2.4		5	V
	Low level, V_{IL}	0.0		0.5	0.0		0.5	
nput voltage, V_S	to disable	9.75	10	10.25†	9.75	10	10.25†	V
	to enable	0.0		0.5	0.0		0.5	
ation of all outputs except the one to be programmed		0.0		0.5	0.0		0.5	V
e applied to output to be programmed, $V_{O(pr)}$ (See Note 2)		16.75	17	17.25†	16.75	17	17.25†	V
mming ramp (10% to 90% times	Rise time, t_r	10‡		50	10‡		50	µs
C, VS, and $V_{O(pr)}$	Fall time, t_f	10			10			
on of $V_{O(pr)}$ programming pulse (See Figure 3)		98	100	10³	98	100	10³	µs
mming duty cycle			25	35		25	35	%
r temperature		0		55	0		55	°C

†Absolute maximum ratings.

‡This minimum rise time applies only for the $V_{O(pr)}$ ramp.

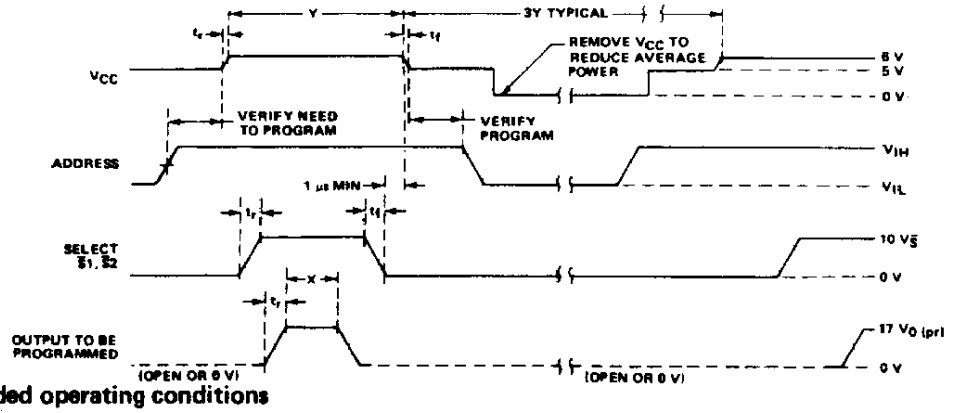
NOTES: 1. Voltage values are with respect to network ground terminal.
2. All bit locations contain a high logic level and programming a bit changes the output of the bit to low logic level.
3. Programming is guaranteed if the pulse applied is 98 µs in duration.

y-step programming procedure

. Apply steady-state supply voltage and address the word to be programmed.
. Enable the PROM and verify that the bit location needs to be programmed. If not, proceed to the next bit.
. If the bit requires programming, increase V_{CC} by 1 volt (minimum current capability should be 200 mA) and disable the outputs by applying 10 volts to chip-select inputs. Minimum chip-select input current capabilities should be 5 mA.
. Only one bit location is programmed at a time. Connect each output not being programmed to a 0 to 0.5 volt source. Apply the $V_{O(pr)}$ voltage pulse specified in the table to the output to be programmed. Minimum current capability of the programming output supply (during programming) should be 200 mA. See programming sequence of Figure 1.
. After the X pulse is completed, disconnect the output that was programmed. Then, remove the 0 to 0.5 volt source from the remaining outputs.

6. The chip-select inputs may be taken to a low logic level (to permit program verification).
7. One microsecond after the chip select input(s) reach low logic level V_{CC} should be decreased 1 V at which verification can be accomplished by measuring V_{OL} at the programmed output.
8. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 7 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.



recommended operating conditions

PARAMETER		'54S0			'54S1			'54S78, '52708			'54S79, '53708			'54S76			'54S77			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	SN54S	5.8	6	6.5	5.8	6	6.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	SN74S	5.8	6	6.25	5.8	6	6.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	SN54S			−2						−2						−2				mA
	SN74S			−3.2						−3.2						−3.2				
Low-level output current, I_{OL}				12			12			12			12			16			16	mA
Operating free-air temperature, T_A	SN54S	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	SN74S	0		70	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'54S0, '54S76, '54S78, '52708			'54S1, '54S77 '54S79, '53708			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4					V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}, I_{OH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.4 V			50			50	μA
			V_O = 5.5 V						100	
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54S'	−20		−100				mA
			SN74S'	−15		−100				
I_{CC}	Supply current	V_{CC} = MAX	4096-BIT PROM		95	140		95	140	mA
			8192-BIT PROM		120			120		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

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SERIES 54/74, 54S/74S READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512259, MAY 1975

- **Mask-Programmed Memories That Can Replace PROMs**
- **Full On-Chip Decoding and Fast Chip Select(s) Simplify System Decoding**
- **All Schottky-Clamped ROMs Offer**
  - **–Choice of 3-State or Open-Collector Outputs**
  - **–P-N-P Inputs for Reduced Loading on System Buffers/Drivers**
- **Applications Include:**
  - **–Microprogramming Firmware/Firmware Loaders**
  - **–Code Converters/Character Generators**
  - **–Translators/Emulators**
  - **–Address Mapping/Look-Up Tables**

YPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES	
55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATION)	CHIP-SELECT	ADDRESS
5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	22 ns	26 ns
54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	20 ns	40 ns
54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	15 ns	45 ns
54S370(J)	SN74S370(J, N)	3-State			
54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	15 ns	45 ns
54S371(J)	SN74S371(J, N)	3-State			

scription

These monolithic TTL custom-programmed read-only memories (ROMs) are particularly attractive for applications requiring medium to large quantities of the same bit pattern. Plug-in replacements can be obtained for most of the popular TTL PROMs.

The high-complexity 2048-bit ROMs can be used to significantly improve system bit density for fixed memory as all are offered in compact 16- or 20-pin dual-in-line packages having pin-row spacings of 0.300-inch.

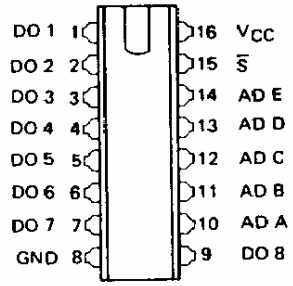
The Schottky-clamped versions offer considerable flexibility for upgrading existing designs or improving new designs as they feature improved performance; plus, they offer low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

Data from a sequenced deck of data cards punched according to the specified format are permanently programmed by the factory into the monolithic structure for all bit locations. Upon receipt of the order, Texas Instruments will assign a special identifying number for each pattern programmed according to the order. The completed devices will be marked with the appropriate TI special device number. It is important that the customer specify not only the output levels desired at all bit locations, but also the other information requested under ordering instructions.

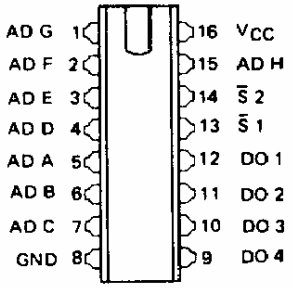
The three-state outputs offer the convenience of an open-collector output with the speed of a totem-pole output: they can be bus-connected to other similar outputs yet they retain the fast rise time characteristic of the TTL totem-pole output. The open-collector outputs offer the capability of direct interface with a data line having a passive pull-up.

Word-addressing is accomplished in straight positive-logic binary and the memory may be read when all $\overline{S}$ inputs are low. A high at any $\overline{S}$ input causes the outputs to be off.

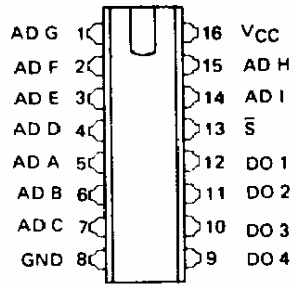
256 BITS (32 WORDS BY 8 BITS)
'88A



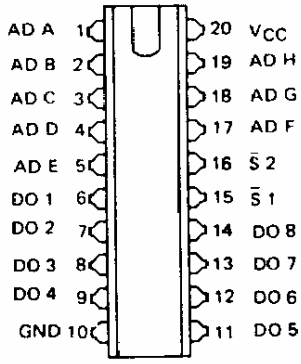
1024 BITS (256 WORDS BY 4 BITS)
'187



2048 BITS (512 WORDS BY 4 BITS)
'S270, 'S370



2048 BITS (256 WORDS BY 8 BITS)
'S271, 'S371



Pin assignments for all of these memories are the same for all packages.

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