

Document Title

256Kx16 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	July 29, 2002	Preliminary
0.1	Revised - Added Commercial product - Deleted 44-TSOP2-400R Package Type. - Added 55ns product(@ 3.0V~3.6V)	December 2, 2002	Preliminary
1.0	Finalized Revised - Changed Icc(Operating power supply current) from 4mA to 2mA - Changed Icc1(Average operating current) from 4mA to 3mA - Changed Icc2(Average operating current) from 40mA to 25mA - Changed Isb1(Standby Current(CMOS), Commercial) from 15μA to 10μA - Changed Isb1(Standby Current(CMOS), Industrial) from 20μA to 10μA - Changed Isb1(Standby Current(CMOS), Automotive) from 30μA to 20μA - Changed Idr(Data retention current, Commercial) from 15μA to 10μA - Changed Idr(Data retention current, Industrial) from 20μA to 10μA - Changed Idr(Data retention current, Automotive) from 30μA to 20μA	August 8, 2003	Final

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## 256Kx16 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 256K x16
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 44-TSOP2-400F

### GENERAL DESCRIPTION

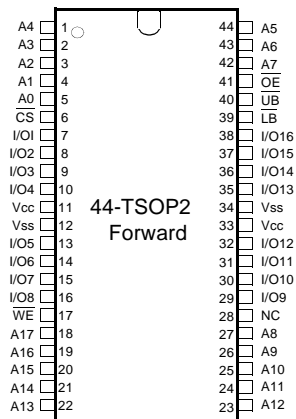
The K6X4016T3F families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature range and have 44-TSOP2 package type for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
K6X4016T3F-B	Commercial(0~70°C)	2.7~3.6V	55 <sup>1)</sup> /70 <sup>2)</sup> /85ns	10μA	25mA	44-TSOP2-400F
K6X4016T3F-F	Industrial(-40~85°C)			10μA		
K6X4016T3F-Q	Automotive(-40~125°C)		20μA			

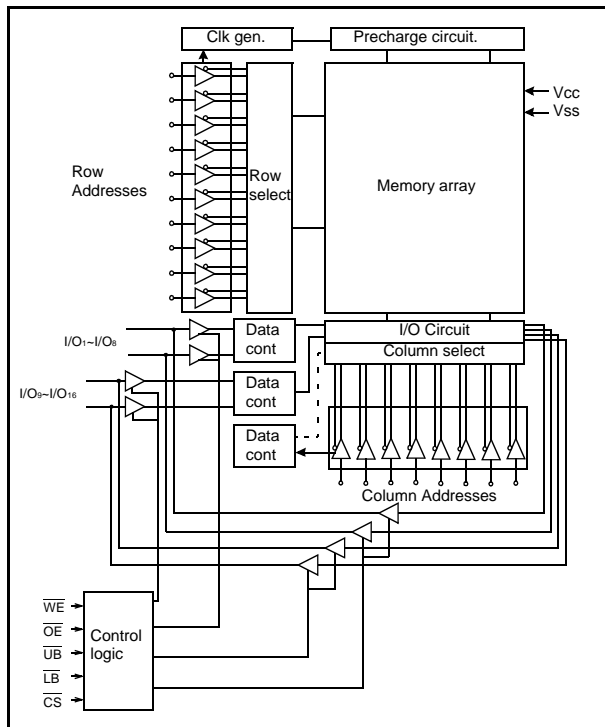
1. This parameter is measured with 30pF test load (Vcc=3.0~3.6V).
2. The parameter is measured with 30pF test load.

### PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{LB}$	Lower Byte (I/O1-8)
A0~A17	Address Inputs	$\overline{UB}$	Upper Byte (I/O9-16)
I/O1~I/O16	Data Input/Output	NC	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6X4016T3F-TB55 <sup>1)</sup> K6X4016T3F-TB70 K6X4016T3F-TB85	44-TSOP2-F, 55ns, LL 44-TSOP2-F, 70ns, LL 44-TSOP2-F, 85ns, LL	K6X4016T3F-TF55 <sup>1)</sup> K6X4016T3F-TF70 K6X4016T3F-TF85	44-TSOP2-F, 55ns, LL 44-TSOP2-F, 70ns, LL 44-TSOP2-F, 85ns, LL	K6X4016T3F-TQ70 K6X4016T3F-TQ85	44-TSOP2-F, 70ns, L 44-TSOP2-F, 85ns, L

1. Operating voltage range is 3.0~3.6V

## FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O <sub>1-8</sub>	I/O <sub>9-16</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
L	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
L	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X <sup>1)</sup>	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X <sup>1)</sup>	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X <sup>1)</sup>	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to V <sub>CC</sub> +0.3(max. 3.9V)	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.2 to 3.9	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6X4016T3F-B
		-40 to 85		K6X4016T3F-F
		-40 to 125		K6X4016T3F-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0/3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.2 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.6	V

Note:

- Commercial Product: T<sub>A</sub>=0 to 70°C, otherwise specified.  
Industrial Product: T<sub>A</sub>=-40 to 85°C, otherwise specified.  
Automotive Product: T<sub>A</sub>=-40 to 125°C, otherwise specified.
- Overshoot: V<sub>CC</sub>+2.0V in case of pulse width ≤ 30ns.
- Undershoot: -2.0V in case of pulse width ≤ 30ns.
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

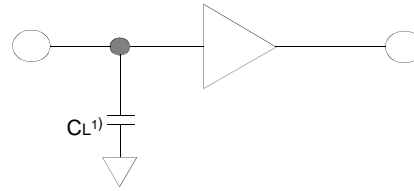
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IL</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read	-	-	2	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA $\overline{CS} \leq 0.2V$ , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	3	mA	
	I <sub>CC2</sub>	Cycle time=Min <sup>2)</sup> , 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	25	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}=V_{IH}$ , Other inputs=V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.3	mA	
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC}-0.2V$ , Other inputs=0-V <sub>CC</sub>	K6X4016T3F-B	-	-	10	μA
			K6X4016T3F-F	-	-	10	μA
			K6X4016T3F-Q	-	-	20	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load(see right):  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS

(  $V_{CC}=2.7\sim 3.6\text{V}$ , Commercial product:  $T_A=0$  to  $70^\circ\text{C}$ , Industrial product:  $T_A=-40$  to  $85^\circ\text{C}$ , Automotive product:  $T_A=-40$  to  $125^\circ\text{C}$  )

Parameter List		Symbol	Speed Bins						Units
			55ns <sup>1)</sup>		70ns		85ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	85	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	-	85	ns
	Chip select to output	t <sub>CO</sub>	-	55	-	70	-	85	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	-	40	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ valid to data output	t <sub>BA</sub>	-	25	-	35	-	40	ns
	Chip select to low-Z output	t <sub>lZ</sub>	10	-	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ enable to low-Z output	t <sub>BLZ</sub>	5	-	5	-	5	-	ns
	Output hold from address change	t <sub>OH</sub>	10	-	10	-	10	-	ns
	Chip disable to high-Z output	t <sub>hZ</sub>	0	20	0	25	0	25	ns
	$\overline{\text{OE}}$ disable to high-Z output	t <sub>OHZ</sub>	0	20	0	25	0	25	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ disable to high-Z output	t <sub>BHZ</sub>	0	20	0	25	0	25	ns
Write	Write cycle time	t <sub>WC</sub>	55	-	70	-	85	-	ns
	Chip select to end of write	t <sub>CW</sub>	45	-	60	-	70	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	70	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	55	-	60	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	25	0	25	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	35	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	5	-	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ valid to end of write	t <sub>BW</sub>	45	-	60	-	70	-	ns

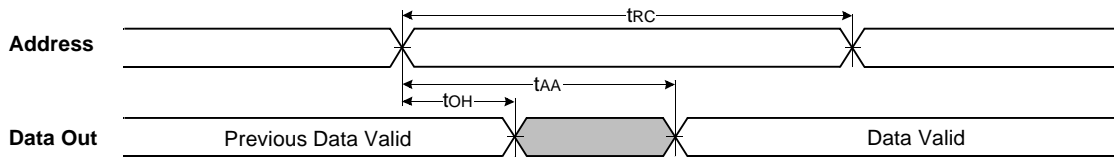
1. Voltage range is 3.0V~3.6V for commercial and industrial product.

## DATA RETENTION CHARACTERISTICS

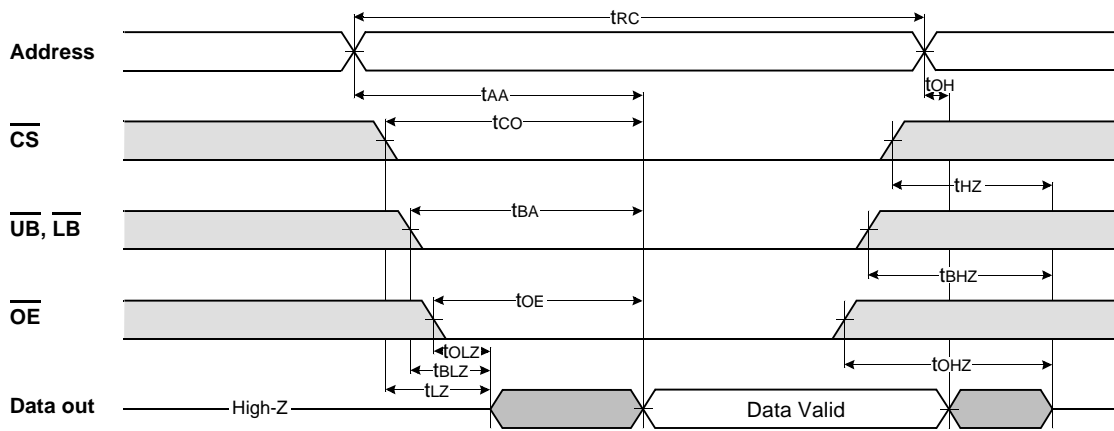
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0\text{V}$ , $\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	-	-	10	$\mu\text{A}$
					10	$\mu\text{A}$
					20	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )

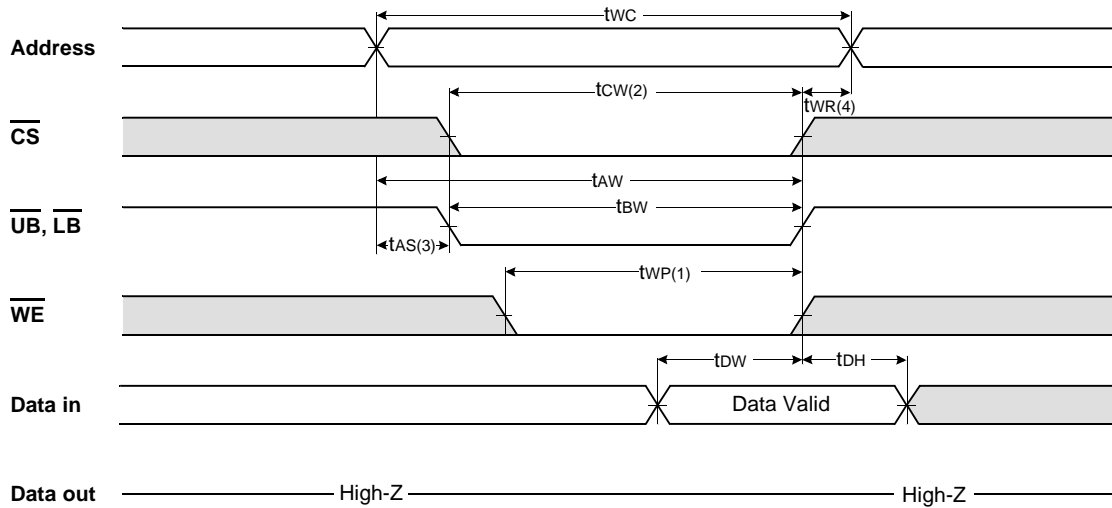


NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.



TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

DATA RETENTION WAVE FORM

$\overline{CS}$  controlled

