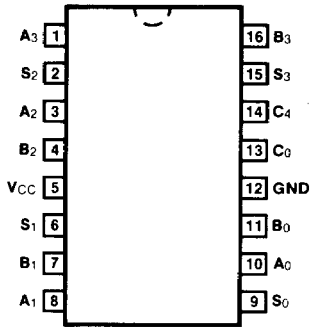
54/7483A
54LS/74LS83A

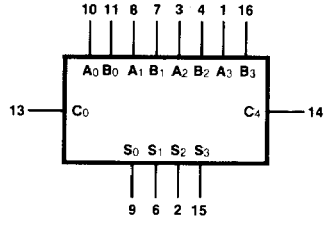
4-BIT BINARY FULL ADDER
(With Fast Carry)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '83A high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words ($A_0 - A_3$, $B_0 - B_3$) and a Carry input (C_0). They generate the binary Sum outputs ($S_0 - S_3$) and the Carry output (C_4) from the most significant bit. They operate with either HIGH or active LOW operands (positive or negative logic). The '283 is recommended for new designs since it features standard corner power pins.

LOGIC SYMBOL



VCC = Pin 5
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7483APC, 74LS83APC		9B
Ceramic DIP (D)	A	7483ADC, 74LS83ADC	5483ADM, 54LS83ADM	6B
Flatpak (F)	A	7483AFC, 74LS83AFC	5483AFM, 54LS83AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	A Operand Inputs	1.0/1.0	1.0/0.5
$B_0 - B_3$	B Operand Inputs	1.0/1.0	1.0/0.5
C_0	Carry Input	1.0/1.0	0.5/0.25
$S_0 - S_3$	Sum Outputs	20/10	10/5.0 (2.5)
C_4	Carry Output	10/5.0	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '83A adds two 4-bit binary words (A and B) plus the incoming carry. The binary sum appears on the sum outputs (S_0 — S_3) and outgoing carry (C_4) outputs.

$$C_0 + (A_0 + B_0) + 2(A_1 + B_1) + 4(A_2 + B_2) + 8(A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the '83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

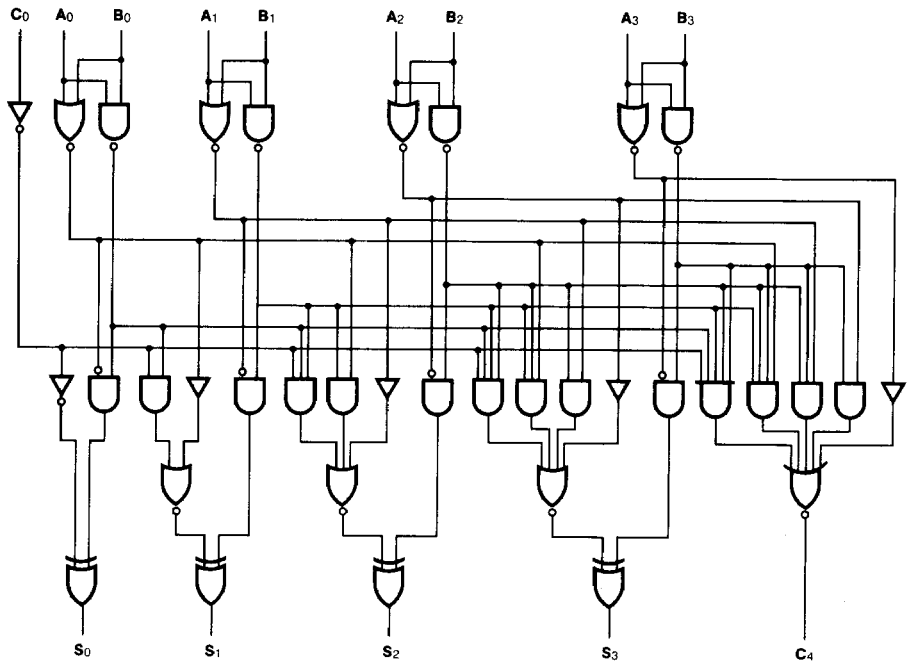
Interchanging inputs of equal weight does not affect the operation, thus C_0, A_0, B_0 can be arbitrarily assigned to pins 10, 11, 13, etc.

TRUTH TABLE

	INPUTS									OUTPUTS					
	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10 + 9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry + 5 + 6 = 12)

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current at S_n	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-20	-100		
I_{OS}	Output Short Circuit Current at C_4	XM	-20	-70	-20	-100	mA	V_{CC} = Max
		XC	-18	-70	-20	-100		
I_{CC}	Power Supply Current	XM		99		39	mA	V_{CC} = Max, Inputs = Gnd ('LS83A) Inputs = 4.5 V ('83A)
		XC		110		39		

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay C_0 to S_n		21		24	ns	Figs. 3-1, 3-20
t_{PHL}			21		24		
t_{PLH}	Propagation Delay A_n or B_n to S_n		24		24	ns	Figs. 3-1, 3-20
t_{PHL}			24		24		
t_{PLH}	Propagation Delay C_0 to C_4		14		17	ns	Figs. 3-1, 3-5 R_L = 780 Ω ('83A)
t_{PHL}			16		17		
t_{PLH}	Propagation Delay A_n or B_n to C_4		14		17	ns	Figs. 3-1, 3-5 R_L = 780 Ω ('83A)
t_{PHL}			16		17		