SpeedPlus™ Dual, 700MHz, Voltage-Feedback OPERATIONAL AMPLIFIER

FEATURES

- **WIDEBAND BUFFER: 700MHz, G = +1**
- **WIDEBAND LINE DRIVER: 200MHz, G = +2**
- **HIGH OUTPUT CURRENT: 140mA**
- **LOW SUPPLY CURRENT: 5.5mA/Ch**
- **ULTRA-SMALL PACKAGE: SOT23-8**
- **LOW dG/dϕ: 0.05%/0.03°**
- **HIGH SLEW RATE: 335V/μsec**
- **SUPPLY VOLTAGE: ±3V to ±6V**

APPLICATIONS

- **A/D DRIVERS**
- **CONSUMER VIDEO**
- **ACTIVE FILTERS**
- **PULSE DELAY CIRCUITS**
- **LOW COST UPGRADE TO THE AD8056 OR EL2210**

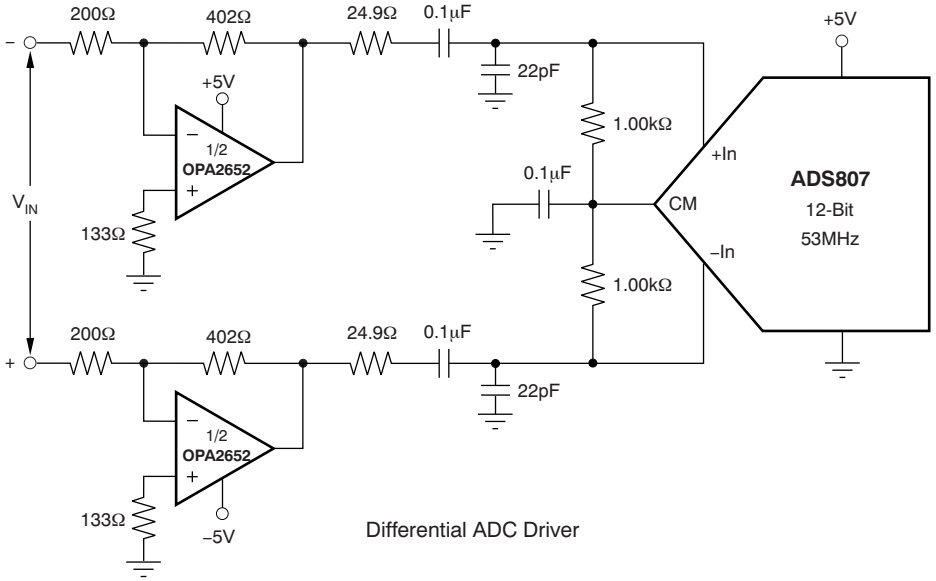
DESCRIPTION

The OPA2652 is a dual, low-cost, wideband voltage feedback amplifier intended for price-sensitive applications. It features a high gain bandwidth product of 200MHz on only 5.5mA/channel quiescent current. Intended for operation on ±5V supplies, it also supports applications on a single supply from +6V to +12V with 140mA output current. Its classical differential input, voltage-feedback design allows wide application in active filters, integrators, transimpedance amplifiers, and differential receivers.

The OPA2652 is internally compensated for unity gain stability. It has exceptional bandwidth (700MHz) as a unity gain buffer, with little peaking (0dB typ). Excellent DC accuracy is achieved with a low 1.5mV input offset voltage and 300nA input offset current.

RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	NOTES
OPA650	OPA2650	—	OPA4650	±5V Spec
OPA680	OPA2680	OPA3680	—	+5V Capable
OPA631	OPA2631	—	—	+3V Capable
OPA634	OPA2634	—	—	+3V Capable



Differential ADC Driver

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2652U	SO-8	D	–40°C to +85°C	OPA2652U	OPA2652U	Rails
					OPA2652U/2K5	Tape and Reel, 2500
OPA2652E	SOT23-8	DCN	–40°C to +85°C	C52	OPA2652E/250	Tape and Reel, 250
					OPA2652E/3K	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

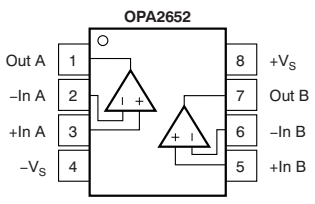
over operating free-air temperature range (unless otherwise noted)(1)

	OPA2652	UNIT
Supply voltage	±6.5	V
Internal power dissipation	See Thermal Characteristics	
Differential input voltage	±1.2	V
Input voltage range	$\pm V_S$	V
Storage temperature range	–40 to +125	°C
Lead temperature (SO-8)	+260	°C
Junction temperature, T_J	+175	°C
ESD rating:		
Human body model	2000	V
Machine model	200	V

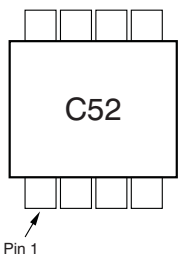
(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PIN CONFIGURATION

Top View — SO-8, SOT23-8



SOT23-8 Marking / Pin Orientation



ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29 for AC performance only.

		OPA2652U, E						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE	(Figure 28 and Figure 29)							
Small-Signal Bandwidth	G = +1, R_F = 25Ω, V_O = 200mV_{PP}	700				MHz	typ	C
	G = +2,V_O = 200mV_{PP}	200				MHz	typ	C
	G = +5,V_O = 200mV_{PP}	45				MHz	typ	C
Gain Bandwidth Product	G ≥ +10	200				MHz	typ	C
Bandwidth for 0.1dB Flatness	V_O = 200mV_{PP}	50				MHz	typ	C
Peaking at a Gain of +1	G = +1, R_F = 25Ω, V_O = 200mV_{PP}	0				dB	typ	C
Slew Rate	4V step	335				V/µs	typ	C
Rise-and-Fall Time	200mV step	2.0				ns	typ	C
	4V step	10				ns	typ	C
Large-Signal Bandwidth	V_O = 4V_{PP}	50				MHz	typ	C
SFDR	V_O = 2V_{PP}, 5MHz	66				dB	typ	C
Input Voltage Noise	f > 1MHz	8				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	1.4				pA/√Hz	typ	C
Differential Gain Error	NTSC, R_L = 150Ω	0.05				%	typ	C
Differential Phase Error	NTSC, R_L = 150Ω	0.03				degrees	typ	C
Channel-to-Channel Crosstalk	f = 5MHz	–100				dBc	typ	C
DC PERFORMANCE(4)	V_{CM} = 0V							
Open-Loop Voltage Gain (A_{OL})		63	56	55	54	dB	min	A
Input Offset Voltage		±1.5	±7			mV	max	A
Average Offset Drift				5	7	µV/°C	max	B
Input Bias Current		4	15	20	25	µA	max	A
Input Bias Current Drift						µA/°C	max	B
Input Offset Current		±0.3	±1.0	±1.4	±2.0	µA	max	A
Input Offset Current Drift						µA/°C	max	B
INPUT(4)								
Common-Mode Input Range		±4.0	±3.0	±2.8	±2.7	V	min	A
Common-Mode Rejection Ratio		95	75			dB	min	A
Input Impedance	V_{CM} = 0V							
Differential		35 || 1				kΩ || pF	typ	C
Common-Mode		18 || 1				MΩ || pF	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(4) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29 for AC performance only.

PARAMETER	CONDITIONS	OPA2652U, E				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
OUTPUT								
Voltage Output Swing	1kΩ load	±3.0	±2.4			V	min	A
	100Ω load	±2.5	±2.2			V	min	A
Output Current, Sourcing	V_O = 0V	140	100	85	75	mA	min	A
Output Current, Sinking	V_O = 0V	140	100	85	75	mA	min	A
Closed-Loop Output Impedance	f < 100kHz	0.06				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			±6	±6	±6	V	max	A
Maximum Quiescent Current	Total both channels	11	13.2	14	15.5	mA	max	A
Minimum Quiescent Current	Total both channels	11	8.8	8	7.5	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input-referred	58	54			dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Temperature Range	U, E Packages	–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U SO-8		125				°C/W	typ	C
E SOT23-8		150				°C/W	typ	C

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

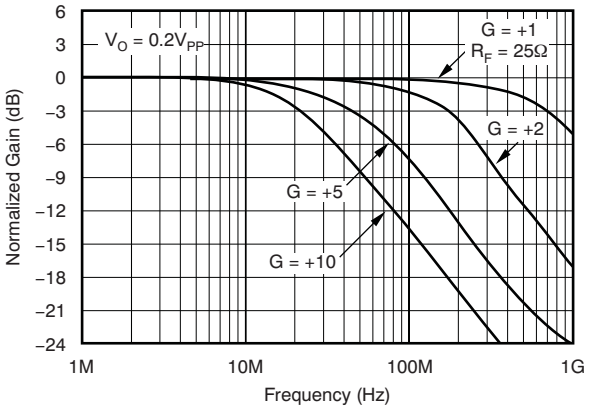


Figure 1.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

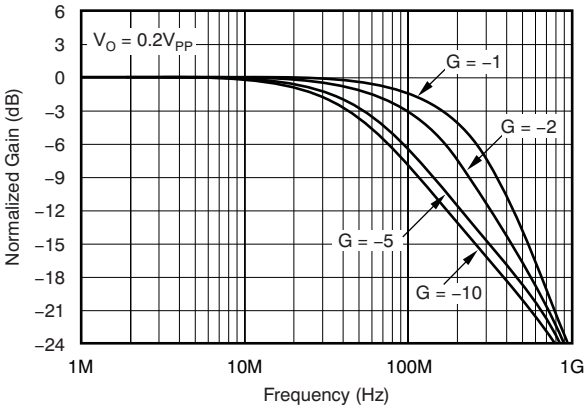


Figure 2.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

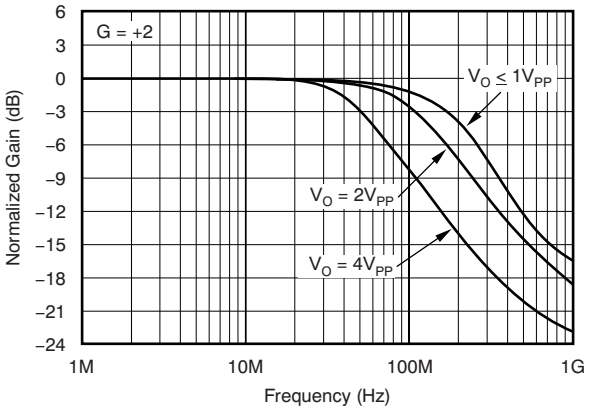


Figure 3.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

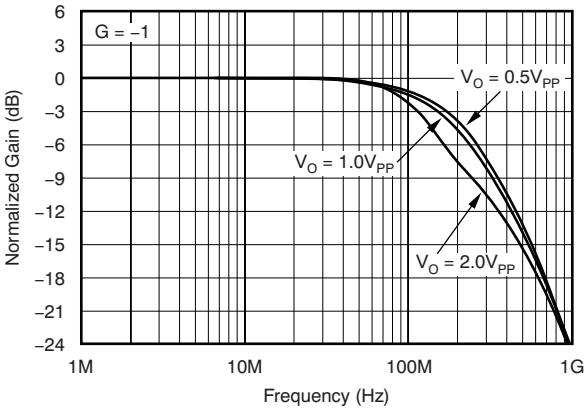


Figure 4.

NONINVERTING PULSE RESPONSE

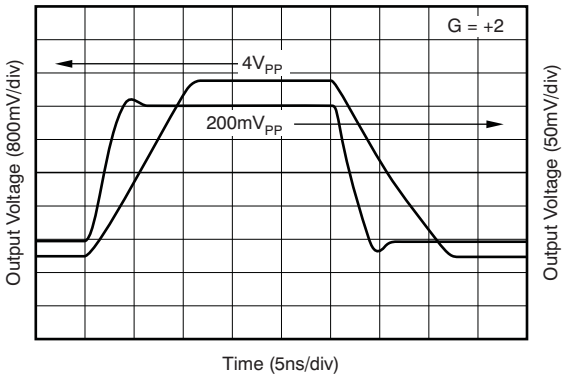


Figure 5.

INVERTING PULSE RESPONSE

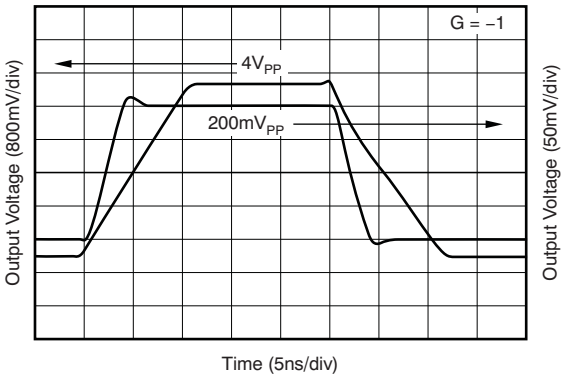


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29.

HARMONIC DISTORTION vs NONINVERTING GAIN

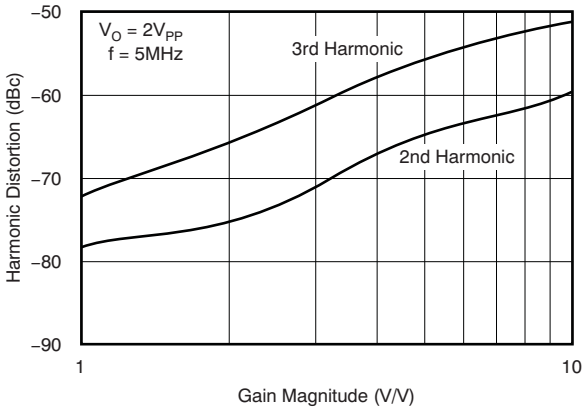


Figure 7.

HARMONIC DISTORTION vs INVERTING GAIN

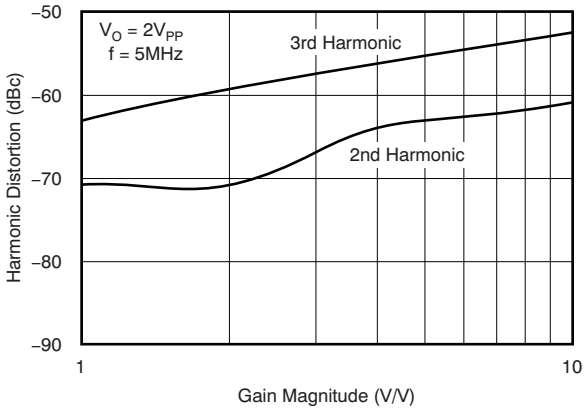


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

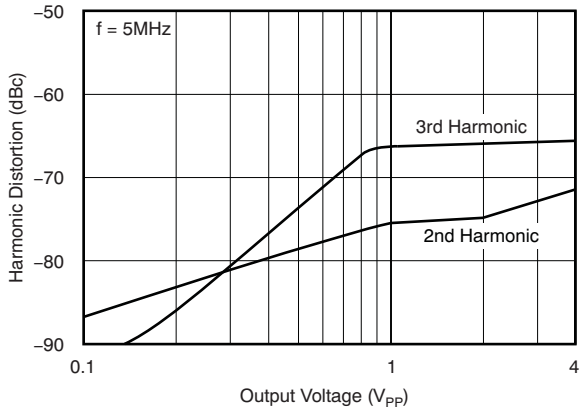


Figure 9.

HARMONIC DISTORTION vs FREQUENCY

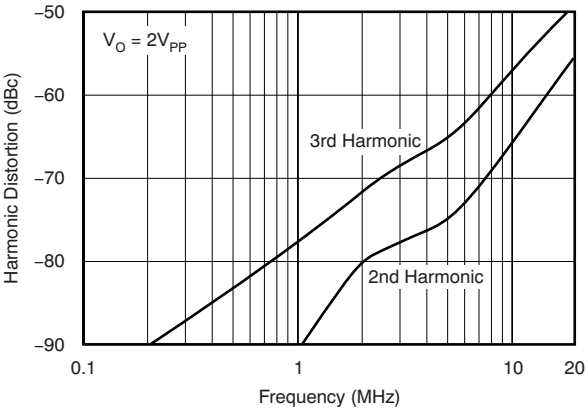


Figure 10.

HARMONIC DISTORTION vs LOAD RESISTANCE

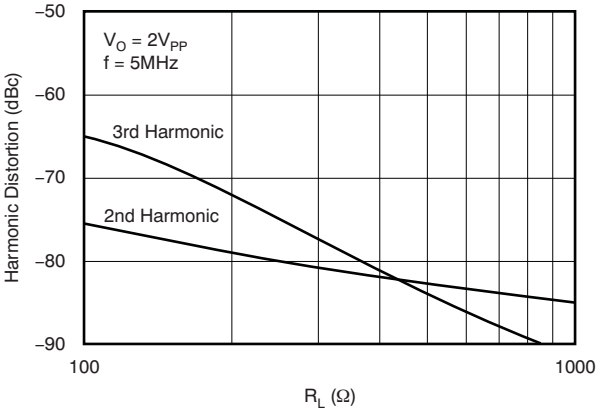


Figure 11.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

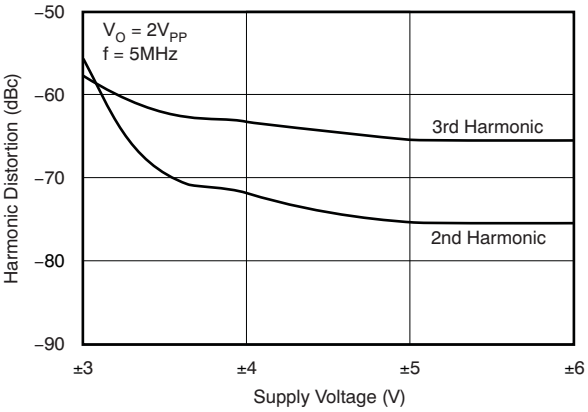


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29.

TWO-TONE, 3rd-ORDER SPURIOUS LEVEL

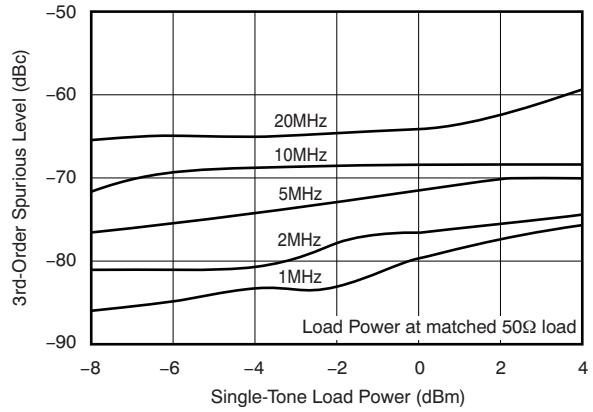


Figure 13.

COMPOSITE VIDEO dG/dϕ

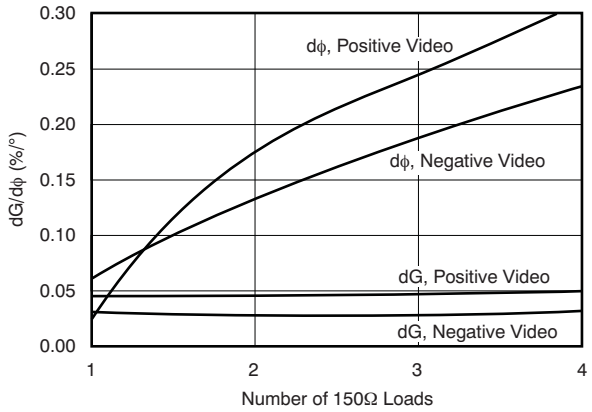


Figure 14.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

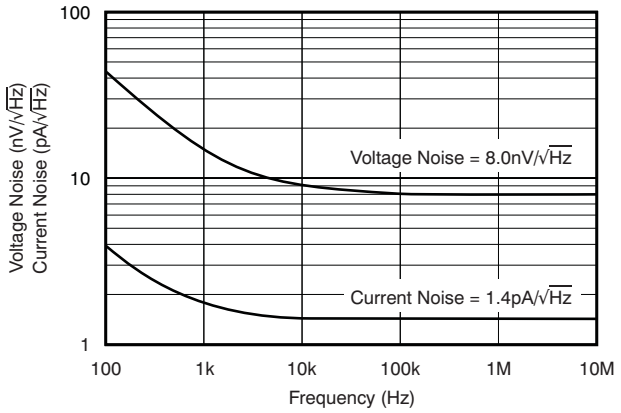


Figure 15.

CHANNEL-TO-CHANNEL CROSSTALK

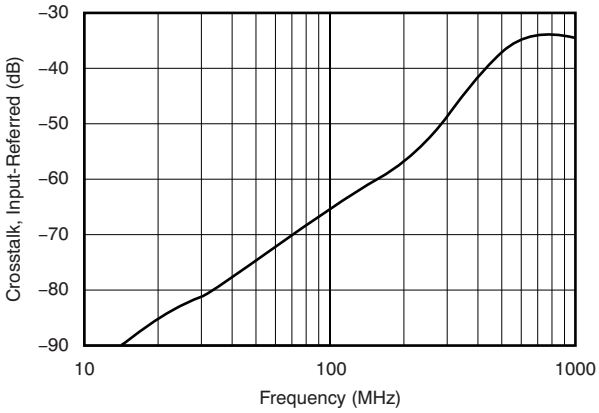


Figure 16.

RECOMMENDED R_S vs CAPACITIVE LOAD

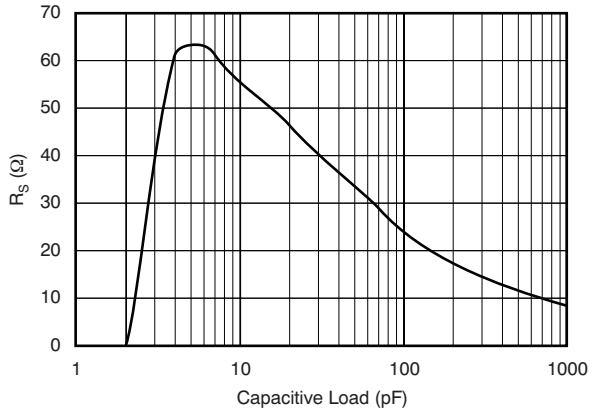


Figure 17.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

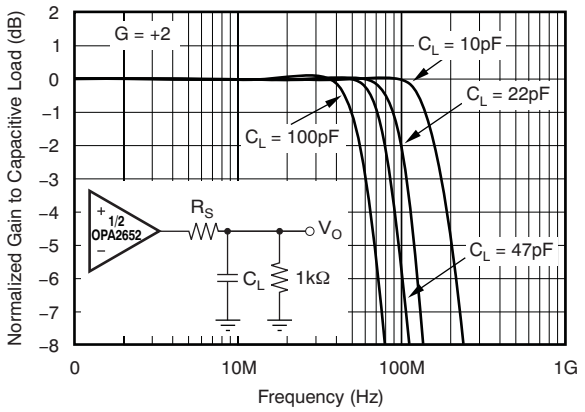


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29.

CMRR AND PSRR vs FREQUENCY

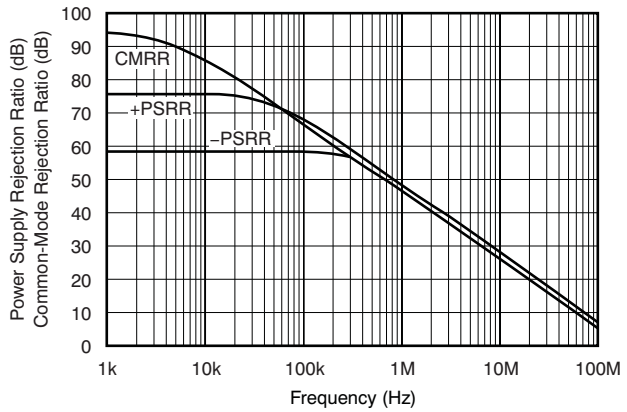


Figure 19.

OPEN-LOOP GAIN AND PHASE

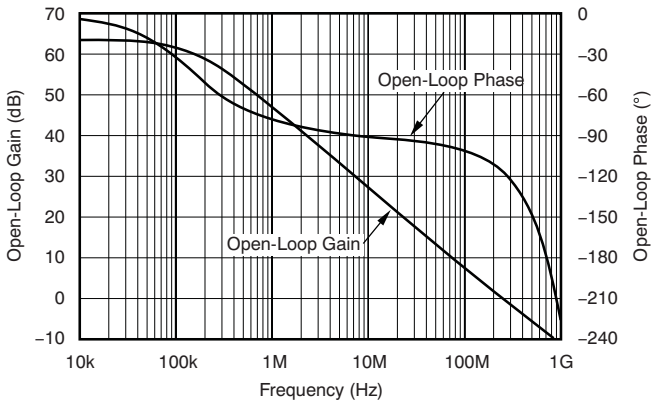


Figure 20.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

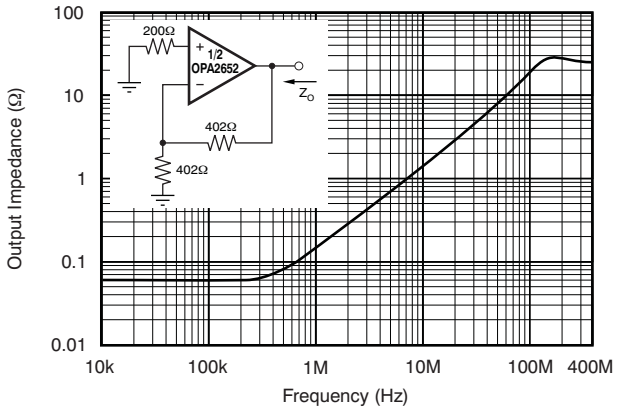


Figure 21.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

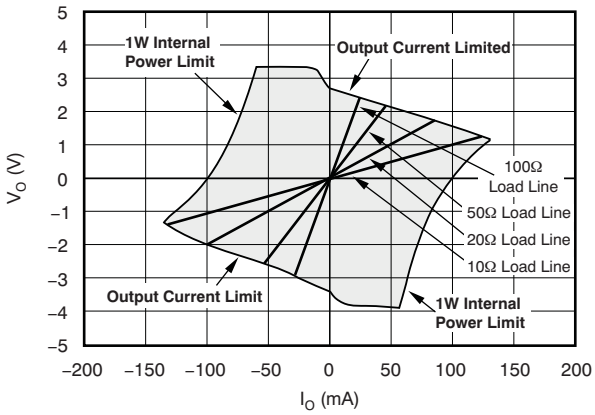


Figure 22.

NONINVERTING OVERDRIVE RECOVERY

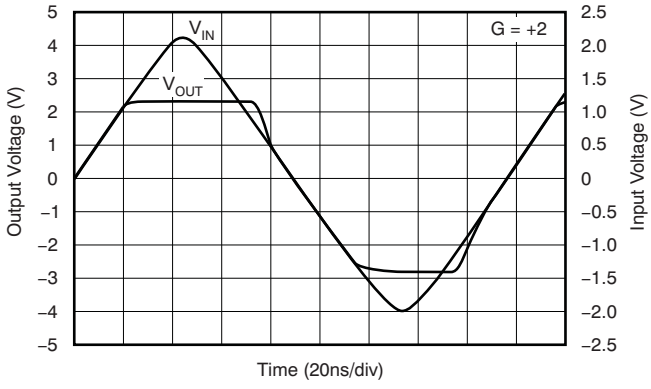


Figure 23.

INVERTING OVERDRIVE RECOVERY

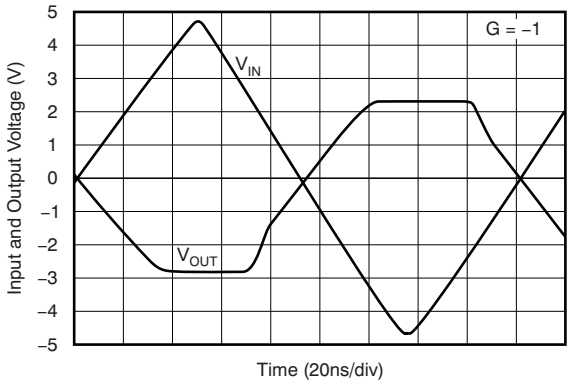


Figure 24.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 28 and Figure 29.

TYPICAL DC DRIFT OVER TEMPERATURE

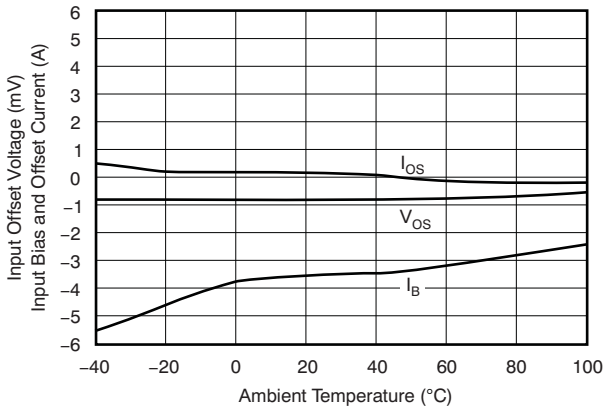


Figure 25.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

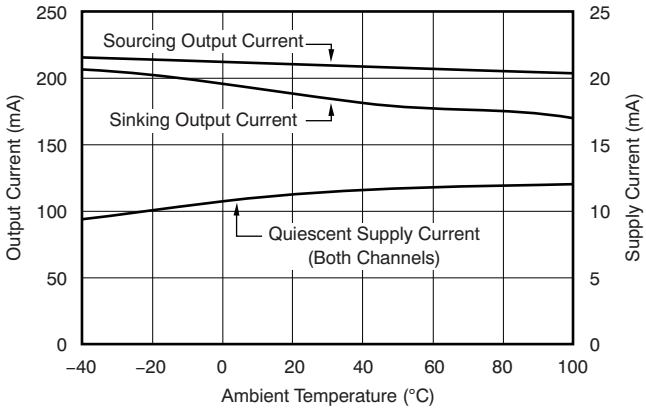


Figure 26.

COMMON-MODE INPUT VOLTAGE RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE

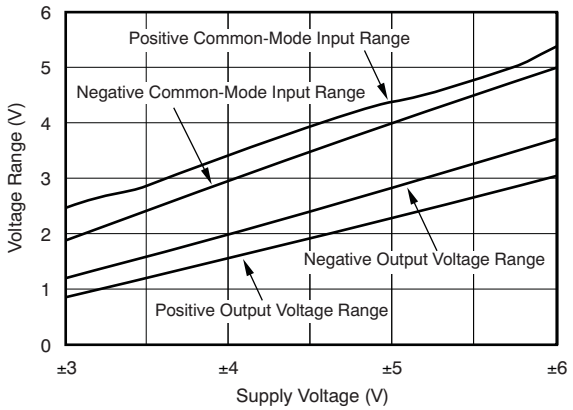


Figure 27.

APPLICATIONS INFORMATION

Wideband Voltage Feedback Operation

The OPA2652 is a dual, low-power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA2652 voltage feedback architecture features true differential and fully symmetrical inputs. This architecture minimizes offset errors, making the OPA2652 well-suited for implementing filter and instrumentation designs. As a dual operational amplifier, OPA2652 is an ideal choice for designs that require multiple channels where reduction of board space, power dissipation and cost are critical. Its AC performance is optimized to provide a gain bandwidth product of 200MHz and a fast rise time of 2.0ns, which is an important consideration in high-speed data conversion applications. The low DC input offset of ±1.5mV and drift of ±5µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the dual current feedback OPA2694, or the OPA2691.

Figure 28 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V specifications and typical characteristics. This configuration is for one channel. The other channel is connected similarly. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor.

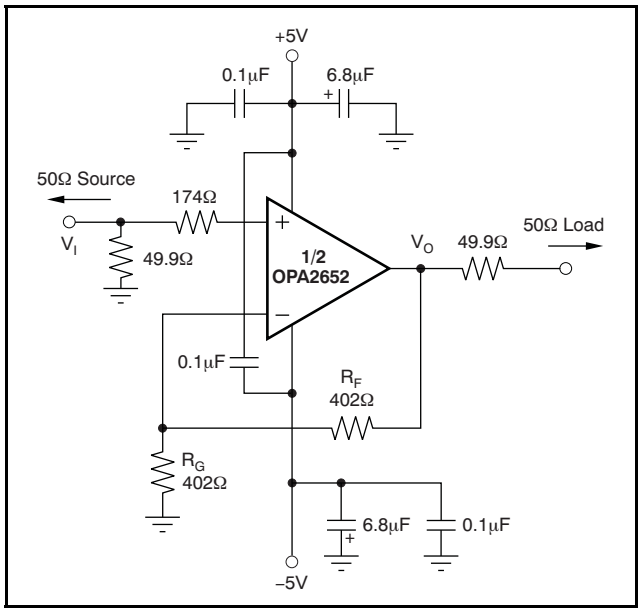


Figure 28. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit

Voltage swings reported in the specifications are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 28, the total effective load will be 100Ω || 804Ω. Two optional components are included in Figure 28.

An additional resistor (174Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this additional resistor gives an input bias current cancelling resistance that matches the 201Ω source resistance seen at the inverting input (see the ***DC Accuracy and Offset Control*** section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional-added capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 29 shows the DC-coupled, gain of –1, bipolar supply circuit configuration that is the basis of the specifications and typical characteristics at G = –1. The input impedance matching resistor (57.6Ω) used for testing gives a 50Ω input load. A resistor (205Ω) connects the noninverting input to ground. This configuration provides the DC source resistance matching to cancel outputs errors arising from input bias current.

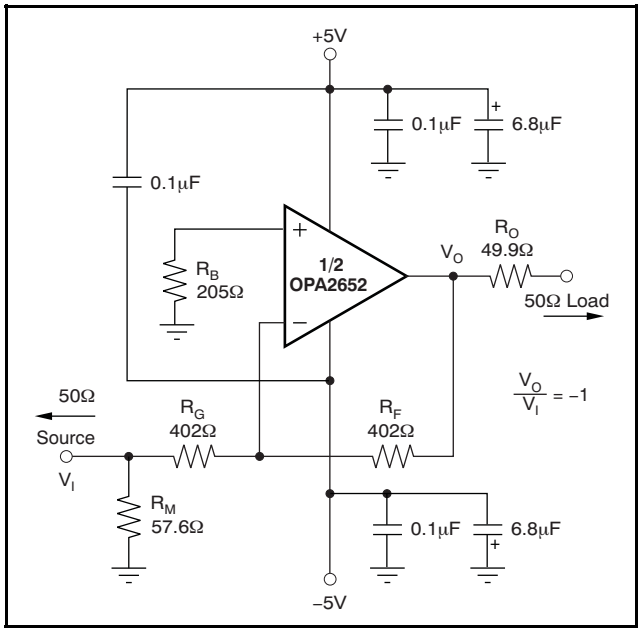


Figure 29. DC-Coupled, G = –1, Bipolar Supply, Specification and Test Circuit

Differential ADC Driver

The circuit on the front page shows an OPA2652 driving the ADS807 analog-to-digital converter (ADC) differentially, at a gain of +2V/V. The outputs are AC-coupled to the converter to adjust for the difference in supply voltages. The 133Ω resistors at the noninverting inputs minimize DC offset errors. The differential topology minimizes even-order distortion products, such as second-harmonic distortion.

Bandpass Filter

Figure 31 shows a single OPA2652 implementing a sixth-order bandpass filter. This filter cascades two second-order Sallen-Key sections with transmission zeros, and a double real pole section. It has 0.3dB of ripple, –3dB frequencies of 450kHz and 11MHz, and –23dB frequencies of 315kHz and 16MHz. The 20.0Ω resistor isolates the first OPA2652 output from capacitive loading. This configuration improves stability with minimal impact on the filter response. Figure 30 shows the nominal response simulated by SPICE.

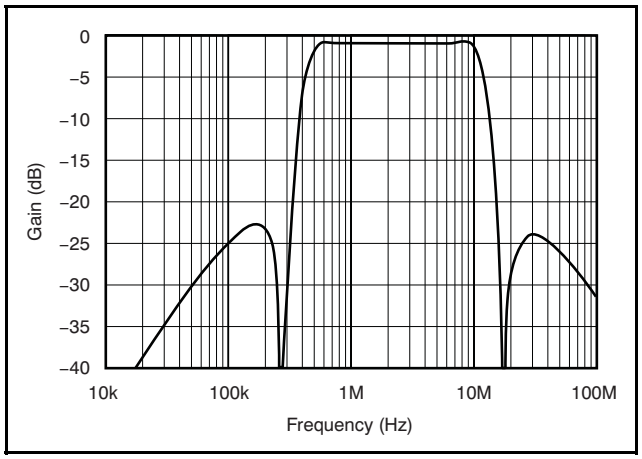


Figure 30. Nominal Filter Response

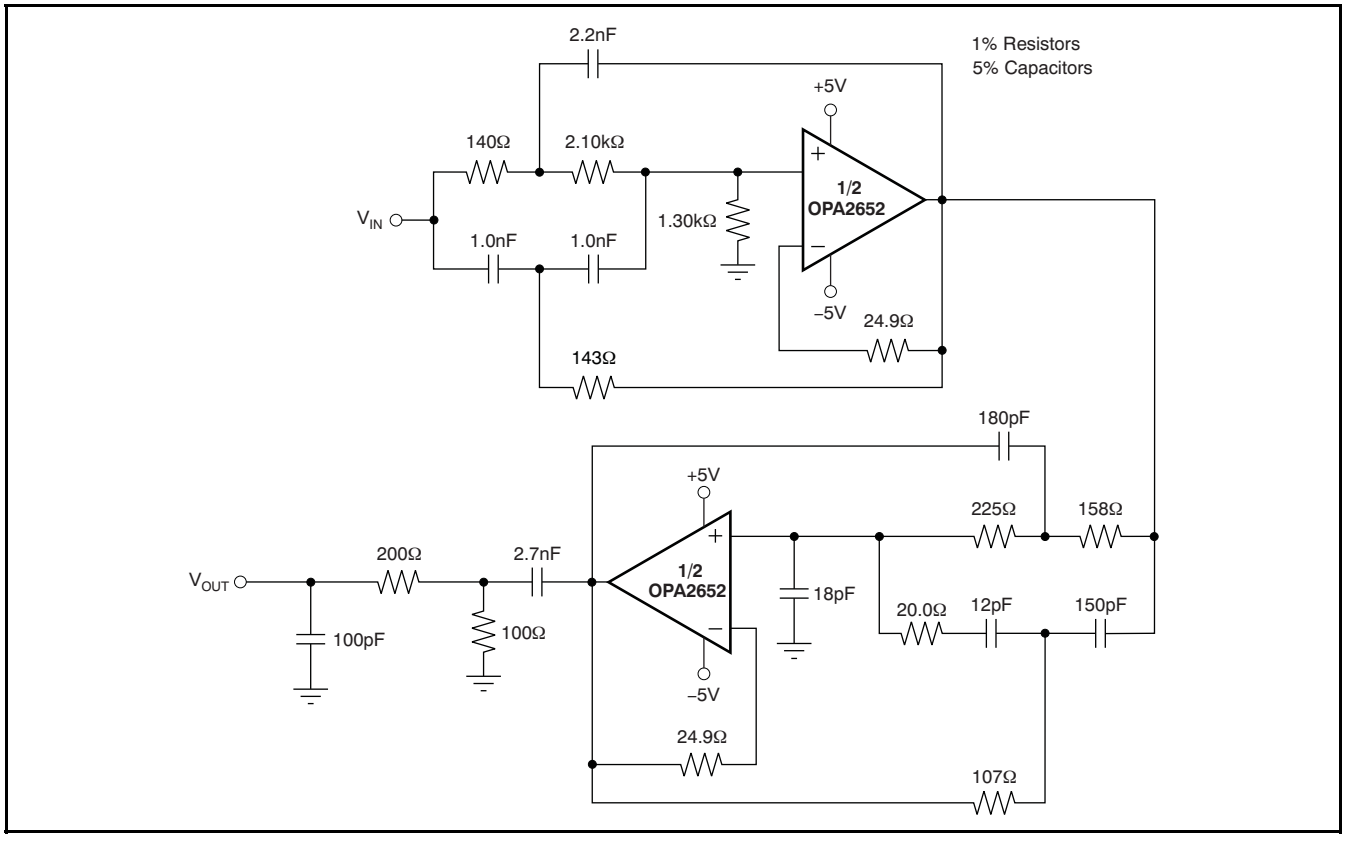


Figure 31. Bandpass Filter

Video Line Driver

Figure 32 shows the OPA2652 used as a video line driver. Its outstanding differential gain and phase allow it to be used in studio equipment, while its low cost and SOT23-8 package option also support consumer applications.

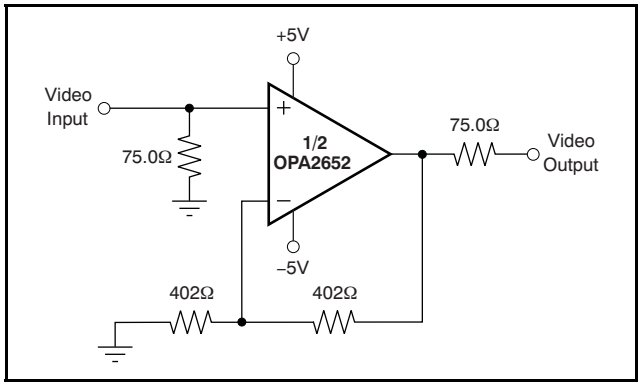


Figure 32. Video Line Driver

Pulse Delay Circuit

Figure 33 shows the OPA2652 used in a pulse delay circuit. This circuit cascades the two op amps in the OPA2652, each forming a single pole, active allpass filter. The overall gain is +1, and the overall delay through the filter is:

$t_{GD} = n(2RC)$, overall group delay

n = 2, the number of cascaded stages

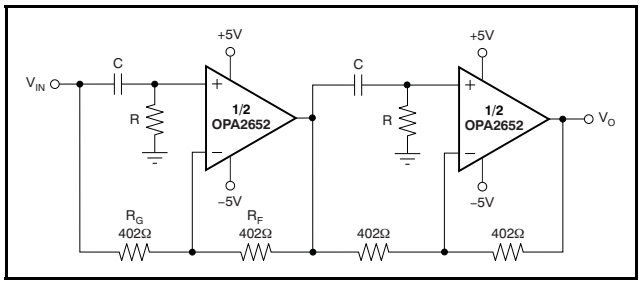


Figure 33. Pulse Delay Circuit

R_F and R_G need to be equal to maintain a constant gain magnitude. The rise and fall times of the input pulses, $tr_{(IN)}$, should be slow enough to prevent pre-shoot artifacts in the response.

$tr_{(IN)} \geq 5RC$, minimal pre-shoot

Simple Bandpass Filter

Figure 34 shows the OPA2652 used as simple bandpass filter. The OPA2652 is well-suited for this type of circuit because it is very stable at a noise gain of +1.

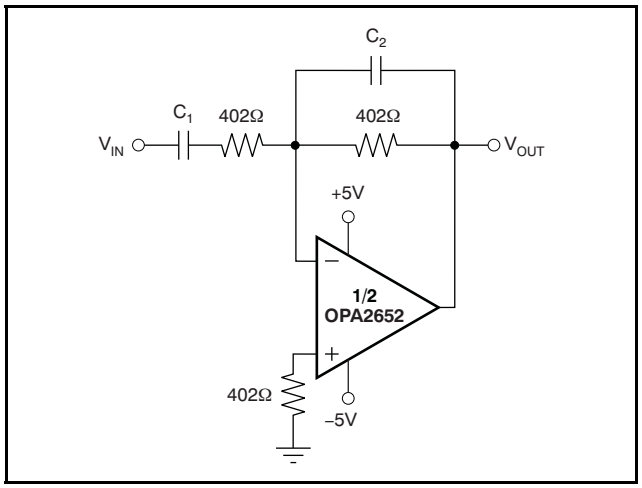


Figure 34. Inverting Bandpass Filter

DESIGN-IN TOOLS

Demonstration Fixtures

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2652 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures for the OPA2652

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2652U	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2652E	SOT23-8	DEM-OPA-SOT-2A	SBOU001

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2652 product folder.

Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This method is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. Check the Texas Instruments web site (www.ti.com) for available SPICE products (note that not all parts have models). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dϕ characteristics. These models do not attempt to distinguish between the package types in small-signal AC performance.

OPERATING SUGGESTIONS

Optimizing Resistor Values

Because the OPA2652 is a unity gain stable voltage feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short. This configuration isolates the inverting input capacitance from the output pin and improves the frequency response flatness. Usually, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA2652. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional bandlimiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 28) to be less than approximately 300Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G < 300\Omega$ keeps this pole above 250MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This increase is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

Bandwidth vs Gain: Noninverting Operation

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) predicts the closed-loop bandwidth. In practice, this prediction only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factor), most amplifiers exhibit a wider bandwidth and lower phase margin. The OPA2652 is compensated to give a flat response in a noninverting gain of 1 (see Figure 28). This configuration results in a typical gain of +1 bandwidth of 700MHz, far exceeding that predicted by dividing the 200MHz GBP by NG = 1. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +5, the 45MHz bandwidth shown in the Electrical Characteristics is close to that predicted using this simple formula.

Inverting Amplifier Operation

Because the OPA2652 is a general-purpose, wideband voltage feedback op amp, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. Figure 29 shows a typical inverting configuration.

In the inverting configuration, three key design consideration must be noted. First, the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This approach is the simplest, and results in optimum bandwidth and noise performance. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of –1, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 50_W feedback resistor. This configuration has the interesting advantage that the noise gain becomes equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered above. However, the amplifier output now sees the 50Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values as shown in Figure 29, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in Figure 29, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of $50\Omega \parallel 57.6\Omega = 26.8\Omega$. This impedance is added in series with R_G for calculating the noise gain (NG). The resulting NG is 1.94 for Figure 29 (an ideal source would cause NG = 2.00).

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC

error, as a result of the input bias currents, is reduced to (Input Offset Current) • R_F. If the 50Ω source impedance is DC-coupled in Figure 29, the total resistance to ground on the inverting input will be 429Ω. Combining this in parallel with the feedback resistor gives 208Ω, which is close to the R_B = 205Ω used in Figure 29. To reduce the additional high-frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as R_B <300Ω, the capacitor is not required since its total noise contribution is much less than that of the op amp input noise voltage.

Output Current and Voltage

The OPA2652 specifications in the spec table, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or VI product, that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero current output voltage limit, respectively. The four quadrants give a more detailed view of the device output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation (500mW for each channel). Superimposing resistor load lines onto the plot shows that the OPA2652 can drive ±2.2V into 50Ω or ±2.5V into 100Ω without exceeding the output capabilities, or the 1W dissipation boundary line.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This configuration will not normally be a problem since most applications include a series matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power supply pin will, in most cases, destroy the amplifier. Including a small series resistor (5Ω) in the power-supply line will protect against this. Always place the 0.1µF decoupling capacitor directly on the supply pins.

Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an analog-to-digital (A/D) converter—including additional external capacitance that may be recommended to improve A/D linearity. A high-speed amplifier such as the OPA2652 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This resistor does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2652. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2652 output pin (see **Board Layout Guidelines**).

Distortion Performance

The OPA2652 provides good distortion performance into a 100Ω load on ±5V supplies. Increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (Figure 28), this is sum of R_F + R_G, while in the inverting configuration, it is only R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

It is also true that increasing the output voltage swing increases harmonic distortion.

Noise Performance

The OPA2652 input-referred voltage noise (8nV/$\sqrt{Hz}$), and the two input-referred current noise terms (1.4pA/$\sqrt{Hz}$), combine to give low output noise under a wide variety of operating conditions. Figure 35 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

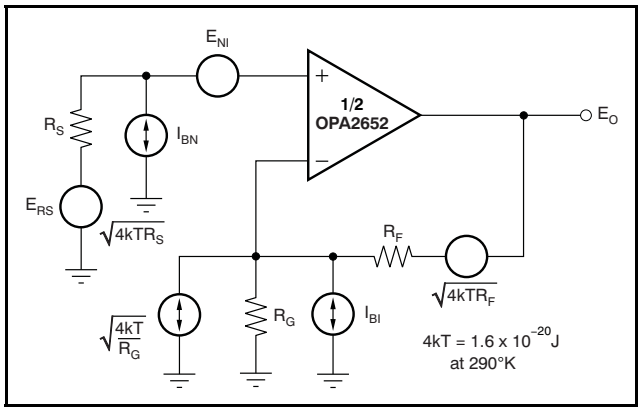


Figure 35. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 35.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (1)$$

Dividing this expression by the noise gain (NG = 1 + R_F/R_G) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 2.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (2)$$

Evaluating these two equations for the OPA2652 circuit and component values shown in Figure 28 gives a total output spot noise voltage of 17nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 8.4nV/$\sqrt{Hz}$. This noise includes the noise added by the bias current cancellation resistor (205Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 8nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This result will be the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 300Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300Ω satisfies both noise and frequency response flatness considerations. Since the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 29 is not required.

DC Accuracy and Offset Control

The balanced input stage of a wideband voltage feedback op amp allows good output DC accuracy in a wide variety of applications. Although the high-speed input stage does require relatively high input bias current (typically 4μA out of each input terminal), the close matching between them may be used to significantly reduce the output DC error caused by this current. This reduction is done by matching the DC source resistances appearing at the two inputs. This matching reduces the output DC error resulting from the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 28, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

$$\pm \left(NG \cdot V_{OS(MAX)}\right) \pm \left(R_F \cdot I_{OS(MAX)}\right)$$
$$= \pm (1.94 \cdot 7.0mV) \pm (402\Omega \cdot 1.0\mu A)$$
$$= \pm 14.0mV$$

(NG = noninverting signal gain)

A fine scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques add a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the DC offset voltage on the summing junction sets up a DC current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 36 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the DC offset current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This configuration ensures that the adjustment circuit has minimal effect on the loop gain, and therefore on the frequency response as well.

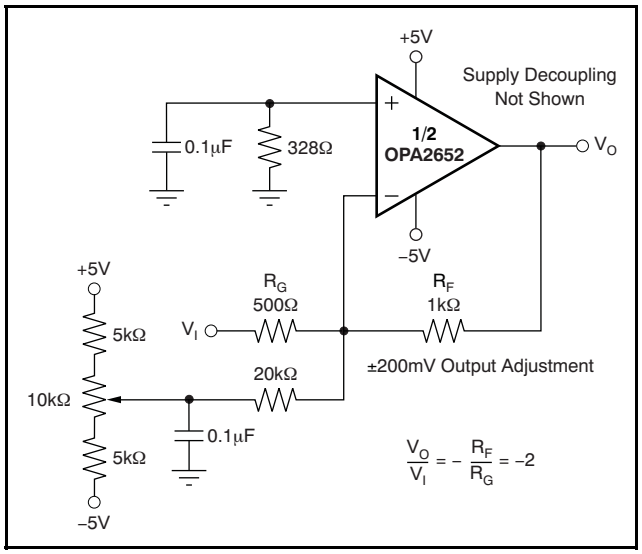


Figure 36. DC-Coupled, Inverting Gain of –2, with Offset Adjustment

Thermal Analysis

Heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As an example, compute the maximum T_J using an OPA2652E (SOT23-8 package) in the circuit of Figure 28 operating at the maximum specified ambient temperature of +85°C and with both outputs driving $2.5V_{DC}$ into a grounded 100Ω load.

$P_D = 10V \bullet 15.5mA + 2\ [5^2/(4 \bullet [100\Omega \| 804\Omega])] = 296mW$

Maximum $T_J = +85°C + (0.30W \bullet 150°C/W) = 130°C$

This absolute worst-case condition meets the specified maximum junction temperature. Actual P_{DL} will almost always be less than that considered here. Carefully consider maximum T_J in your application.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA2652 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA2652. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axiallyleaded resistors can also provide good high frequency performance. Again, keep resistor leads and PCB traces as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side

of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values >1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402Ω feedback used in the typical performance specifications is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for the unity gain follower application. This effectively isolates the inverting input capacitance from the output pin that would otherwise cause additional peaking in the gain of +1 frequency response.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load (Figure 17). Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2652 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2652 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2652 allows multiple destination devices to be handled as separate transmission lines, each with respective series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Recommended R_S vs Capacitive Load (Figure 17). This configuration will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2652 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2652 directly onto the board.

Input and ESD Protection

The OPA2652 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 37.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2652), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

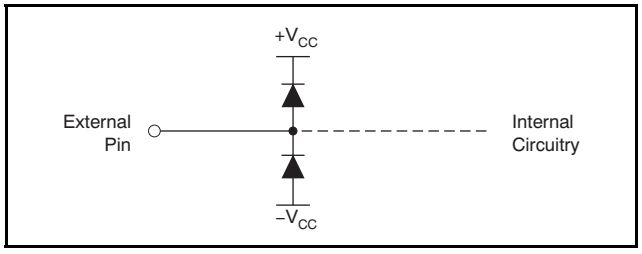


Figure 37. Internal ESD Protection

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2000) to A Revision	Page
• Changed format of data sheet. Updated to XML from PageMaker.	1
• Changed input voltage axis values to correct units.	8
• Changed reference to alternate part numbers.	10
• Changed information regarding available demonstration fixtures.	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2652E/250	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C52	Samples
OPA2652E/250G4	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C52	Samples
OPA2652E/3K	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C52	Samples
OPA2652U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2652U	Samples
OPA2652U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2652U	Samples
OPA2652U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2652U	Samples
OPA2652UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2652U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

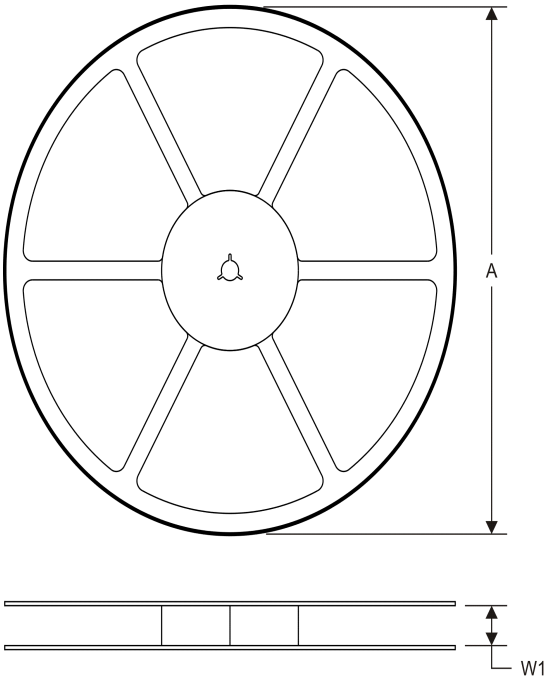
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

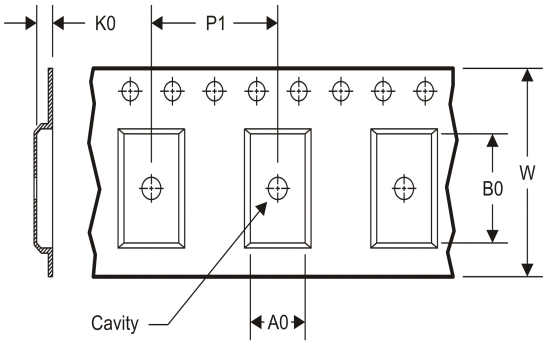
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



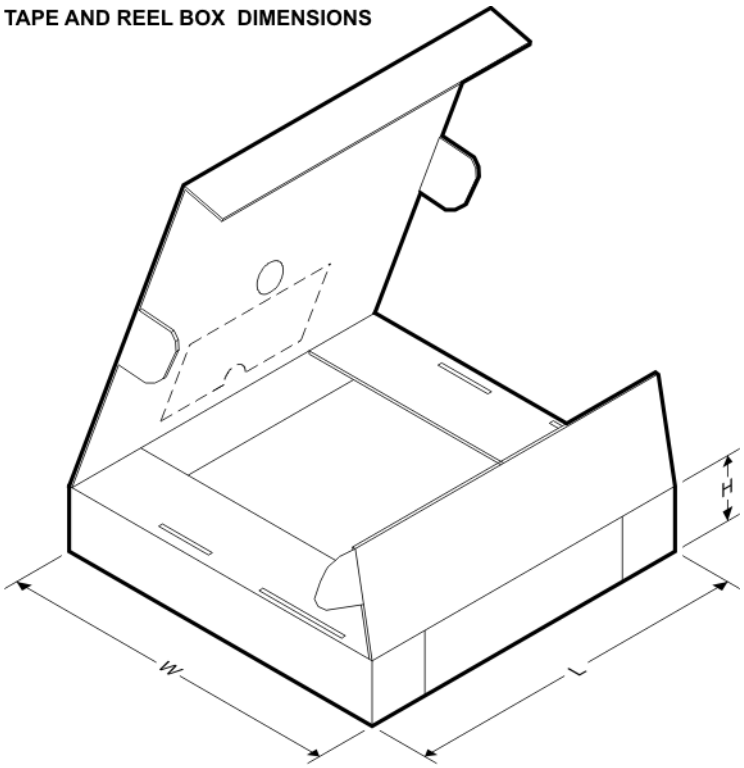
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2652E/250	SOT-23	DCN	8	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA2652E/3K	SOT-23	DCN	8	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA2652U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2652E/250	SOT-23	DCN	8	250	210.0	185.0	35.0
OPA2652E/3K	SOT-23	DCN	8	3000	210.0	185.0	35.0
OPA2652U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

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