

## 4-Mbit (256K x 16) Static RAM

### Features

- Very high speed: 45 ns
- Wide voltage range: 4.5V–5.5V
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- Ultra low active power
  - Typical active current: 2 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 44-pin TSOP II package

### Functional Description<sup>[1]</sup>

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the

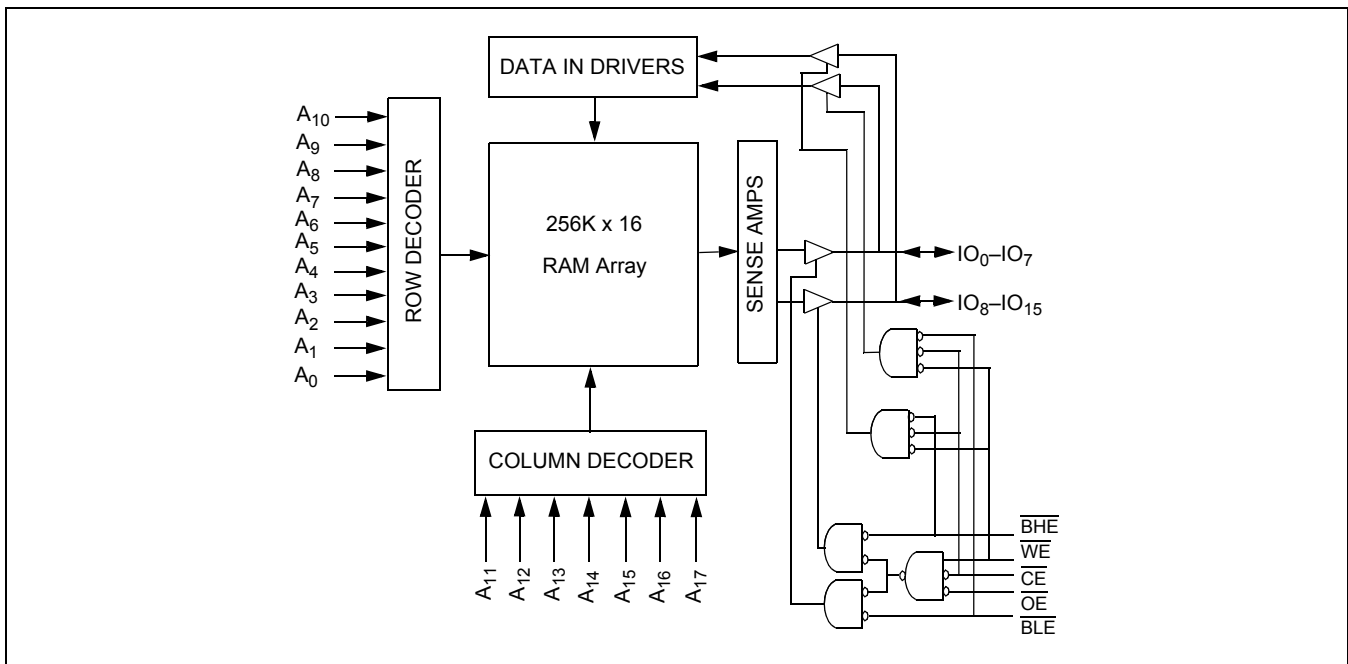
device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both byte high enable and byte low enable are disabled (BHE, BLE HIGH)
- When the write operation is active ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW)

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 9 for a complete description of read and write modes.

### Logic Block Diagram

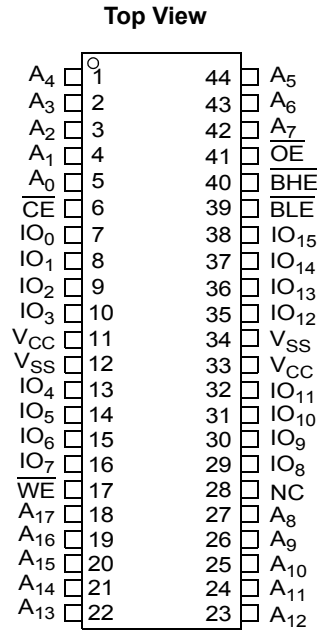


#### Note

1. For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

## Pin Configurations

The figure that follows shows the 44-Pin TSOP II pinout.<sup>[2]</sup>



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
						f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max			
CY62146ELL	Ind'l/Auto-A	4.5	5.0	5.5	45 ns	2	2.5	15	20	1	7

### Notes

2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°.

## Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Storage Temperature .....	-65°C to + 150°C
Ambient Temperature with Power Applied .....	-55°C to + 125°C
Supply Voltage to Ground Potential .....	-0.5V to + 6V ( $V_{CCmax} + 0.5V$ )
DC Voltage Applied to Outputs in High-Z State <sup>[4, 5]</sup> .....	-0.5V to 6V ( $V_{CCmax} + 0.5V$ )

DC Input Voltage <sup>[4, 5]</sup> .....	-0.5V to 6V ( $V_{CCmax} + 0.5V$ )
Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage .....	>2001V (MIL-STD-883, Method 3015)
Latch up Current.....	>200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
CY62146ELL	Ind'I/Auto-A	-40°C to +85°C	4.5V to 5.5V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Ind'I/Auto-A)			Unit
			Min	Typ <sup>[3]</sup>	Max	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1.0$ mA	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 4.5V$ to 5.5V	2.2		$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 4.5V$ to 5.5V	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	$\mu$ A
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	$\mu$ A
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{max} = 1/t_{RC}$		15	20	mA
		$f = 1$ MHz		2	2.5	
$I_{SB2}$ <sup>[7]</sup>	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = V_{CC(max)}$		1	7	$\mu$ A

## Capacitance

For all packages. Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz,	10	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

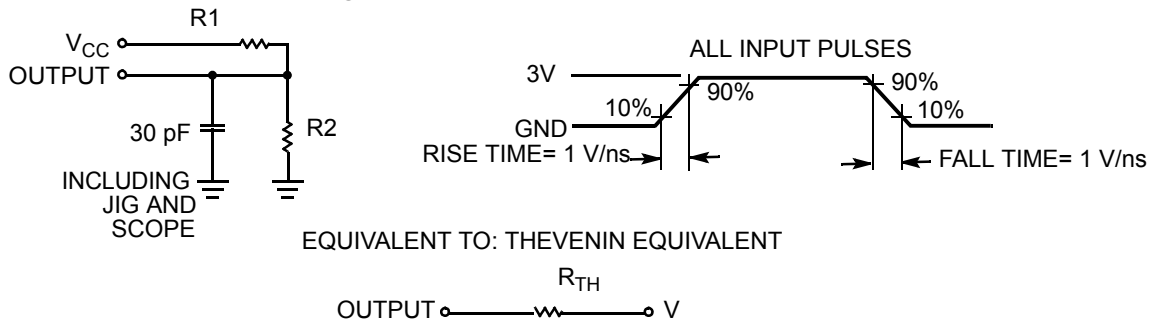
Parameter	Description	Test Conditions	TSOP II Package	Unit
$\Theta_{JA}$	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	77	$^\circ C/W$
$\Theta_{JC}$	Thermal Resistance (junction to case)		13	$^\circ C/W$

### Notes

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns for  $I < 30$  mA.
- $V_{IH(max)}$  =  $V_{CC} + 0.75V$  for pulse durations less than 20 ns.
- Full device AC operations are based on a minimum of 100  $\mu$ s ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu$ s wait time after  $V_{CC}$  stabilization.
- Only chip enable ( $\overline{CE}$ ) and byte enables ( $BHE$  and  $BLE$ ) need to be tied to CMOS levels to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

## AC Test Loads and Waveforms

Figure 1. AC Test Load and Waveforms



Parameters	5.0V	Unit
R1	1800	$\Omega$
R2	990	$\Omega$
R <sub>TH</sub>	639	$\Omega$
V <sub>TH</sub>	1.77	V

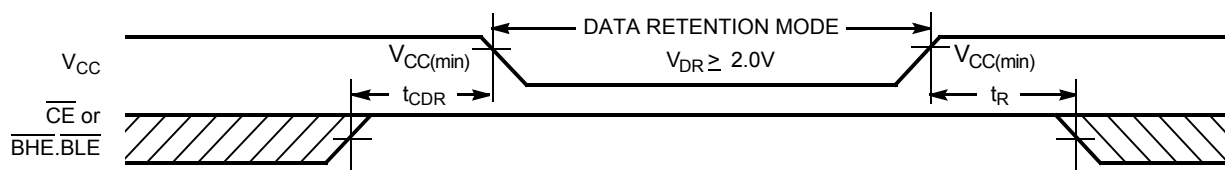
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[3]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2			V
I <sub>CCDR</sub> <sup>[7]</sup>	Data Retention Current	V <sub>CC</sub> = 2V, $\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$		1	7	$\mu A$
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

## Data Retention Waveform<sup>[10]</sup>

Figure 2. Data Retention Waveform



### Notes

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub>  $\geq 100 \mu s$  or stable at V<sub>CC(min)</sub>  $\geq 100 \mu s$ .
10. BHE. BLE is the AND of BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range <sup>[11, 12]</sup>

Parameter	Description	45 ns (Ind'l/Auto-A)		Unit
		Min	Max	
<b>Read Cycle</b>				
t <sub>RC</sub>	Read Cycle Time	45		ns
t <sub>AA</sub>	Address to Data Valid		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[13]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[13, 14]</sup>		18	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[13]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[13, 14]</sup>		18	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power Up	0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power Down		45	ns
t <sub>DBE</sub>	$\overline{BLE/BHE}$ LOW to Data Valid		22	ns
t <sub>LZBE</sub>	$\overline{BLE/BHE}$ LOW to Low <sup>[13]</sup>	5		ns
t <sub>HZBE</sub>	$\overline{BLE/BHE}$ HIGH to High-Z <sup>[13, 14]</sup>		18	ns
<b>Write Cycle<sup>[15]</sup></b>				
t <sub>WC</sub>	Write Cycle Time	45		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	35		ns
t <sub>AW</sub>	Address Setup to Write End	35		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		ns
t <sub>BW</sub>	$\overline{BLE/BHE}$ LOW to Write End	35		ns
t <sub>SD</sub>	Data Setup to Write End	25		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[13, 14]</sup>		18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[13]</sup>	10		ns

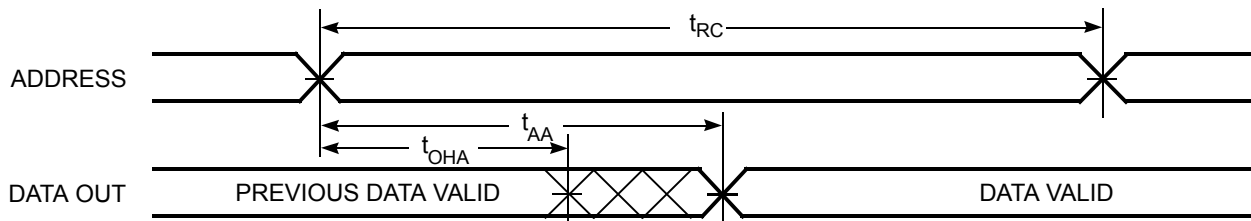
### Notes

11. Test conditions for all parameters other than tri-state parameters are based on signal transition time of 3 ns (1V/ns) or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "AC Test Loads and Waveforms" on page 4.
12. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.
13. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
14. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the output enters a high impedance state.
15. The internal memory write time is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ , BHE, BLE or both = V<sub>IL</sub>. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

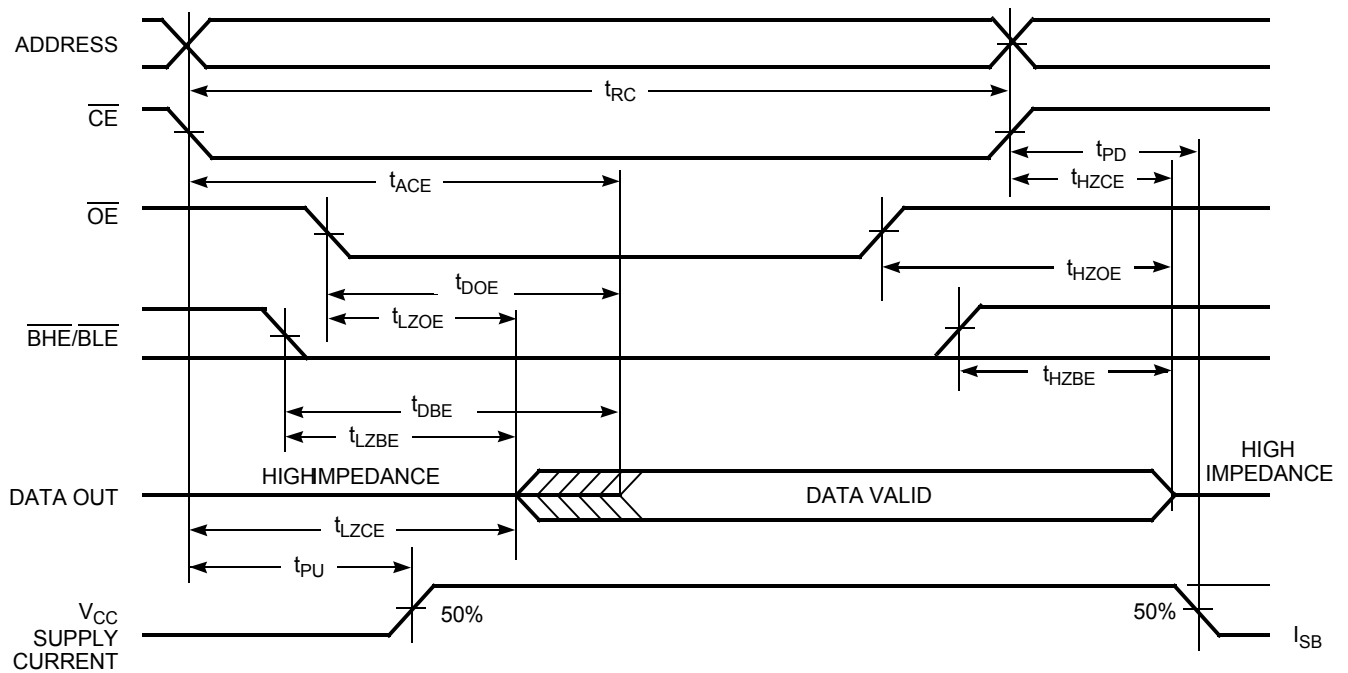
Read Cycle No. 1 (Address Transition Controlled)<sup>[16, 17]</sup>

Figure 3. Read Cycle No. 1



Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[17, 18]</sup>

Figure 4. Read Cycle No. 2



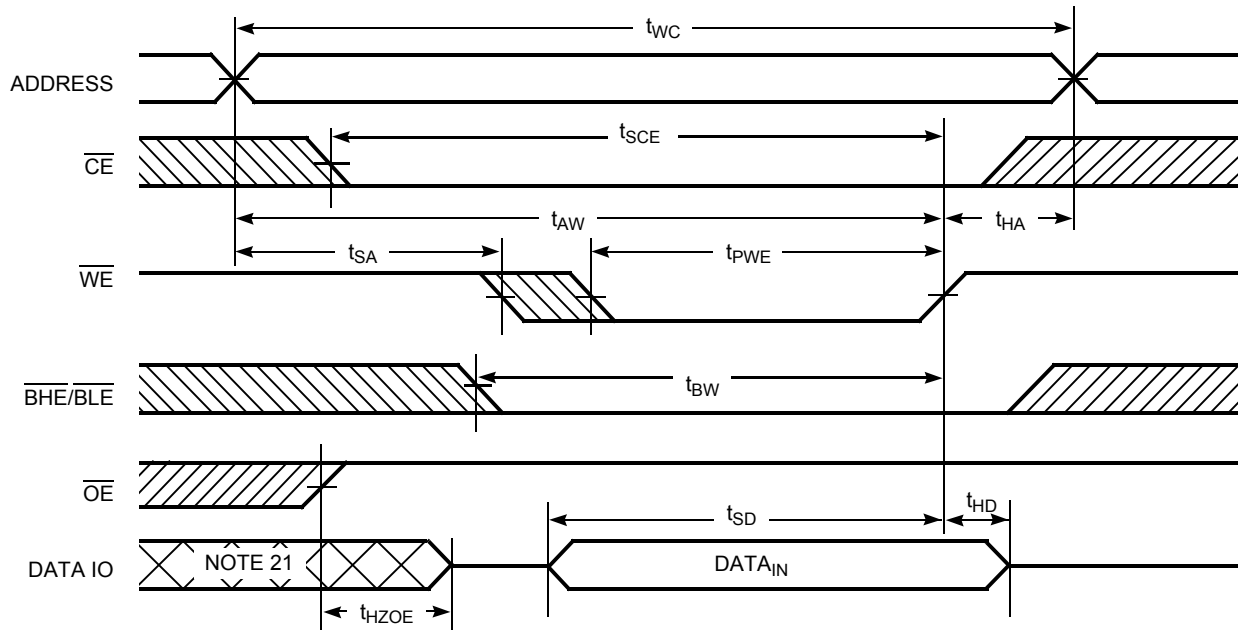
**Notes**

- 16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ .
- 17.  $\overline{WE}$  is HIGH for read cycle.
- 18. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

**Switching Waveforms (continued)**

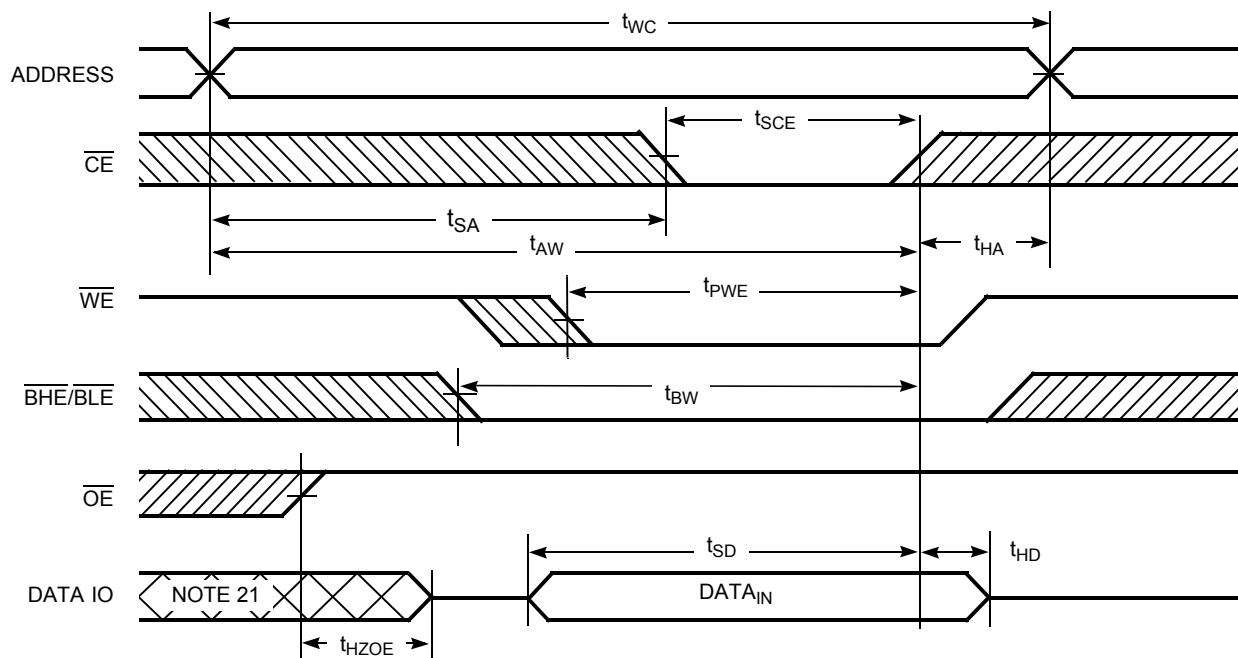
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[15, 19, 20]</sup>**

**Figure 5. Write Cycle No. 1**



**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[15, 19, 20]</sup>**

**Figure 6. Write Cycle No. 2**



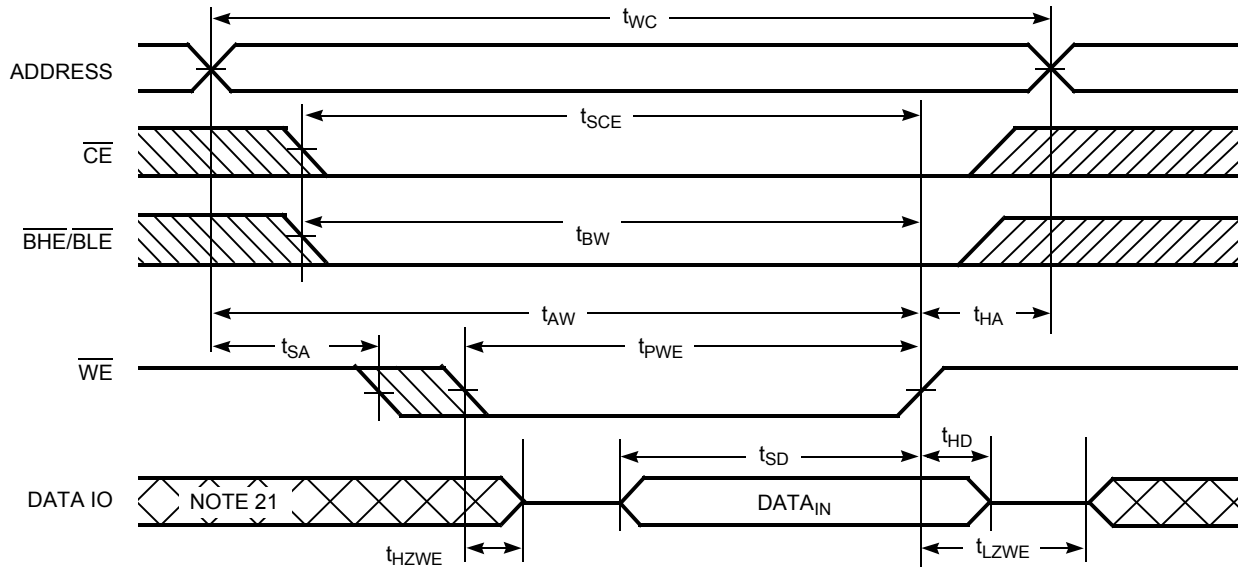
**Notes**

19. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
20. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
21. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

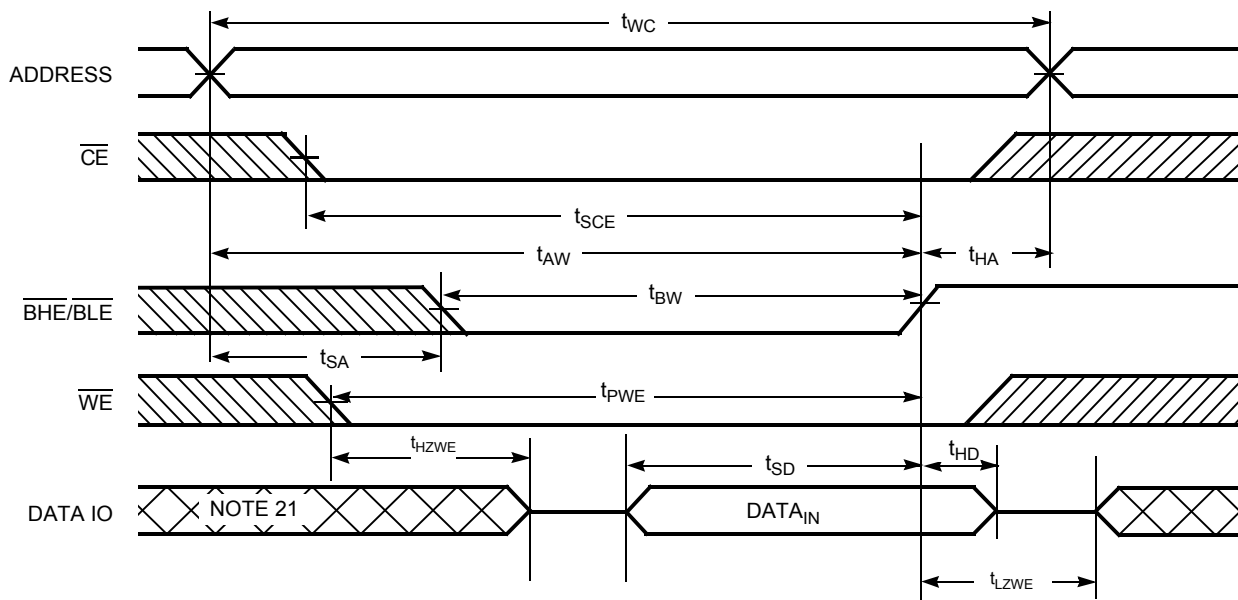
Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[20]</sup>

Figure 7. Write Cycle No. 3



Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[20]</sup>

Figure 8. Write Cycle No. 4





**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power Down	Standby ( $I_{\text{SB}}$ )
L	X	X	H	H	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	L	L	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	H	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_7$ ); $\text{IO}_8\text{--}\text{IO}_{15}$ in High-Z	Read	Active ( $I_{\text{CC}}$ )
L	H	L	L	H	Data Out ( $\text{IO}_8\text{--}\text{IO}_{15}$ ); $\text{IO}_0\text{--}\text{IO}_7$ in High-Z	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	L	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	L	H	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	L	X	L	L	Data In ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	H	L	Data In ( $\text{IO}_0\text{--}\text{IO}_7$ ); $\text{IO}_8\text{--}\text{IO}_{15}$ in High-Z	Write	Active ( $I_{\text{CC}}$ )
L	L	X	L	H	Data In ( $\text{IO}_8\text{--}\text{IO}_{15}$ ); $\text{IO}_0\text{--}\text{IO}_7$ in High-Z	Write	Active ( $I_{\text{CC}}$ )

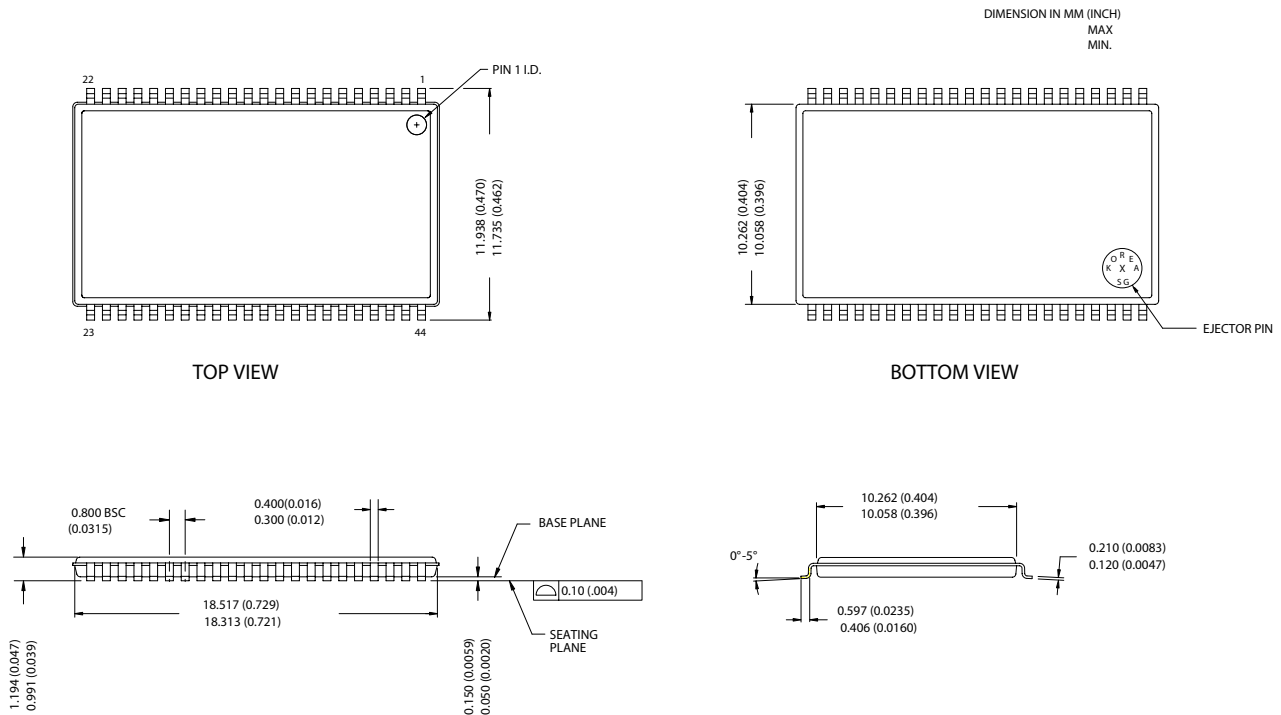
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146ELL-45ZSXI	51-85087	44-pin Thin Small Outline Package II (Pb-free)	Industrial
45	CY62146ELL-45ZSXA	51-85087	44-pin Thin Small Outline Package II (Pb-free)	Automotive-A

Contact your local Cypress sales representative for availability of these parts.

Package Diagram

Figure 9. 44-Pin TSOP II, 51-85087



51-85087-\*A

MoBL is a registered trademark, and More Battery Life is a trademark of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

**Document History Page**

Document Title: CY62146E MoBL <sup>®</sup> , 4-Mbit (256K x 16) Static RAM Document Number: 001-07970				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	463213	See ECN	NXR	New Data Sheet
*A	684343	See ECN	VKN	Added Preliminary Automotive-A Information Updated Ordering Information Table
*B	925501	See ECN	VKN	Added footnote #8 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Added footnote #13 related AC timing parameters
*C	1045260	See ECN	VKN	Converted Automotive-A specs from preliminary to final