DATA SHEET

PCA9551

8-bit I^2C LED driver with programmable blink rates

Product data sheet
Supersedes data of 2003 May 05

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8-bit I²C LED driver with programmable blink rates

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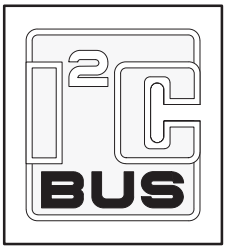


FEATURES

- 8 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.148 Hz and 38 Hz (6.74 and 0.026 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active-LOW reset input
- 8 open drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, HVQFN16

DESCRIPTION

The PCA9551 LED Blinker blinks LEDs in I²C-bus and SMBus applications where it is necessary to limit bus traffic or free up the I²C Master's (MCU, MPU, DSP, chipset, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O Expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I²C-bus and uses up one of the master's timers. The PCA9551 LED Blinker instead requires only the initial set up command to program BLINK RATE 1 and BLINK RATE 2 (i.e., the frequency and duty cycle) for each individual output. From then on, only one command from the bus master is required to turn each individual open drain output ON, OFF, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 100 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The active-LOW hardware reset pin ($\overline{\text{RESET}}$) and Power-On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Three hardware address pins on the PCA9551 allow eight devices to operate on the same bus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-pin plastic SO	–40 °C to +85 °C	PCA9551D	PCA9551D	SOT109-1
16-pin plastic TSSOP	–40 °C to +85 °C	PCA9551PW	PCA9551	SOT403-1
16-pin plastic HVQFN	–40 °C to +85 °C	PCA9551BS	9551	SOT629-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.

PIN CONFIGURATION — SO, TSSOP

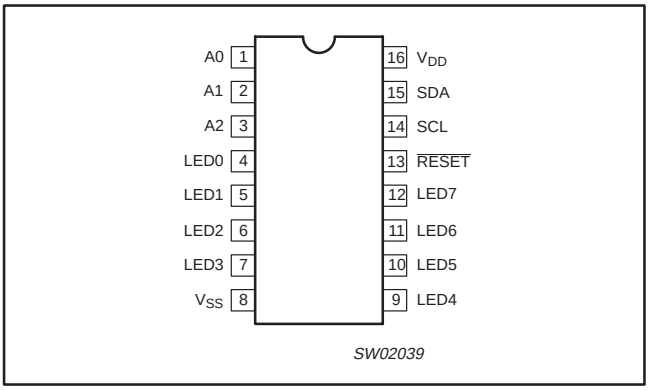


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION — HVQFN

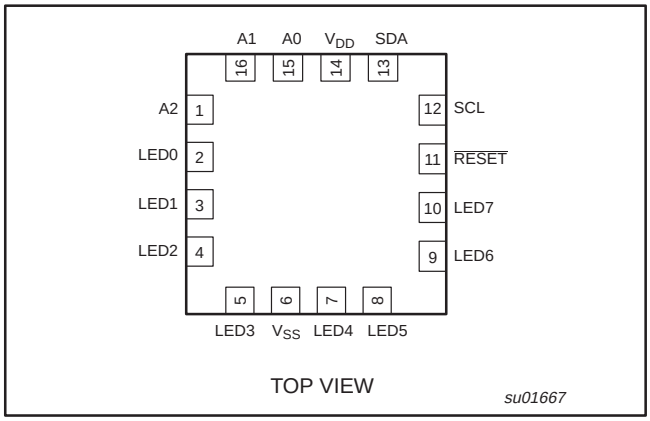


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

SO, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	15	A0	Address input 0
2	16	A1	Address input 1
3	1	A2	Address input 2
4, 5, 6, 7	2, 3, 4, 5	LED0 to LED3	LED drivers 0–3
8	6	V_{SS}	Supply ground
9, 10, 11, 12	7, 8, 9, 10	LED4 to LED7	LED drivers 4–7
13	11	$\overline{\text{RESET}}$	Active-LOW reset input
14	12	SCL	Serial clock line
15	13	SDA	Serial data line
16	14	V_{DD}	Supply voltage

BLOCK DIAGRAM

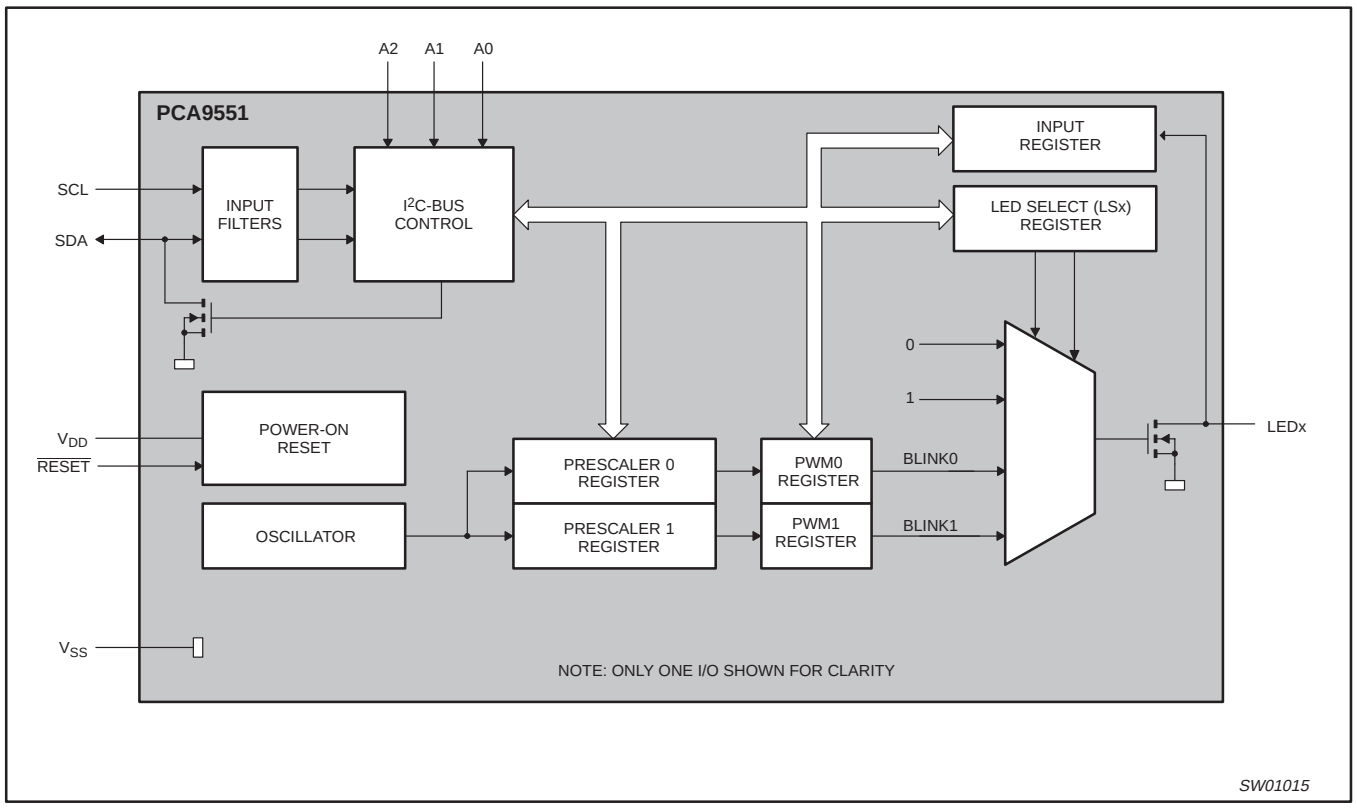


Figure 3. Block diagram

DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9551 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

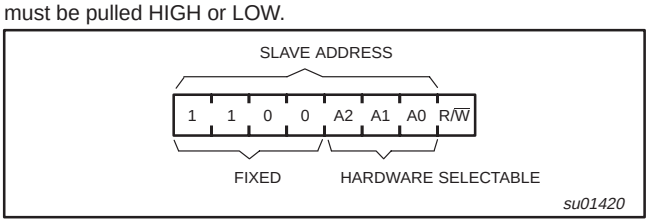


Figure 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9551 which will be stored in the Control Register.

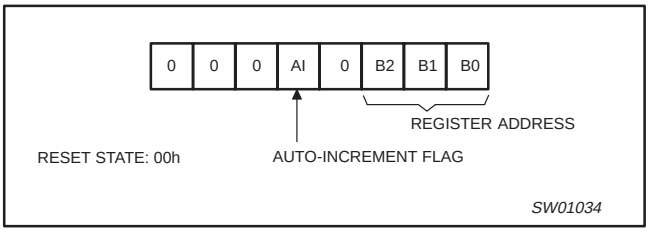


Figure 5. Control register

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag is set, the three low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from '0' (B2 B1 B0 ≠ 0 0 0)

Only the 3 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

CONTROL REGISTER DEFINITION

B2	B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	INPUT	READ	INPUT REGISTER
0	0	1	PSC0	READ/ WRITE	FREQUENCY PRESCALER 0
0	1	0	PWM0	READ/ WRITE	PWM REGISTER 0
0	1	1	PSC1	READ/ WRITE	FREQUENCY PRESCALER 1
1	0	0	PWM1	READ/ WRITE	PWM REGISTER 1
1	0	1	LS0	READ/ WRITE	LED0–LED3 SELECTOR
1	1	0	LS1	READ/ WRITE	LED4–LED7 SELECTOR

REGISTER DESCRIPTION

INPUT — INPUT REGISTER

	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

NOTE: The default value "X" is determined by the externally applied logic level, normally '1' when used for directly driving LED with pull-up to V_{DD}.

PSC0 — FREQUENCY PRESCALER 0[1]

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(\text{PSC0} + 1)}{38}$$

NOTE:

1. Prescaler calculation is different between the PCA9551 and other PCA955x LED Blinkers. A divider ratio of 38 instead of 44 is used. This different divider ratio causes the blinking frequency to be 13% (1 – 38/44) lower when the same 8-bit word is used. The programmed value of the FREQUENCY PRESCALER must be adjusted to compensate for this difference in applications where the PCA9551 is used in conjunction with other PCA955x LED Blinkers and the observed blinking frequencies need to be the same.

PWM0 — PWM REGISTER 0

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM0 register determines the duty cycle of BLINK0. The outputs are HIGH (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

$$\text{The duty cycle of BLINK0 is:} \quad \frac{256 - \text{PWM0}}{256}$$

PSC1 — FREQUENCY PRESCALER 1[1]

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC1 is used to program the period of PWM output.

$$\text{The period of BLINK1} = \frac{(\text{PSC1} + 1)}{38}$$

NOTE:

1. Prescaler calculation is different between the PCA9551 and other PCA955x LED Blinkers. A divider ratio of 38 instead of 44 is used. This different divider ratio causes the blinking frequency to be 13% (1 – 38/44) lower when the same 8-bit word is used. The programmed value of the FREQUENCY PRESCALER must be adjusted to compensate for this difference in applications where the PCA9551 is used in conjunction with other PCA955x LED Blinkers and the observed blinking frequencies need to be the same.

PWM1 — PWM REGISTER 1

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW (LED off).

$$\text{The duty cycle of BLINK1 is:} \quad \frac{256 - \text{PWM1}}{256}$$

LS0 — LED0–3 SELECTOR

	LED 3		LED 2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

LS1 — LED4–7 SELECTOR

	LED 7		LED 6		LED 5		LED 4	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

The LSx LED select registers determine the source of the LED data.

00 = Output is set LOW (LED on)
01 = Output is set Hi-Z (LED off – default)
10 = Output blinks at PWM0 rate
11 = Output blinks at PWM1 rate

PINS USED AS GENERAL PURPOSE I/Os

LED pins not used to control LEDs can be used as general purpose I/Os.

For use as input: Set LEDx to high-impedance (01) and then read the pin state via the input register.

For use as output: Connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LED output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the “LED selector” register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

POWER-ON RESET

When power is applied to V_{DD}, an internal Power-On Reset holds the PCA9551 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9551 registers are initialized to their default states, all the outputs in the off state. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

EXTERNAL RESET

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of t_W. The PCA9551 registers and I²C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

This input requires a pull-up resistor to V_{DD} if no active connection is used.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

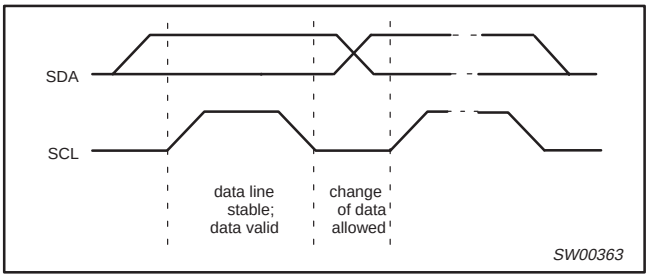


Figure 6. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

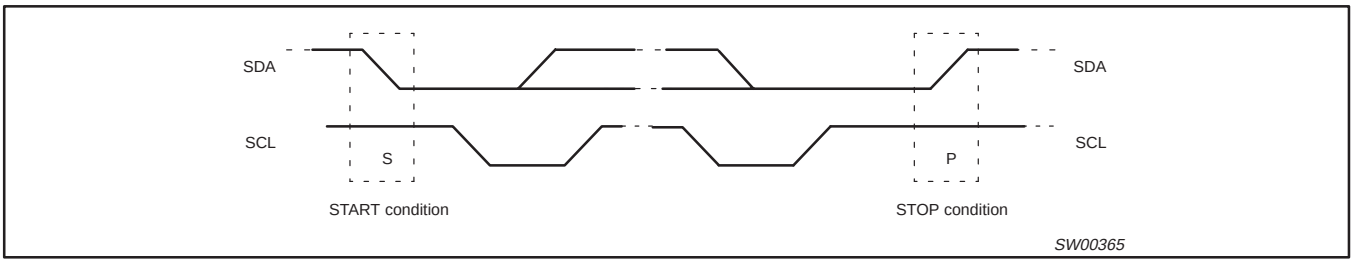


Figure 7. Definition of start and stop conditions

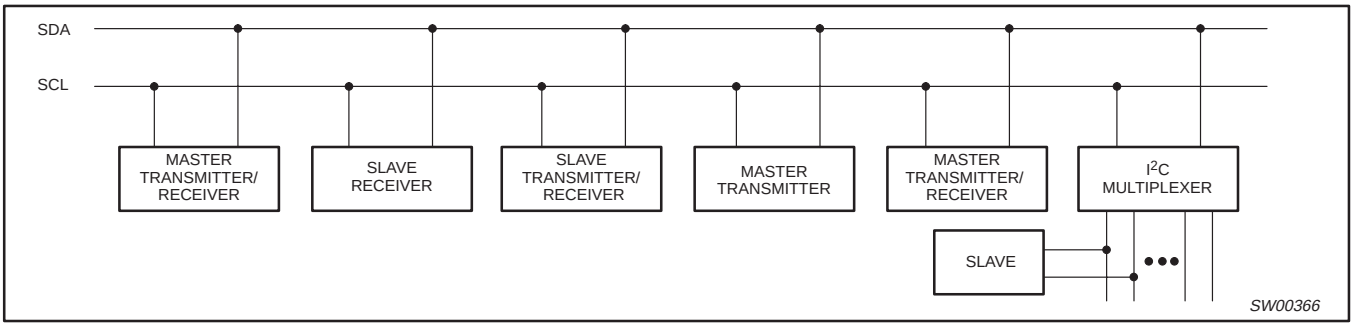


Figure 8. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

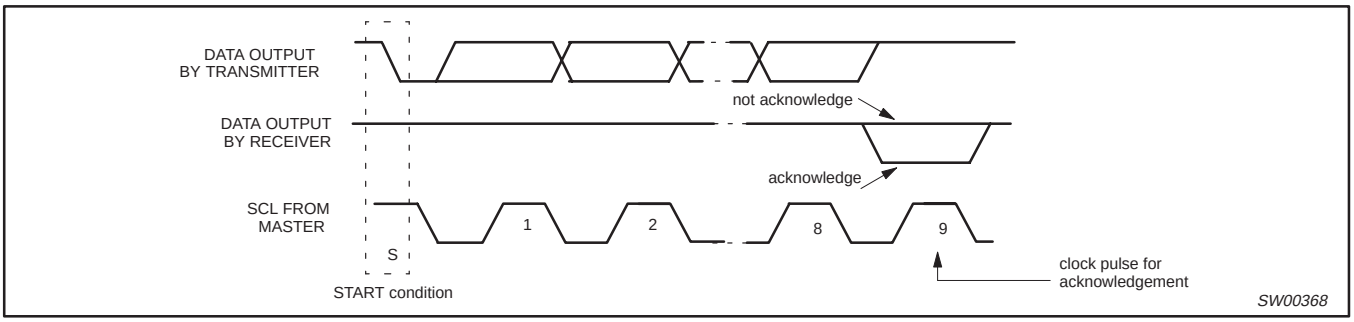


Figure 9. Acknowledgement on the I2C-bus

Bus transactions

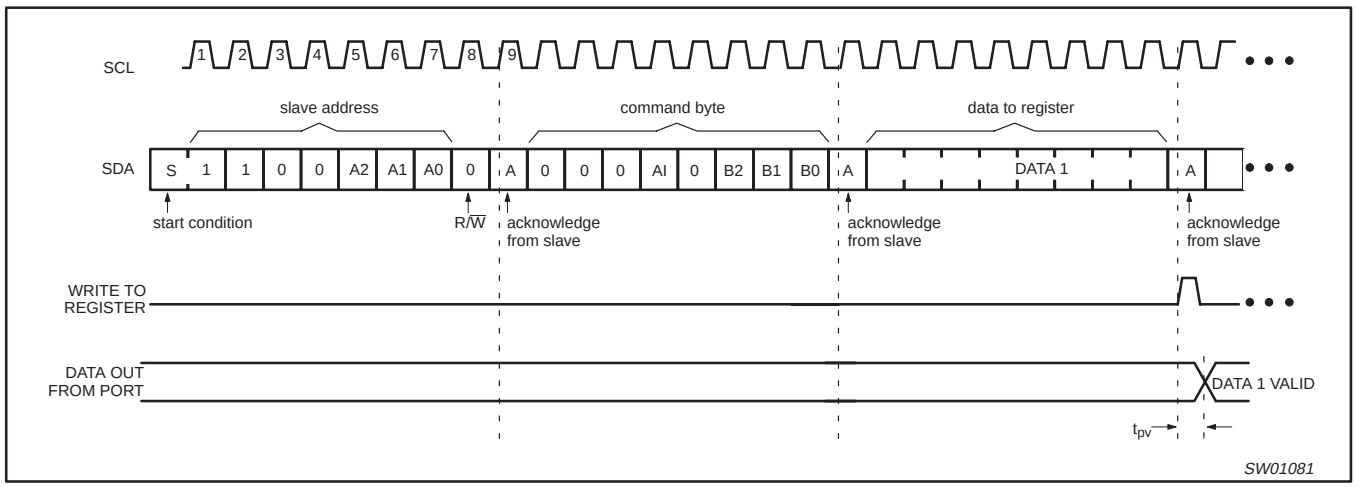


Figure 10. WRITE to register

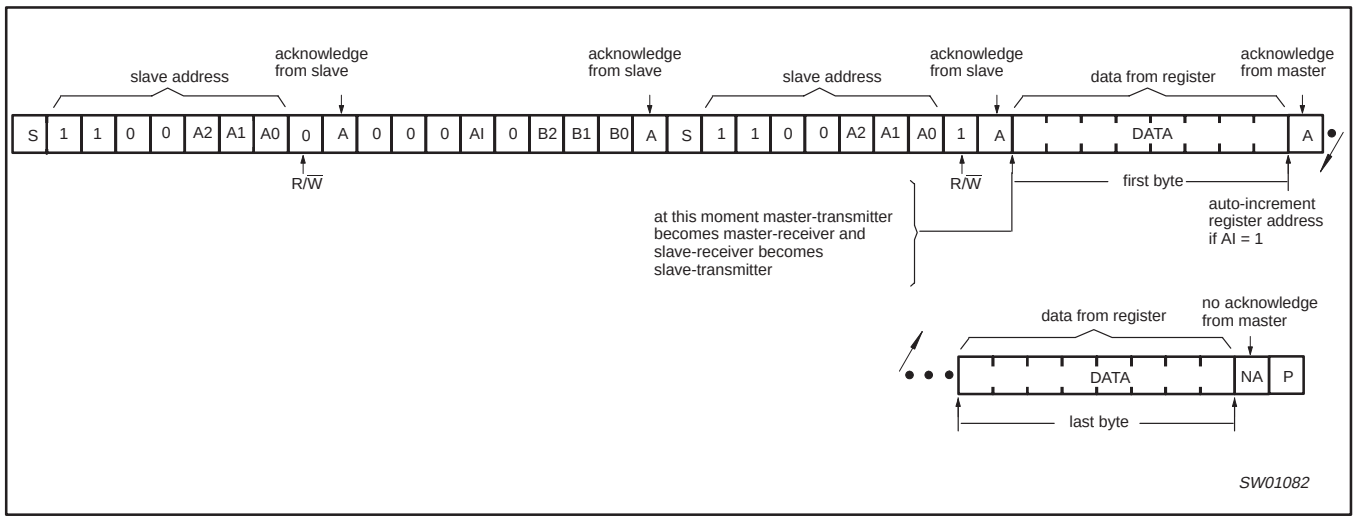
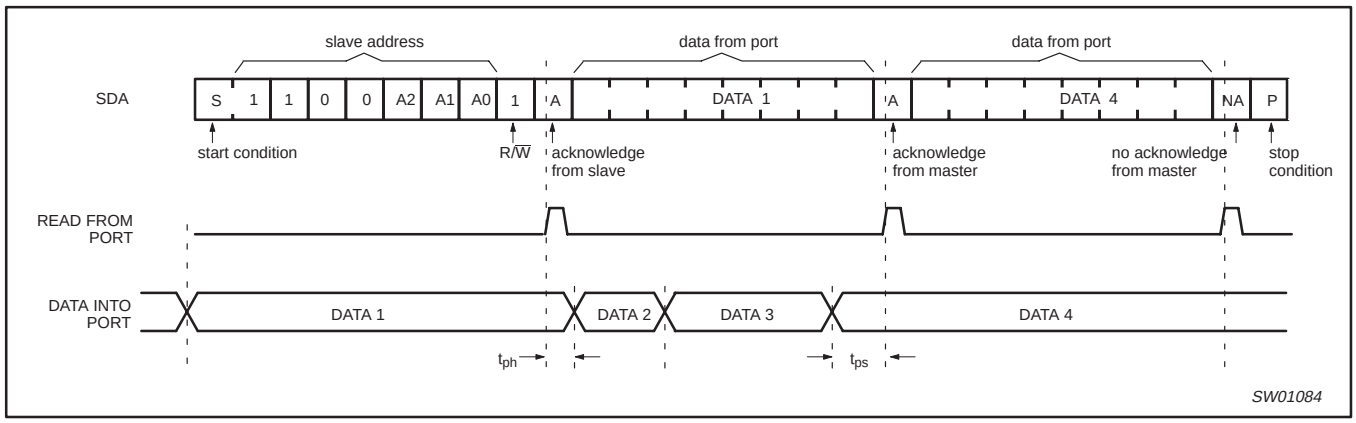


Figure 11. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.

Figure 12. READ input port register

APPLICATION DATA

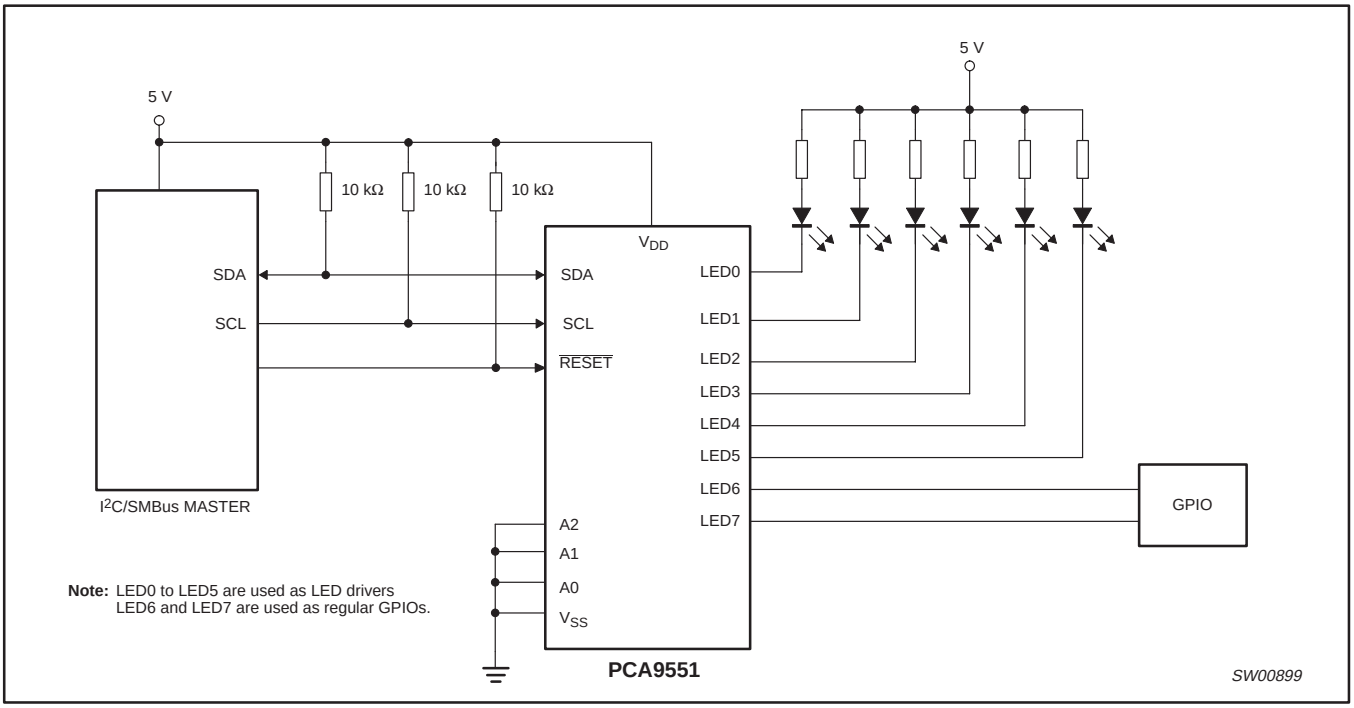


Figure 13. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

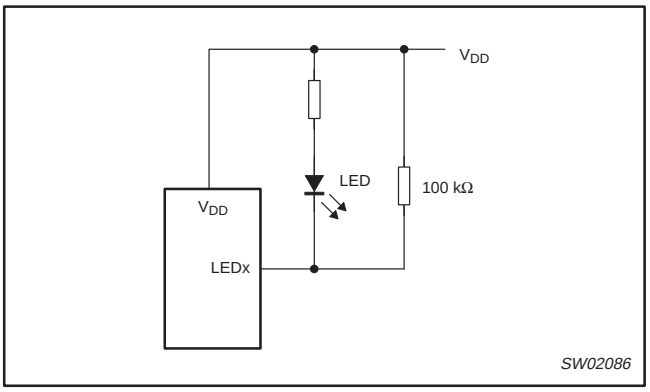


Figure 14. High value resistor in parallel with the LED

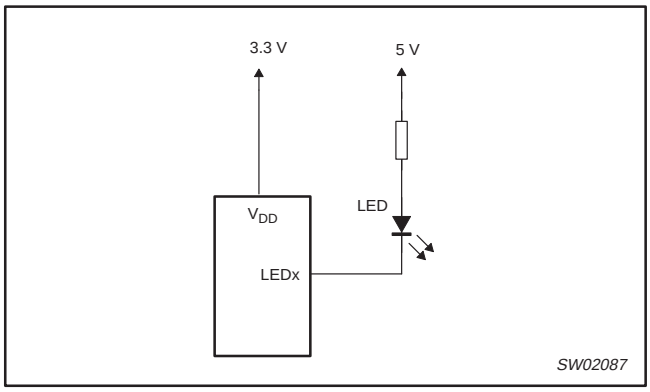


Figure 15. Device supplied by a lower voltage

Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50% duty cycle. LED6 and LED7 will be set to blink at 4 Hz and at a 25% duty cycle.

Table 1.

	I2C-bus
Start	S
PCA9551 address with A0–A2 = LOW	C0h
PSC0 subaddress + auto-increment	11h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{PSC0 + 1}{38}$ PSC0 = 37	25h
Set PWM0 duty cycle to 50%: $\frac{256 - PWM0}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PCS1 to achieve a period of 0.25 seconds: $\text{Blink period} = 0.25 = \frac{PSC1 + 1}{38}$ PSC1 = 9	09h
Set PWM1 output duty cycle to 25%: $\frac{256 - PWM1}{256} = 0.25$ PWM1 = 192	C0h
Set LED0 to LED3 on	00h
Set LED4 and 5 to PWM0, and LED6 or 7 to PWM1	FAh
Stop	P

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
$V_{I/O}$	DC voltage on an I/O		V_{SS} – 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±25	mA
I_{SS}	Supply current		—	100	mA
P_{tot}	Total power dissipation		—	400	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	—	350	500	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz	—	1.9	3.0	µA
ΔI_{DD}	Additional standby current	Standby mode; V_{DD} = 5.5 V; Every LED I/O at V_{IN} = 4.3 V; f_{SCL} = 0 kHz	—	—	800	µA
V_{POR}	Power-on reset voltage (Note 1)	No load; V_I = V_{DD} or V_{SS}	—	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	6.5	—	mA
I_L	Leakage current	V_I = V_{DD} = V_{SS}	–1	—	+1	µA
C_I	Input capacitance	V_I = V_{SS}	—	3.7	5	pF
I/Os						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V; Note 2	6	9	—	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V; Note 2	8	11	—	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V; Note 2	10	14	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 2	11	14	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 2	14	18	—	mA
		V_{OL} = 0.7 V; V_{DD} = 5.0 V; Note 2	17	24	—	mA
I_L	Input leakage current	V_{DD} = 3.6 V; V_I = 0 or V_{DD}	–1	—	1	µA
C_{IO}	Input/output capacitance		—	2.1	5	pF
Select Inputs A0, A1, A2 / $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage; A0 / $\overline{\text{RESET}}$		2.0	—	5.5	V
V_{IH}	HIGH-level input voltage; A1 / A2		2.0	—	V_{DD} + 0.5	V
I_{LI}	Input leakage current		–1	—	1	µA
C_I	Input capacitance	V_I = V_{SS}	—	2.3	5	pF

NOTES:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition set-up time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	—	600	—	600	ns
$t_{VD;DAT}$ (L)	Data out valid time[3]	—	600	—	600	ns
$t_{VD;DAT}$ (H)	Data out valid time[3]	—	1500	—	600	ns
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data set-up time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Reset						
t_W	Reset pulse width	6	—	6	—	ns
t_{REC}	Reset recovery time	0	—	0	—	ns
t_{RESET}[4,5]	Time to reset	400	—	400	—	ns

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
4. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
5. Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

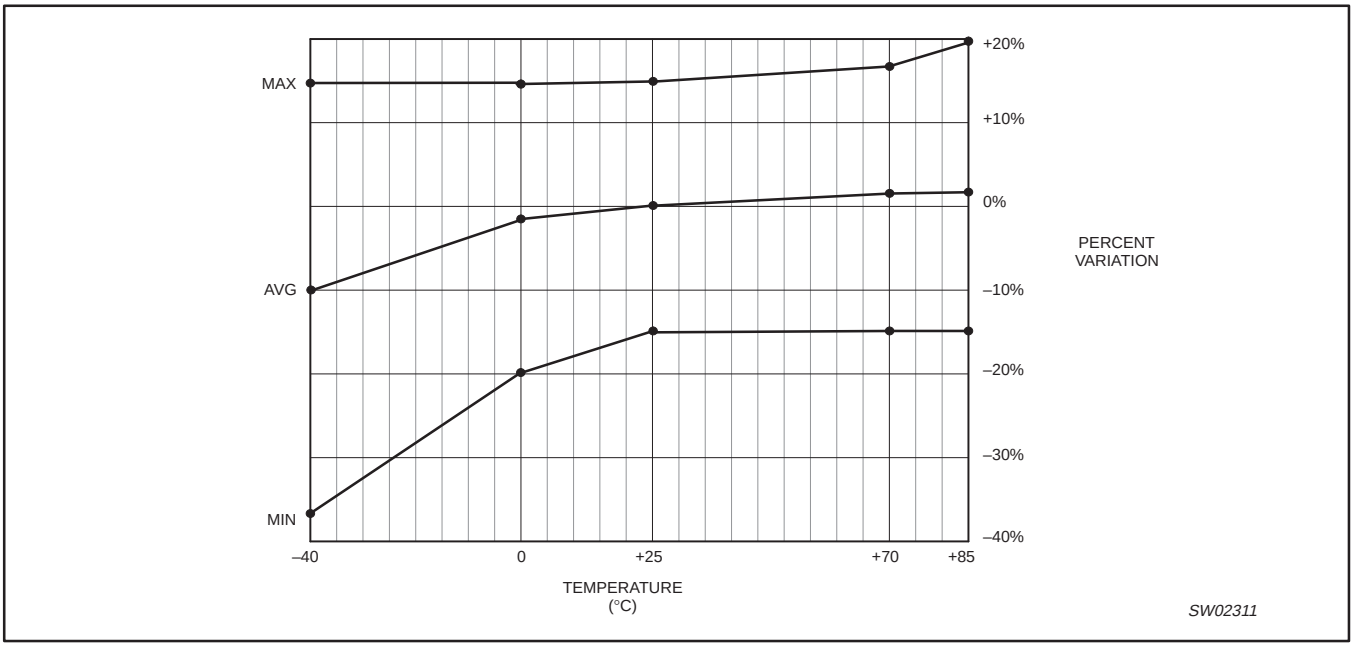


Figure 16. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V

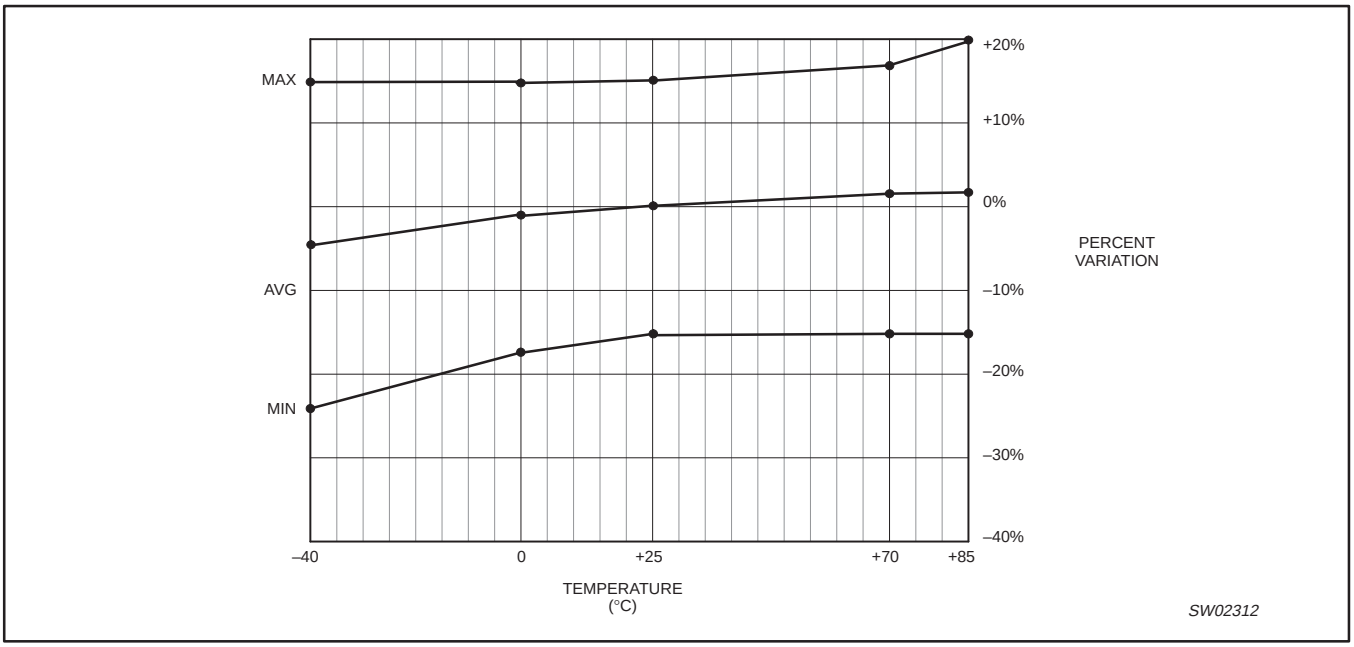


Figure 17. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

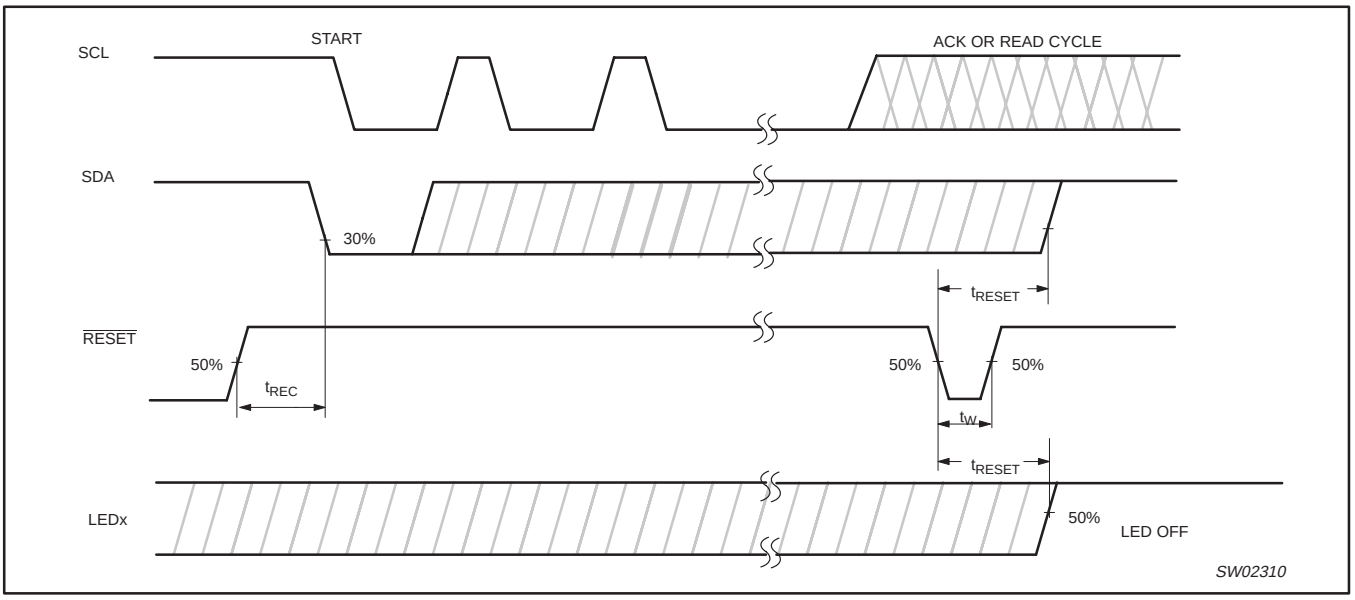


Figure 18. Definition of $\overline{\text{RESET}}$ timing

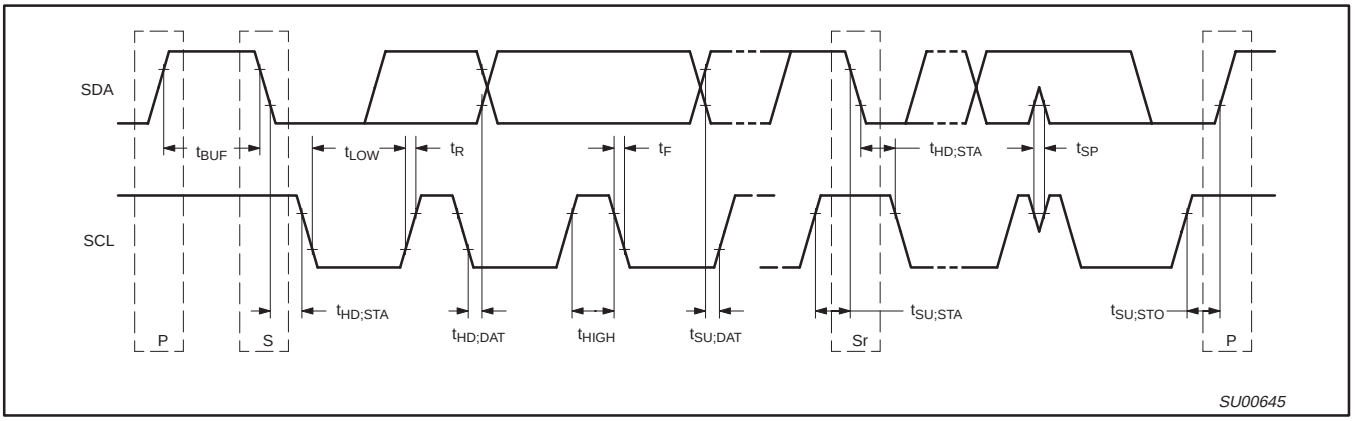


Figure 19. Definition of timing

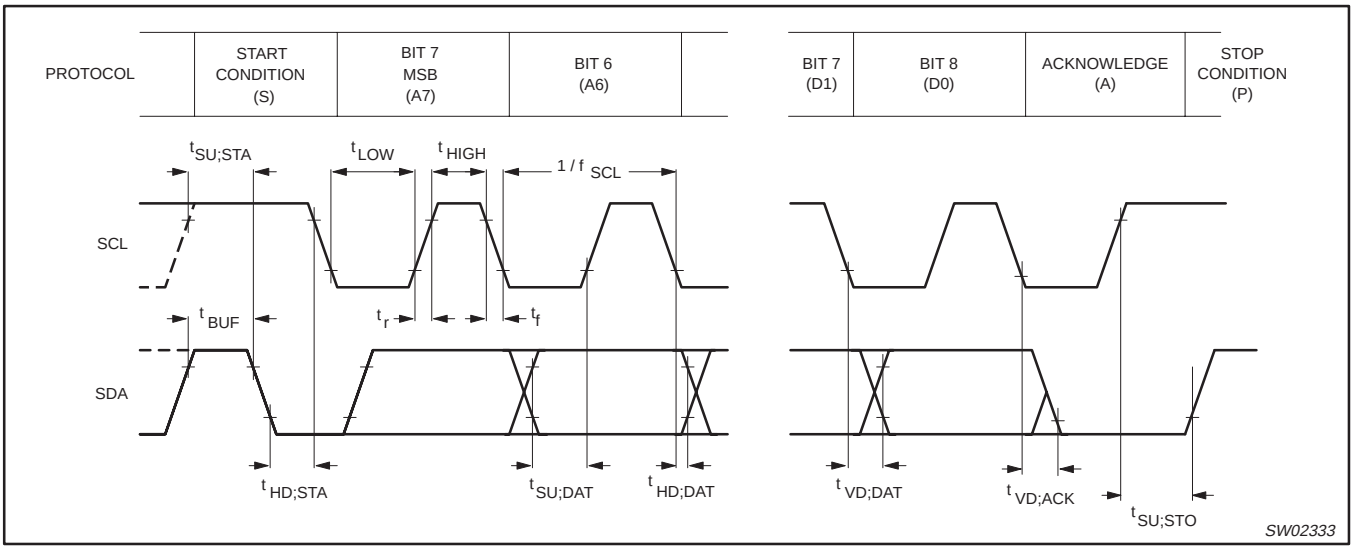
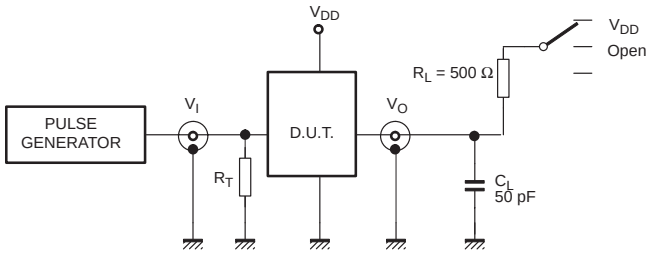


Figure 20. I2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}



DEFINITIONS

R_L = Load resistor FOR LEDN. R_L FOR SDA AND SCL > 1 kΩ (3 mA or less current).

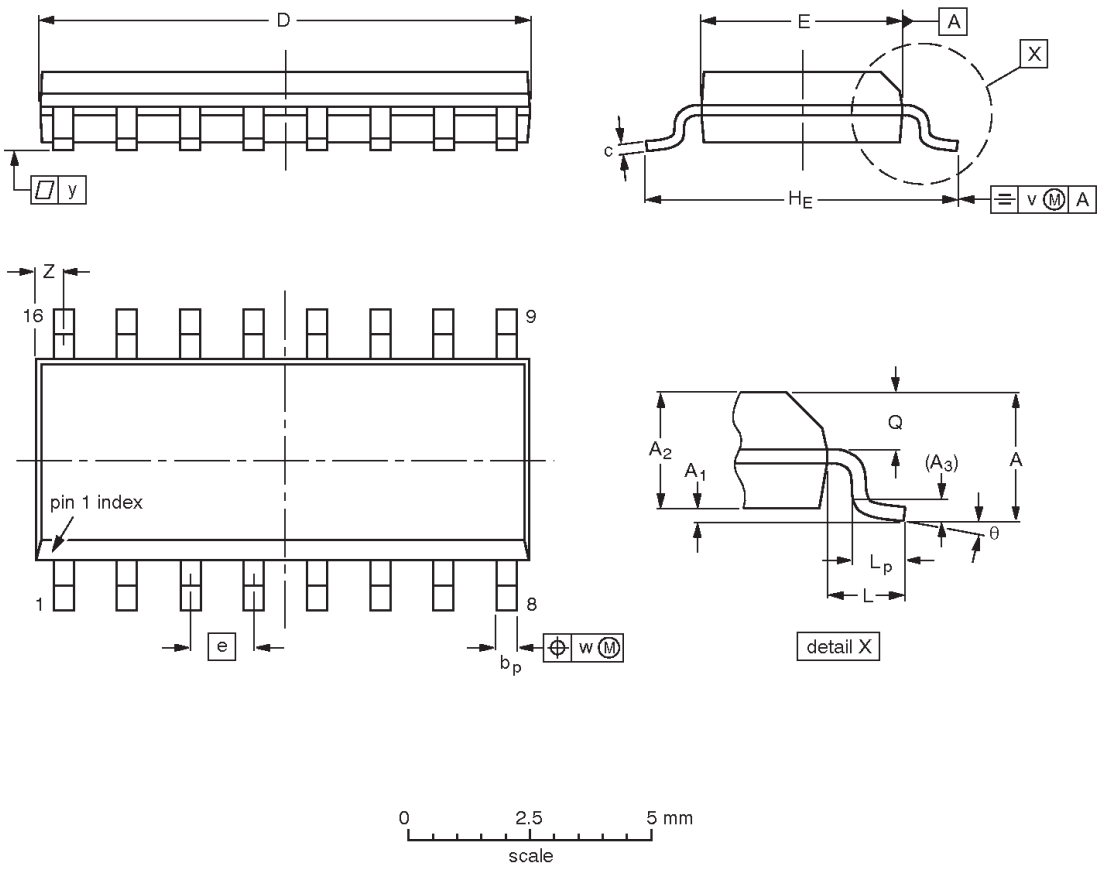
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02334

Figure 21. Test circuitry for switching times

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

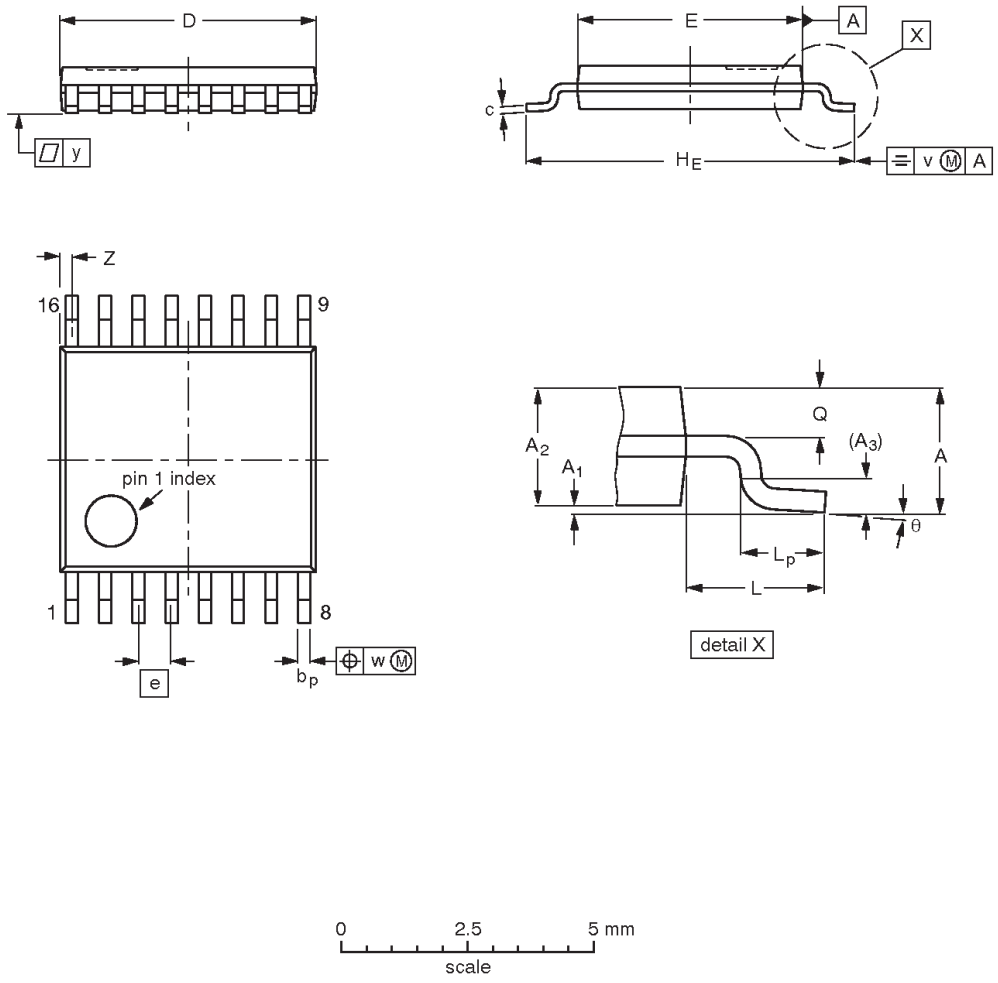
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

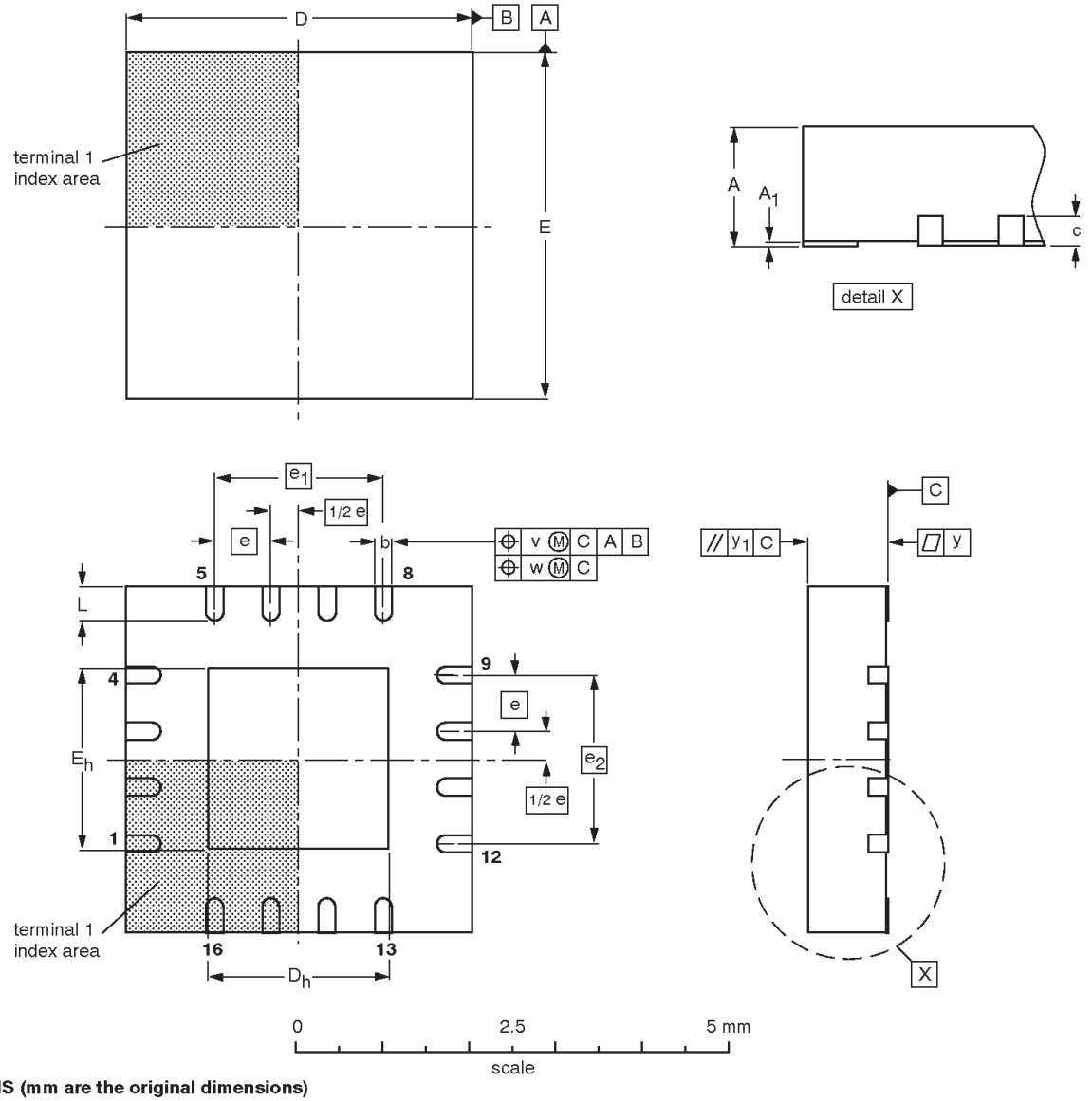
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_5	20041001	**Product data sheet (9397 750 13726). Supersedes data of 2003 May 05 (9397 750 11462).** Modifications: ● "Features" section on page 2: – second bullet: change from "... between 0.15625 and 40 Hz (6.4 and 0.025 seconds)" to "... between 0.148 Hz and 38 Hz (6.74 and 0.026 seconds)" ● "Register description" section on page 5: – section "PCS0—Frequency Prescaler 0": remove "... and PCA953x LED Dimmers" from Note 1 (2 places). – section "PCS1—Frequency Prescaler 1": remove "... and PCA953x LED Dimmers" from Note 1 (2 places). ● Add note to section "Input—Input Register" on page 5 ● Add section "Pins used as General Purpose I/Os" on page 6. ● Section "Power-on Reset" on page 6 re-written. ● Section "External Reset" on page 6: second paragraph changed from "This input requires a pull-up resistor to V_{DD}." to "This input requires a pull-up resistor to V_{DD} if no active connection is used.". ● Figure 13 on page 10: add resistor values ● DC Characteristics table on page 12: add (new) Note 1 and its reference at V_{POR}. ● Add Figures 20 and 21.
_4	20030505	**Product data (9397 750 11462); ECN 853-2343 29858 dated 24 April 2003. Supersedes data of 24 February 2003 (9397 750 11155).**
_3	20030224	**Product data (9397 750 11155); ECN 853-2343 29331 of 20 December 2002; supersedes data of 2002 Sep 09 (9397 750 10328).**
_2	20020927	**Product data (9397 750 10328); ECN 853-2343 28878 of 09 September 2002.**

8-bit I²C LED driver with programmable blink rates PCA9551

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