PWR-INT100

Half-Bridge Driver IC

Low-Side and High-side Drive with Simultaneous Conduction Lockout

POWER INTEGRATIONS, INC.®

Product Highlights

5 V CMOS Compatible Control Inputs
- Combines logic inputs for low and high-side drives
- Schmidt-triggered inputs for noise immunity

Built-in High-voltage Level Shifters
- Can withstand up to 800 V for direct interface to the HV-referenced high-side switch
- Pulsed internal high-voltage level shifters reduce power consumption

Gate Drive Outputs for External MOSFETs
- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gates at up to 15 V
- External MOSFET allows flexibility in design for various motor sizes

Built-in Protection Features
- Simultaneous conduction lockout protection
- Undervoltage lockout

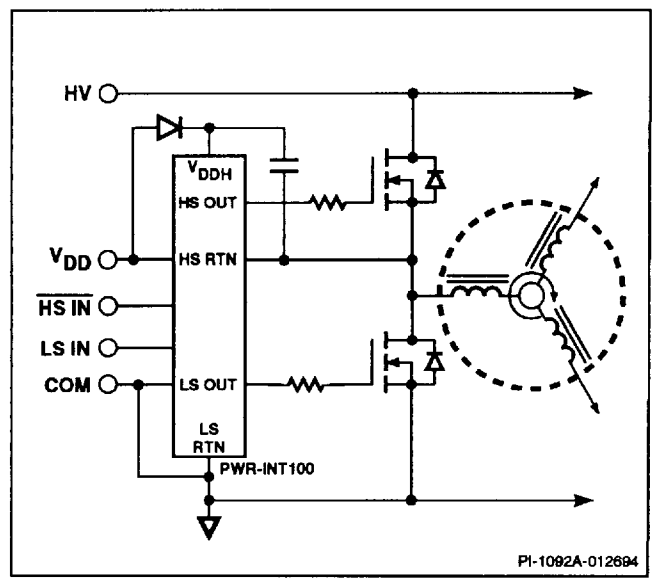


Figure 1. Typical Application

Description

The PWR-INT100 half-bridge driver IC provides gate drive for external low- and high-side MOSFET switches. The PWR-INT100 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads. The PWR-INT100 is designed to be used with rectified 110 V or 220 V supplies. Both high-side and low-side switches can be controlled independently from ground-referenced 5 V logic inputs.

Built-in protection logic prevents both switches from turning on at the same time and shorting the high voltage supply. Pulsed internal level shifting saves power and provides enhanced noise immunity. The circuit is powered from a nominal 15 V supply to provide adequate gate drive for external N-channel MOSFETs. A floating high-side supply is derived from the low-voltage rail by using a simple bootstrap technique.

Applications for the PWR-INT100 include motor drives, electronic ballasts, and uninterruptible power supplies. Multiple devices can also be used to implement full- bridge and multi-phase configurations.

The PWR-INT100 is available in a 16-pin plastic SOIC package.

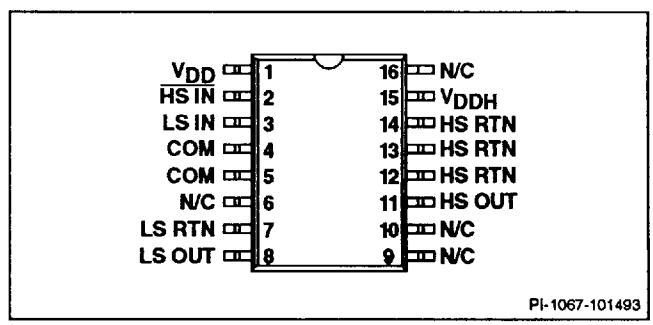


Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	ISOLATION VOLTAGE
PWR-INT100TNI	16-pin SOIC	800 V

411 Clyde Avenue
Business Phone: (415) 960-3572
Applications Hotline: (800) 552-3155
FAX: (800) 468-0809 In CA: (415) 940-1541

PRELIMINARY

January 1994

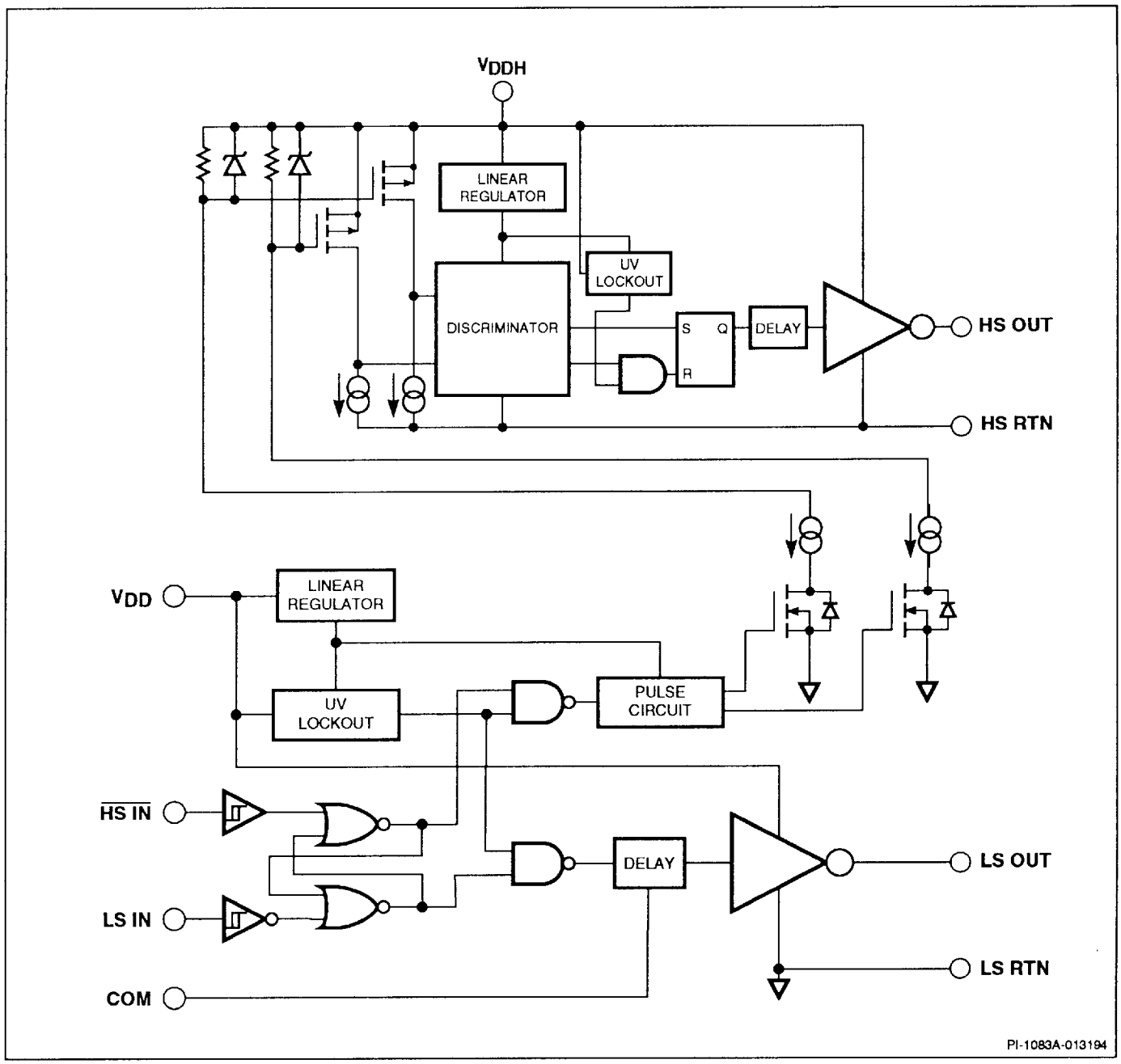


Figure 3. Functional Block Diagram of the PWR-INT100

Pin Functional Description

Pin 1:
V_{DD} supplies power to the logic, high-side interface, and low-side driver.

Pin 2:
Active-low logic level input $\overline{\text{HS IN}}$ controls the high-side driver output.

Pin 3:
Active-high logic level input **LS IN** controls the low-side driver output.

Pin 4, 5:
COM connection is used as the analog reference point for the circuit.

Pin 7:
LS RTN is the power reference point for the low-side circuitry, and should be connected to the source of the low-side MOSFET and to the COM pin.

Pin 8:
LS OUT is the driver output which controls the low-side MOSFET.

Pin 11:
HS OUT is the driver output which controls the high-side MOSFET.

Pin 12,13,14:
HS RTN is the power reference point for the high-side circuitry, and should be connected to the source of the high-side MOSFET.

Pin 15:
V_{DDH} supplies power to the high-side control logic and output driver. This is normally connected to a high-side referenced bootstrap circuit or can be supplied from a separate floating power supply.

PWR-INT100 Functional Description

5 V Regulators
Both low- and high-side driver circuits incorporate a 5 V linear regulator circuit. The low-side regulator provides the supply voltage for the control logic and high-voltage level shift circuit. This allows $\overline{\text{HS IN}}$ and LS IN to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply. The high-side regulator provides the supply voltage for the noise rejection circuitry and high-side control logic.

Undervoltage Lockout
The undervoltage lockout circuit for the low-side driver disables both the LS OUT and HS OUT pins whenever the V_{DD} power supply falls below 9.25 V, and maintains this condition until the V_{DD} power supply rises above 9.5 V. This guarantees that both MOSFETs will remain off during power-up or fault conditions.

The undervoltage lockout circuit for the high-side driver disables the HS OUT pin whenever the V_{DDH} power supply falls below 9.25 V, and maintains this condition until the V_{DDH} power supply rises above 9.5 V. This guarantees that the high-side MOSFET will be off during power-up or fault conditions.

Level Shift
The level shift control circuitry of the low-side driver is connected to integrated high-voltage N-channel MOSFET transistors which perform the level-shifting function for communication to the high-side driver. Controlled current capability allows the drain voltage to float with the high-side driver. Two individual channels produce a true differential communication channel for accurately controlling the high-side driver in the presence of fast moving high-voltage waveforms. The high voltage level shift transistors employed exhibit very low output capacitance, minimizing the displacement currents between the low-side and high-side drivers during fast moving voltage transients created during switching of the external MOSFETs. As a result, power dissipation is minimized and noise immunity optimized.

The pulse circuit provides the two high-voltage level shifters with precise timing signals. These signals are used by the discriminator to reject spurious noise. The combination of differential communication with the precise timing provides maximum immunity to noise.

Simultaneous Conduction Lockout
A latch prevents the low-side driver and high-side driver from being on at the same time, regardless of the input signals.

Delay Circuit
The delay circuit matches the low-side propagation delay with the combination of the pulse circuit, high voltage level shift, and high-side driver propagation delays. This ensures that the low-side driver and high-side driver will never be on at the same time during switching transitions in either direction.

Driver
The CMOS drive circuitry on both low-side and high-side driver ICs provide drive power to the gates of the external MOSFETs. The drivers consist of a CMOS buffer capable of driving external transistor gates at up to 15 V.

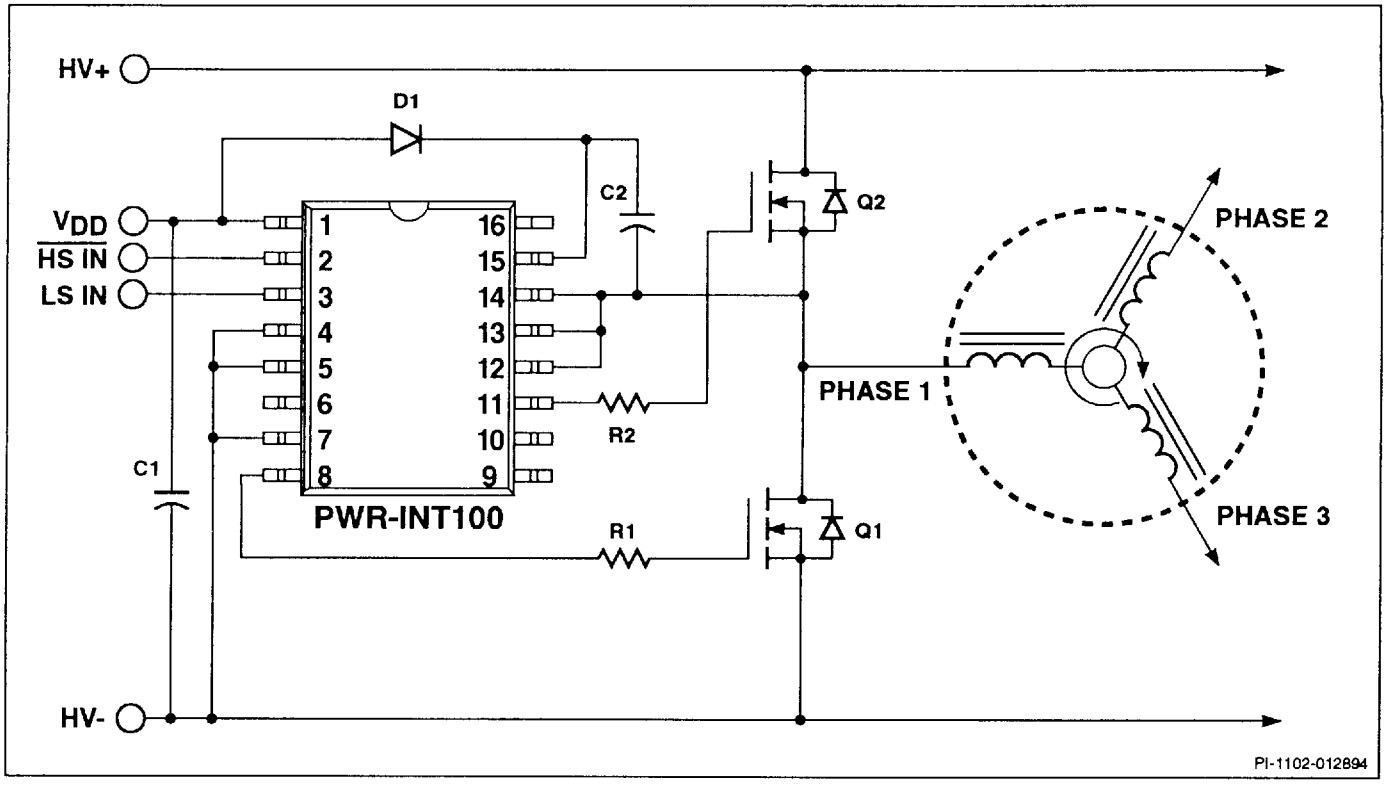


Figure 4. Using the PWR-INT100 in a 3-phase Configuration.

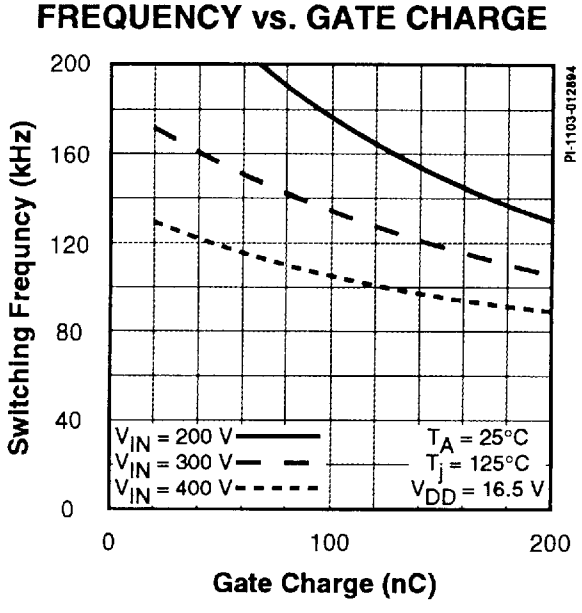


Figure 5. Gate Charge versus Switching Frequency.

General Circuit Operation

One phase of a three-phase motor drive circuit is shown in Figure 4 to illustrate an application of the PWR-INT100. The LS IN signal directly controls MOSFET Q1. The $\overline{\text{HS IN}}$ signal controls MOSFET Q2 via the high voltage level shift transistors communicating with the high-side driver. The PWR-INT100 will ignore input signals that would command both Q1 and Q2 to conduct simultaneously, protecting against shorting the HV+ bus to HV-.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to V_{DD}. Normal CMOS power supply sequencing should be observed. The order of signal application should be V_{DD}, logic signals, and then HV+.

The output returns (HS RTN and LS RTN) are isolated from one another by the internal high-voltage MOSFET level shifters. The level shift circuitry is designed to operate properly even when the HS RTN swings as much as 5 V below the LS RTN pin with V_{DDH} biased at 15 V. The PWR-INT100 will also safely tolerate more negative voltages (as low as $-V_{DDH}$ below LS RTN).

Maximum frequency of operation is limited by power dissipation due to high-voltage switching, gate charge, and bias power. Figure 5 indicates the maximum switching frequency as a function of input voltage and gate charge. For higher ambient temperatures, the switching frequency should be derated linearly.

The bootstrap capacitor must be large enough to provide bias current over the entire on-time of the high-side driver without significant voltage sag or decay. The high-side MOSFET gate charge must also be supplied at the desired switching frequency. Figure 6 shows the maximum high-side on-time versus gate charge of the external MOSFET. Applications with extremely long high-side on times require special techniques discussed in AN-10.

The high-side driver is latched on and off by the edges of the appropriate low-side logic signal. The high-side driver will latch off and stay off if the bootstrap capacitor discharges below the undervoltage lockout threshold. Undervoltage lockout-induced turn off can occur during conditions such as power ramp up, motor start, or low speed operation.

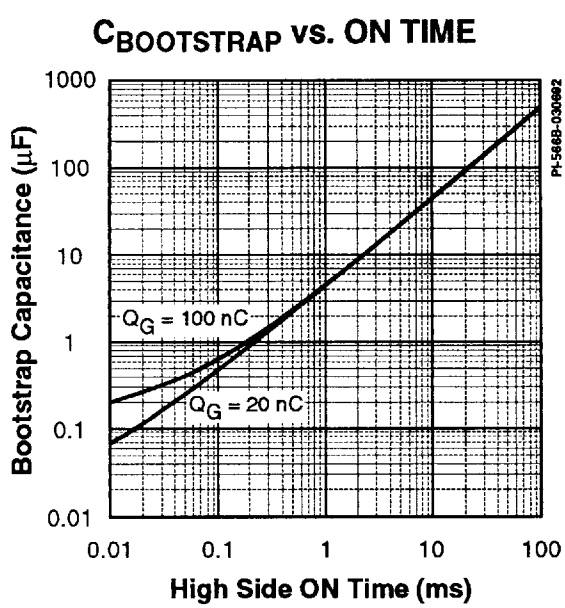


Figure 6. High-side On Time versus Bootstrap Capacitor.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} Voltage ..... 16.5 V
V_{DDH} Voltage ..... HS RTN + 16.5 V
HS RTN ..... 800 V - V_{DDH} to -V_{DDH}
Logic Input Voltage ..... -0.3V to 5.5 V
LS OUT Voltage ..... LS RTN - 0.3 V to V_{DD} + 0.3 V
HS OUT Voltage ..... HS RTN - 0.3 V to V_{DDH} + 0.3 V
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... -40 to 85°C

Junction Temperature ..... 150°C
Lead Temperature[2] ..... 260°C
Power Dissipation (T_A = 250°C) ..... 1.0 W
(T_A = 70°C) ..... 800 mW
Thermal Impedance (θ_{JA}) ..... 55°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DDH} = V_{DD} = 15 V, HS RTN = LS RTN = COM = 0 V, T_A = -40 to 85°C		Test Limits MIN	TYP	MAX	Units
LOGIC							
Input Current, High or Low	I_{IH}, I_{IL}	V_{IH} = 4.0 V		0	10	150	µA
		V_{IL} = 1.0 V		-20	0	20	
Input Voltage High	V_{IH}			4.0	3.0		V
Input Voltage Low	V_{IL}				2.3	1.0	V
Input Voltage Hysteresis	V_{HY}			0.3	0.7		V
LS OUT/HS OUT							
Output Voltage High	V_{OH}	I_o = -20 mA	LS OUT	V_{DD}-1.0	V_{DD}-0.5		V
			HS OUT	V_{DDH}-1.0	V_{DDH}-0.5		
Output Voltage Low	V_{OL}	I_o = 40 mA			0.3	1.0	V
Output Short Circuit Current	I_{OS}	See Note 1	V_o = 0 V	-150			mA
			V_o = 15 V	300			
Turn-on Delay Time	$t_{d(on)LS}$	See Figure 7	LS OUT		0.6	1	µs
	$t_{d(on)HS}$		HS OUT		1.0	1.5	
Rise Time	t_r	See Figure 7			80	120	ns
Turn-off Delay Time	$t_{d(off)LS}$	See Figure 7	LS OUT		500	1000	ns
	$t_{d(off)HS}$		HS OUT		420	600	
Fall Time	t_f	See Figure 7			50	100	ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DDH} = V_{DD} = 15 V, HS RTN = LS RTN = COM = 0 V, T_A = -40 to 85°C	Test Limits			Units
			MIN	TYP	MAX	
LEVEL SHIFT						
Breakdown Voltage	BV_{DSS}	V_{DDH} = HS OUT = HS RTN, $I_{HS\ RTN}$ = 250 µA	800			V
Leakage Current	$I_{HSD(OFF)}$	V_{DDH} = HS OUT = HS RTN = 500 V		0.1	15	µA
Interface Capacitance		V_{DDH} = HS OUT = HS RTN = 500 V		20		pF
SYSTEM RESPONSE						
Deadtime (Low Off to High On)	Dt_{P+}	See Figure 8	0	450		ns
Deadtime (High Off to Low On)	Dt_{P-}	See Figure 8	0	300		ns
UNDERVOLTAGE LOCKOUT						
Input UV Trip-off Voltage			8.5	9.25	10	V
Input UV Hysteresis			175	350		mV
SUPPLY						
Supply Current	I_{DD}, I_{DDH}			1.5	3.0	mA
Supply Voltage	V_{DD}, V_{DDH}		10		16	V

NOTES:

1. Applying a short circuit to the LS OUT or HS OUT pin for more than 500 µs will exceed the thermal rating of the package, resulting in destruction of the part.

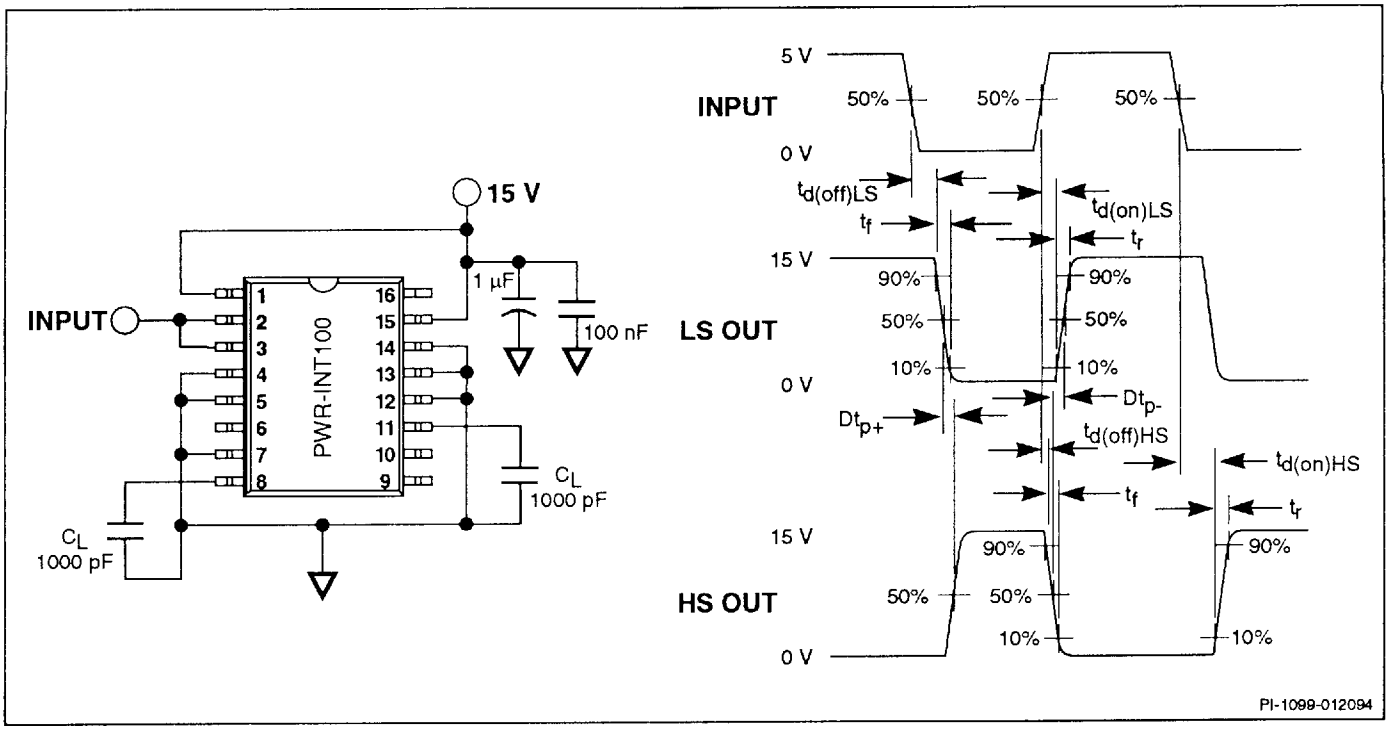
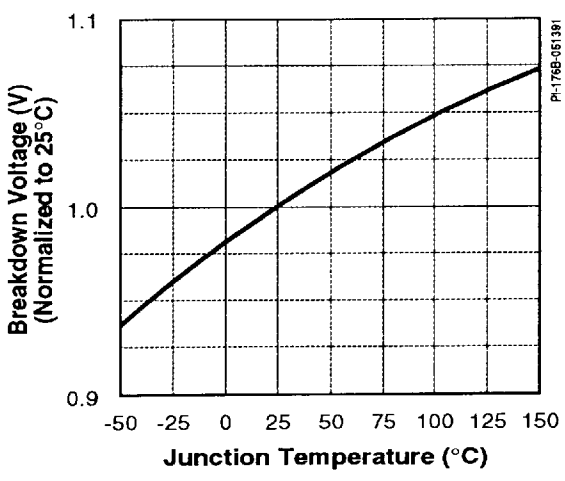
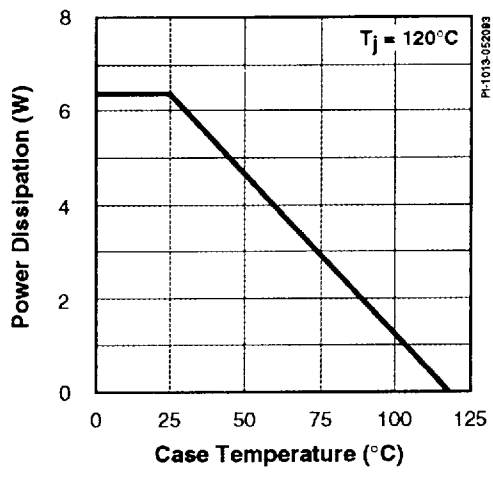


Figure 7. Switching Time/Deadtime Test Circuit.

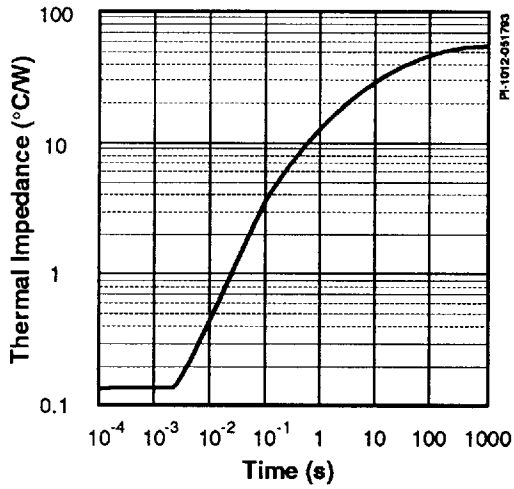
BREAKDOWN vs. TEMPERATURE



PACKAGE POWER DERATING

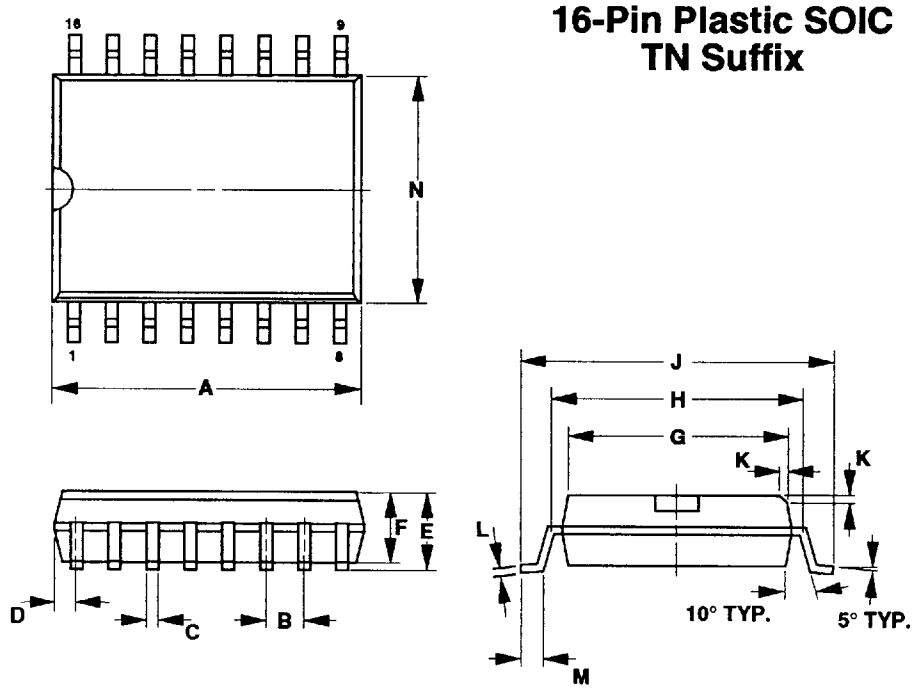


TRANSIENT THERMAL IMPEDANCE



DIM	Inches	mm
A	.405-.409	10.287-10.387
B	.048-.052	1.219-1.321
C	.014-.018	.356-.457
D	.027-.031	.686-.787
E	.99-.101	.2.514-2.565
F	.090-.094	2.286-2.388
G	.293-.297	7.442-7.544
H	.326-.330	8.280-8.382
J	.404-.408	10.262-10.363
K	.015 TYP	.381 TYP
L	.008-.012	.203-.305
M	.030-.034	.762-.864
N	.297-.301	7.544-7.645

16-Pin Plastic SOIC
TN Suffix



PO-010-022791