

Synchronous Buck PWM DC-DC Controller

Description

The FP6329/A is designed to drive two N-channel MOSFETs in a synchronous rectified buck topology. It provides the output adjustment, internal soft-start, frequency compensation networks, monitoring and protection functions into a single package.

The FP6329/A operating at fixed 300/600kHz frequency provides simple, single feedback loop, voltage mode control with fast transient response. The resulting PWM duty ratio ranges from 0-100%.

The FP6329/A features over current protection. The output current is monitored by sensing the voltage drop across the R_{DS-ON} of the low side MOSFET which eliminates the need for a current sensing resistor.

This device is available in SOP-8 package.

Features

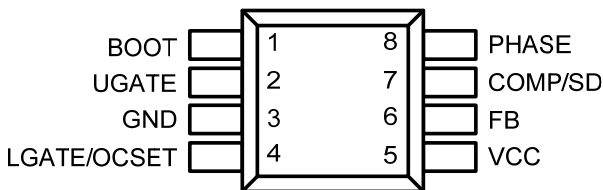
- Operates from +5V or +12V
- High Output Current
- Drives Two Low Cost N-Channel MOSFETs
- Fast Transient Response
- Simple Single-Loop Control Design (Voltage-Mode PWM Control)
- Internal Soft-Start
- Over-Current Protection
- Over-Voltage Protection
- Under-Voltage Protection
- SOP-8 Package
- RoHS Compliant

Applications

- Motherboard
- Graphic Card
- Telecomm Equipments
- High Power DC-DC Regulators
- Switching Power Supply (SPS)

Pin Assignment

SO Package (SOP-8)



SP Package (SOP-8<Exposed Pad>)

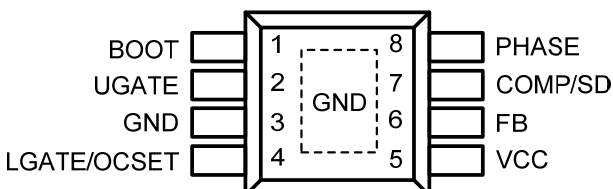
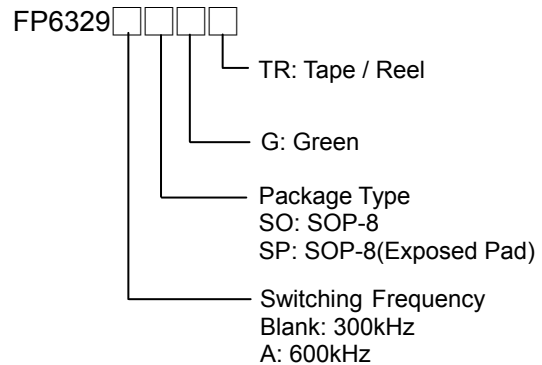


Figure 1. Pin Assignment of FP6329/A

Ordering Information



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Typical Application Circuit

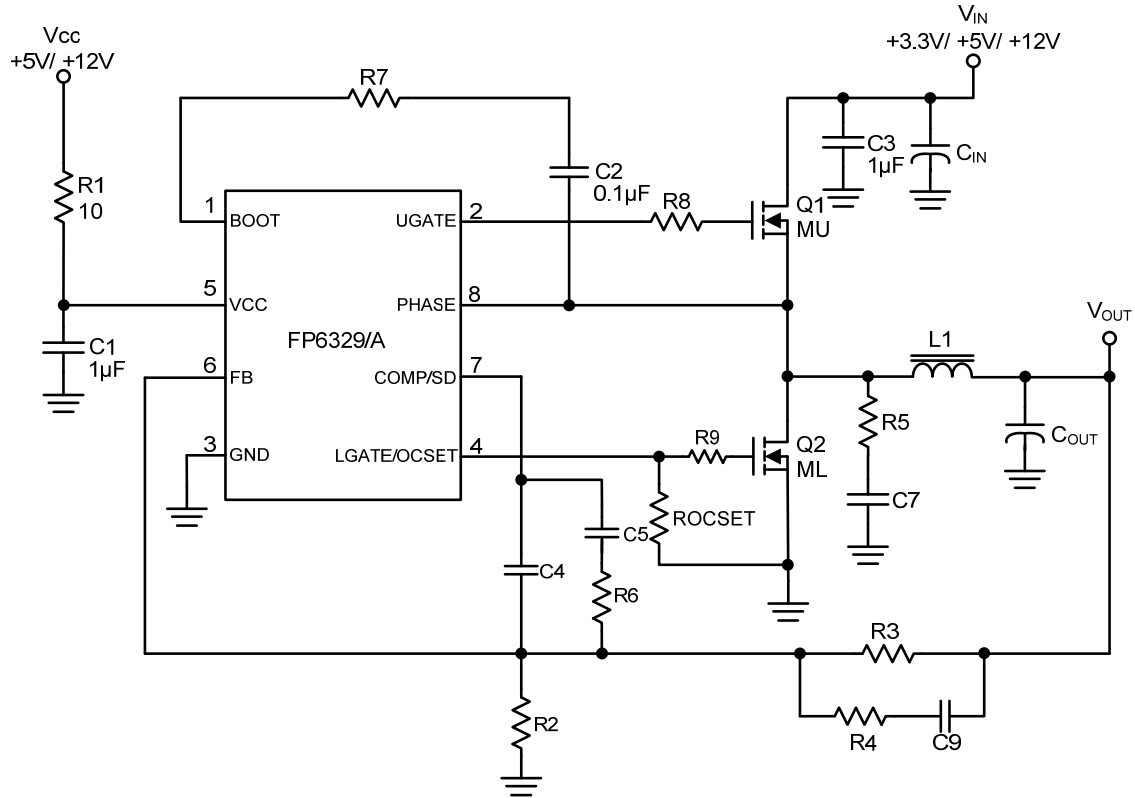


Figure 2. Typical Application Circuit of FP6329/A

Functional Pin Description

Pin Name	Pin Function
BOOT	This pin provides bias voltage to the high side MOSFET Driver. A bootstrap circuit may be to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.
UGATE	Connect UGATE to the high side MOSFET gate. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high side MOSFET has turned off.
GND	Ground.
LGATE/OCSET	Connect LGATE to the low side MOSFET gate. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high side MOSFET has turned off. Connect a resistor (R _{OCSET}) from this pin to GND to determine the over-current threshold of the converter.
VCC	Power Pin.
FB	Feedback Pin. The typical reference voltage is 0.6V.
COMP/SD	PWM error amplifier output and Shutdown Control pin. It can be used to compensate the voltage control feedback loop of the converter
PHASE	Connect the PHASE pin to the high side MOSFET source.



Absolute Maximum Ratings

- VCC to GND ----- - 0.3V to +16V
- BOOT, V_{BOOT} - V_{PHASE} ----- - 0.3V to +16V
- PHASE ----- -5V to +16V
- UGATE ----- V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
- LGATE ----- -0.3V to VCC+0.3V
- FB,COMP to GND ----- - 0.3V to +6V
- Continuous Power Dissipation @ T_A=+25°C (P_D) -----
 - SOP-8 ----- +0.63W
 - SOP-8 (Expose Pad)----- +1.25W
- Package Thermal Resistance, SOP-8 (θ_{JA})-----
 - SOP-8 ----- +160°C/W
 - SOP-8 (Expose Pad)----- +80°C/W
- Junction Temperature ----- +150°C
- Storage Temperature Range----- - 65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ----- +260°C

Note1 : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage, V_{CC} ----- 5V ±5%, 12V ±10%
- Operating Temperature Range ----- -40°C to +85°C

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Block Diagram

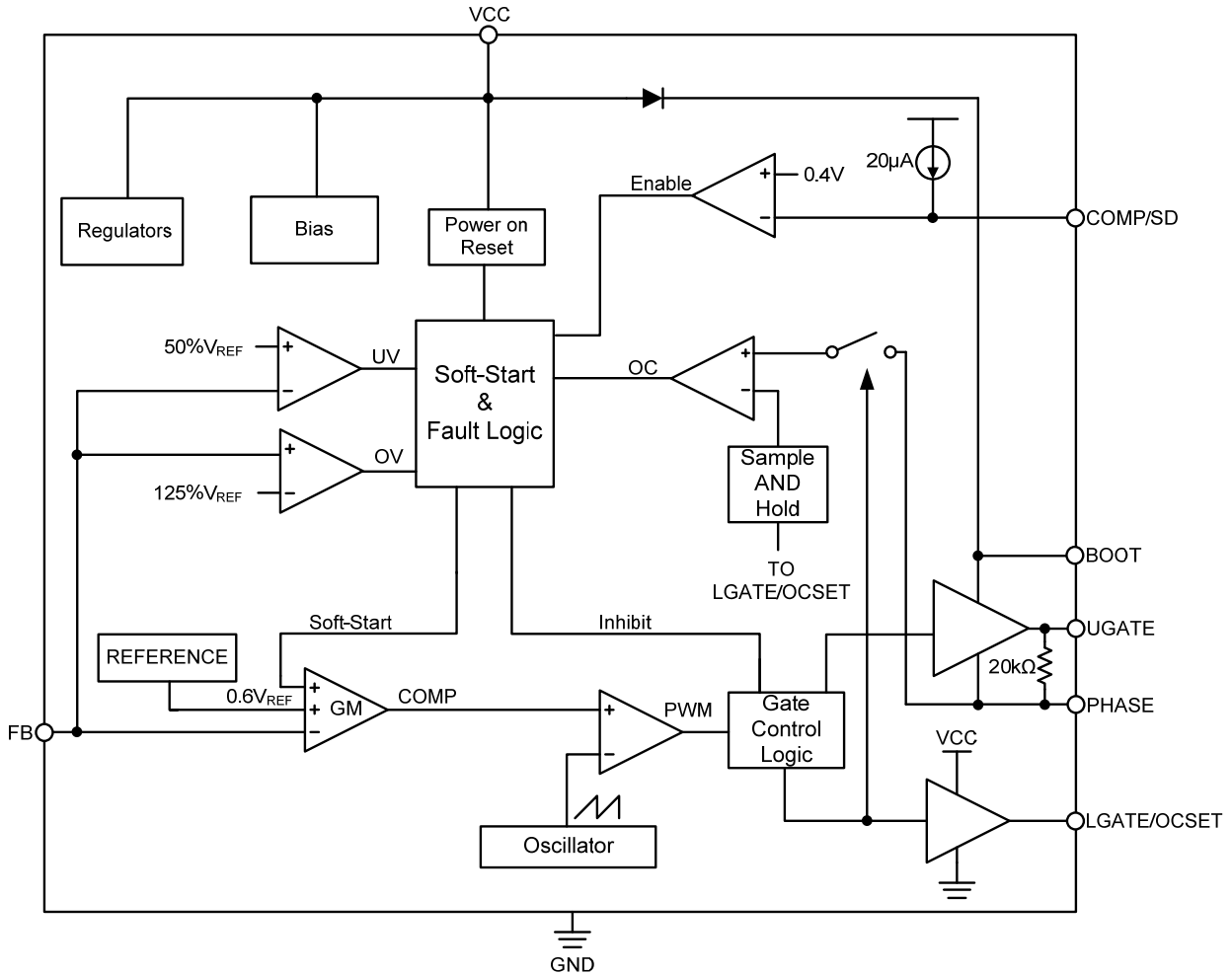


Figure 3. Block Diagram of FP6329/A

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Electrical Characteristics

($V_{CC}=12V$, $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT						
V _{CC} Under Voltage Lockout	V _{UVLO}	V _{CC} rising	3.9	4.1	4.3	V
UVLO Hysteresis		V _{CC} falling		0.45		V
Quiescent Current	I _{CC}	UGATE and LGATE open		5		mA
ERROR AMPLIFIER						
Feedback Voltage	V _{FB}		0.591	0.6	0.609	V
FB Input Bias Current	I _{FB}	V _{FB} =1V		0.1		μA
Open Loop DC gain (Note2)	A _O			88		dB
Open Loop Bandwidth (Note2)	BW			15		MHz
Slew Rate (Note2)	SR			9		V/μs
OSCILLATOR						
Frequency	F _{OSC}	FP6329	270	300	330	kHz
		FP6329A	540	600	660	
Ramp Amplitude (Note2)	ΔV _{OSC}			1.5		V _{p-p}
GATE DRIVERS						
Upper Gate Source Current (Note2)	I _{UGATE}	V _{BOOT} =12V, V _{UGATE} -V _{PHASE} =2V		2.6		A
Upper Gate Sink Impedance	R _{UGATE}	V _{BOOT} =12V, I _{UGATE} =0.1A		1.6		Ω
Lower Gate Source Current (Note2)	I _{LGATE}	V _{VCC} =12V, V _{LGATE} =2V		4.9		A
Lower Gate Sink Impedance	R _{LGATE}	V _{VCC} =12V, I _{LGATE} =0.1A		1.25		Ω
Dead Time (Note2)	T _{DT}				100	ns
PROTECTION						
FB Under-Voltage Trip		FB falling	40	50	60	%
FB Over-Voltage Trip				125		%
OCSET Current Source	I _{OCSET}		19.5	21.5	23.5	μA
Disable Threshold	V _{DISABLE}	COMP/SD falling	0.3	0.4	0.5	V

Note2 : The specification is guaranteed by design, not production tested.

Typical Performance Curves

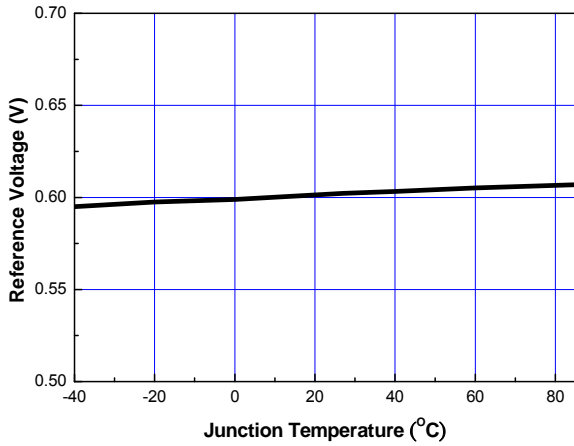


Figure 4. Reference Voltage vs. Junction Temperature

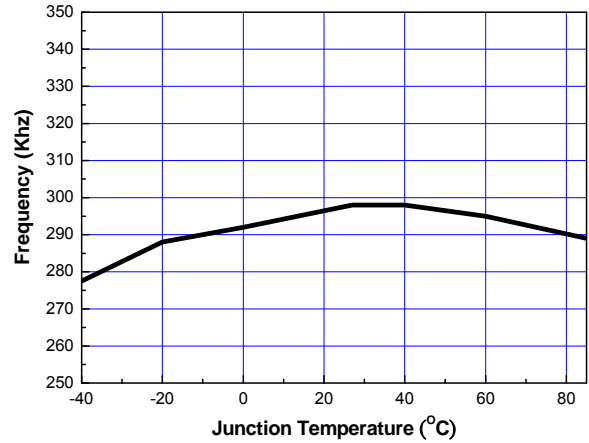


Figure 5. Frequency vs. Junction Temperature

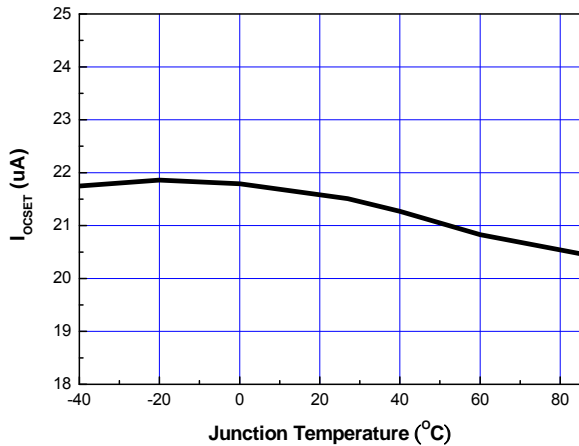


Figure 6. OCSET Current Source vs. Junction Temperature

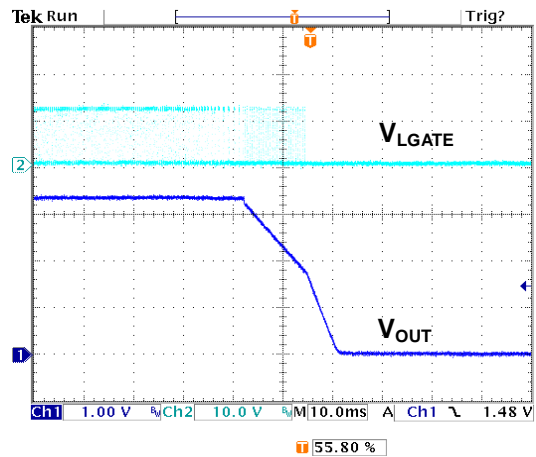


Figure 7. Under Voltage Protection

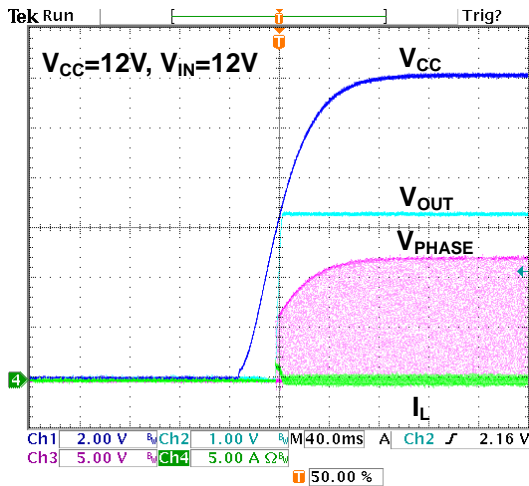


Figure 8. Power On at 0A Loading

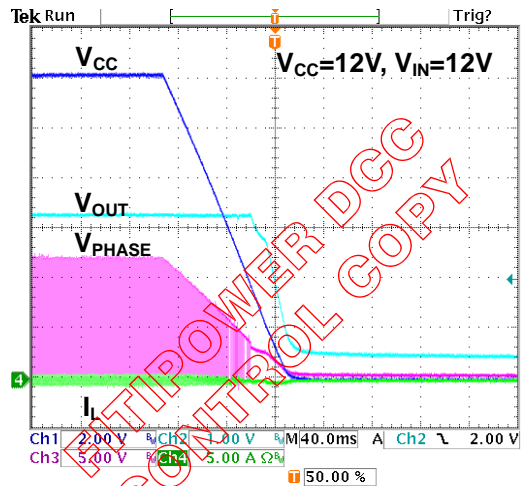


Figure 9. Power Off at 0A Loading

Typical Performance Curves (Continued)

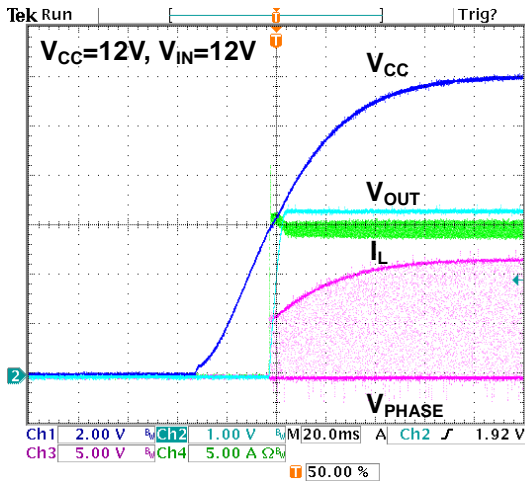


Figure 10. Power On at 15A Loading

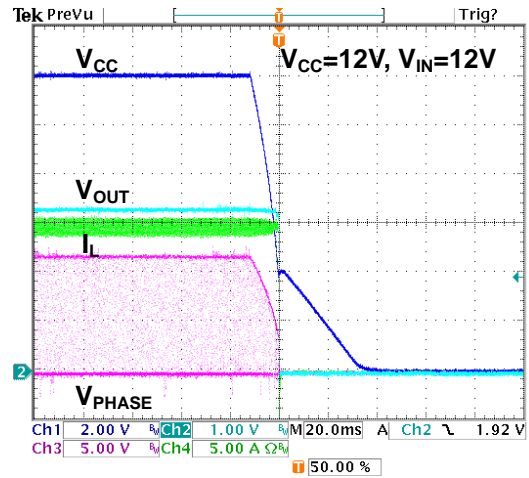


Figure 11. Power Off at 15A Loading

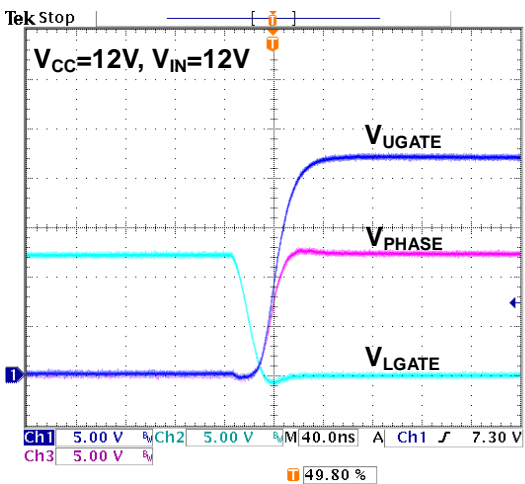


Figure 12. Switching waveform (UGATE rising) $I_{OUT}=0A$

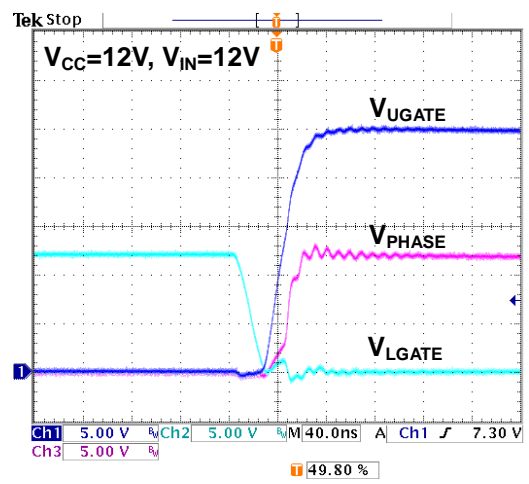


Figure 13. Switching waveform (UGATE rising) $I_{OUT}=15A$

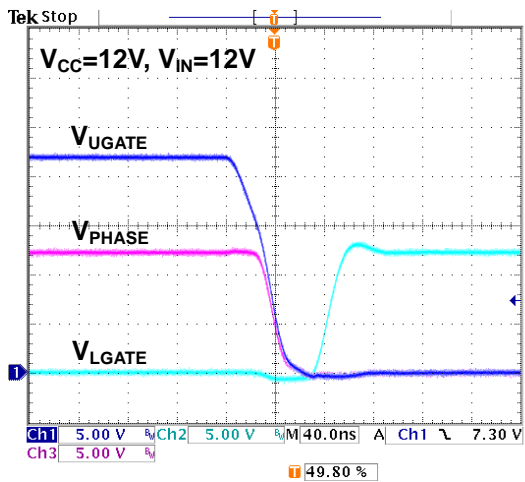


Figure 14. Switching waveform (UGATE Falling) $I_{OUT}=0A$

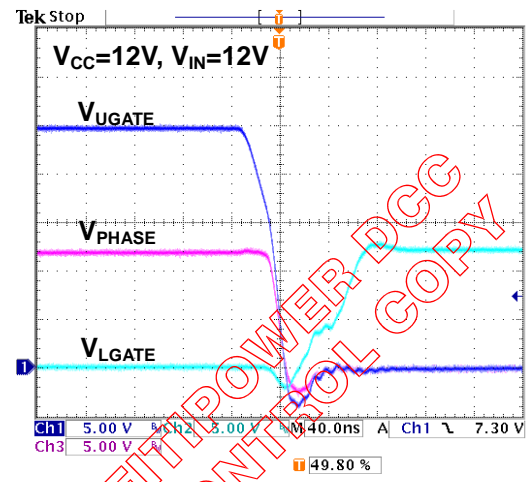


Figure 15. Switching waveform (UGATE Falling) $I_{OUT}=15A$

Typical Performance Curves (Continued)

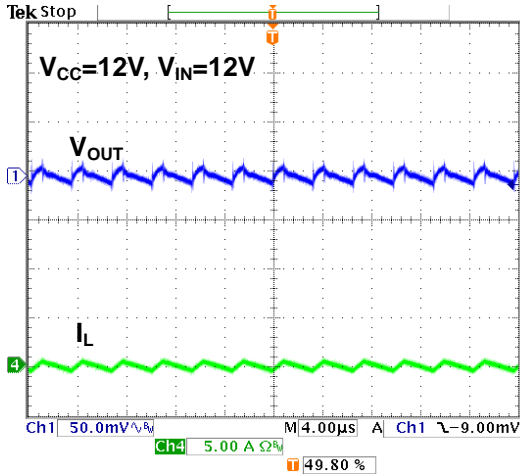


Figure 16. Output Ripple at 0A

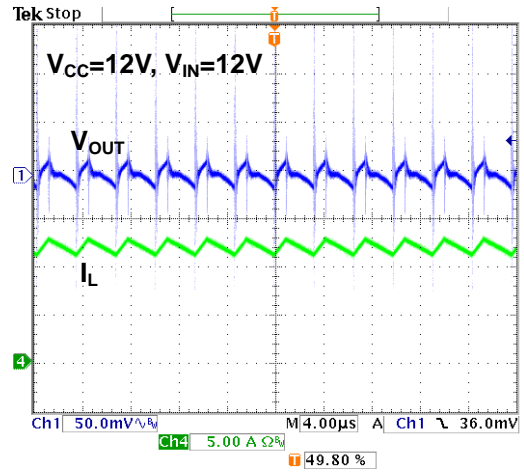


Figure 17. Output Ripple at 15A

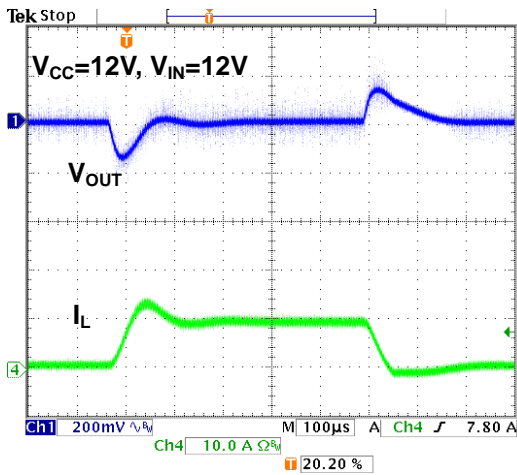


Figure 18. Transient test: Slew rate:2.5A/us,(1A to 10A)

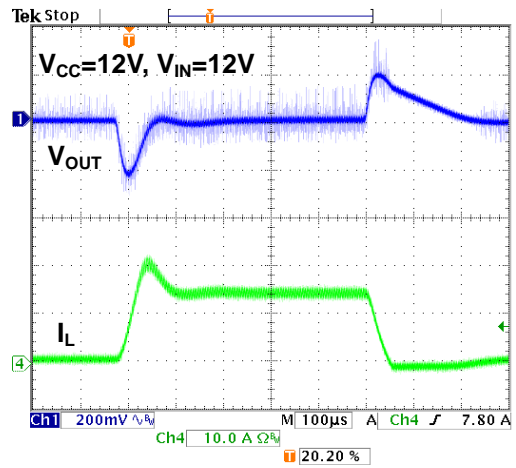


Figure 19. Transient test: Slew rate:2.5A/us, (1A to 15A)

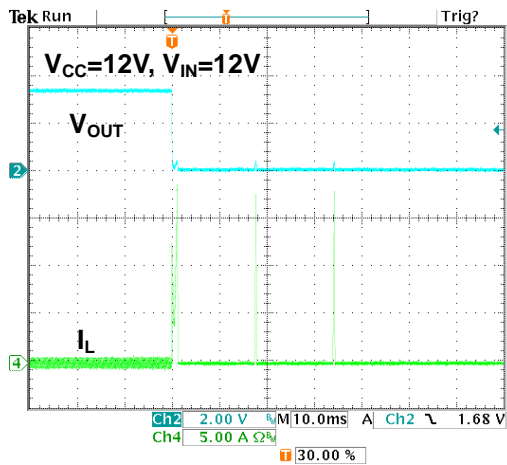


Figure 20. Output short after power on

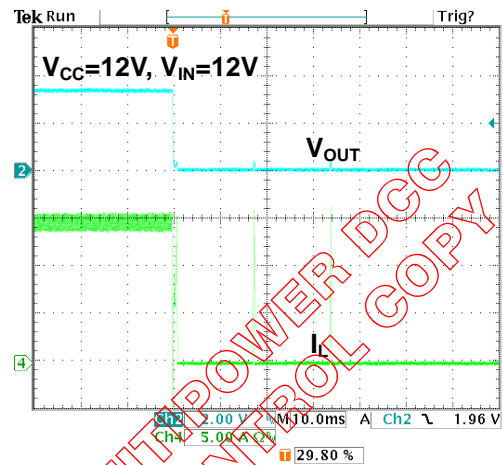


Figure 21. OCP using DC loading

Typical Performance Curves (Continued)

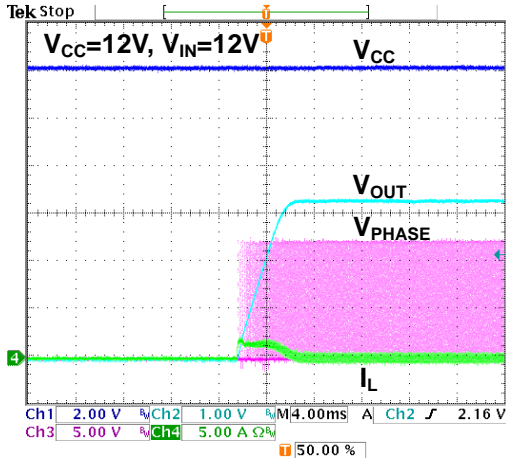


Figure 22. Power On with Enable at 0A Loading

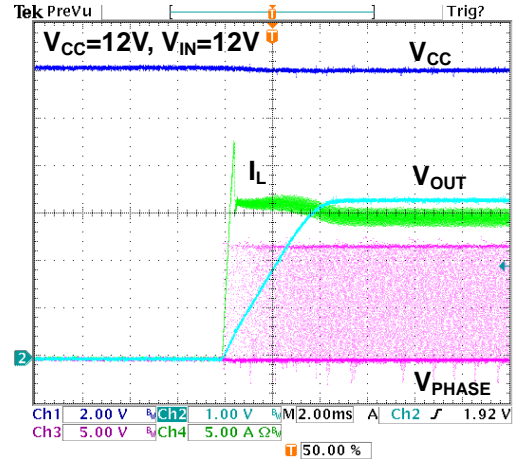


Figure 23. Power On with Enable at 15A Loading

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Functional Description

The Power-On Reset (POR) function continually monitors the input supply voltage and the enable function. The POR monitors the bias voltage at the VCC pin. When VCC power is ready, the FP6329/A starts to ramp up the output voltage up to the target voltage.

Soft-Start

The FP6329/A features soft-start to limit inrush current and control the output voltage rise at start-up. The soft-start is accomplished by ramping the internal reference input from 0V to 0.6V. The soft-start interval is 3.5ms typical.

Over-Current Protection

The over-current function protects the converter a shorted output by using the low side MOSFET on-resistance R_{DS-ON} to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. After four times are counted, the high side and low side gate will turn off and the output is latched off until the VCC bias supply is re-started. A resistor (R_{OCSET}), connected from the gate of low side MOSFET to the source of low side MOSFET to set the over-current trigger level. An internal 21.5uA (typical) current source develops the voltage across the R_{OCSET} . The over-current setting equation is shown as below:

$$I_{OCSET} = \frac{2 \times 21.5\mu A \times R_{OCSET}}{R_{DS-ON}}$$

*Note: If $R_{OCSET} > 25k\Omega$, the over-current function will be disabled.

To avoid the normal operation trigger the OCP function at load transient and junction temperature. All parameters variation must be concerned.

- (1) The maximum R_{DS-ON} at the highest junction temperature.
- (2) The minimum OCSET current.

Shutdown

Connecting a small transistor to COMP/SD pin, and pulling the voltage of COMP/SD pin less than 0.4V can shutdown the FP6329/A. At this condition, the FP6329/A is shutdown and high side and low side MOSFETs are turned off.

Under-Voltage Protection

The under-voltage function monitors the FB voltage to protection the converter against the output short-circuit condition. The under-voltage threshold is $0.5 \times V_{REF}$. When UVP happens, the high side and low side gate will turn off and the output is latched off until the VCC bias supply is re-started.

Over-Voltage Protection

The over-voltage function monitors the FB voltage to protection the converter against the output from over-voltage. When the feedback voltage rises to $1.25 \times V_{REF}$, the FP6329/A turns on the low side MOSFET until the feedback voltage below the OVP threshold. During the soft start period, the over-voltage protection function is disabled.

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Application Information

Introduction

The FP6329/A integrated circuit is a synchronous PWM controller; it operates over a wide input voltage range. Being low cost, it is a very popular choice of PWM controller. This section will describe the FP6329/A application suggestion. The operation and the design of this application will also be discussed in detail.

Design Procedures

This section will describe the steps to design synchronous buck system, and explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop.

(1) Synchronous Buck Converter

Since this is a buck output system, the first quantity to be determined is the duty cycle value. The formula calculated the PWM duty ratio; apply to the system which we propose to design:

$$\text{Duty ratio } D = \frac{V_O + V_{DS(\text{sat}), \text{Lowside } N}}{V_{IN} - V_{DS(\text{sat}), \text{Highside } N} + V_{DS(\text{sat}), \text{Lowside } N}} = \frac{T_{ON}}{T_S}$$

(2) Inductor Selection

To find the inductor value it is necessary to consider the inductor ripple current. Choose an inductor which operated in continuous mode down to 10 percent of the rated output load:

$$\Delta I_L = 2 \times 10\% \times I_O$$

The inductor "L" value for this system is connected to be:

$$L \geq \frac{(V_{IN} - V_{DS(\text{sat})} - V_O) \times D_{\text{MIN}}}{\Delta I_L \times f_S}$$

If the core loss is a problem, increasing the inductance of L will be helpful. But large inductor values reduce the converter's response time to a load transient.

(3) Output Capacitor Selection

The output capacitor is required to filter the output noise and provide regulator loop stability. When selecting an output capacitor, the important capacitor parameters are Equivalent Series Resistance (ESR), the RMS ripples current rating, the voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.

The ESR can be calculated from the following formula.

$$\text{ESR} = \left(\frac{V_{\text{RIPPLE}}}{\Delta I_L} \right)$$

An aluminum electrolytic capacitor's ESR value is related to the capacitance and its voltage rating. In most case, higher voltage electrolytic capacitors have lower ESR values. Most of the time, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage.

(4) Input Capacitor Selection

The RMS current rating of the input capacitor can be calculated as below:

$$I_{IN(\text{rms})} = I_{OUT} \times \sqrt{D(1-D)}$$

This capacitor should be located close to the IC using short leads and the volt age rating should be approximately 1.5 times the maximum input voltage.

(5) Output N-channel MOSFET Selection

The current ability of the output N-channel MOSFETs must be at least more than the peak switching current I_{PK} . The voltage rating V_{DS} of the N-channel MOSFETs should be at least 1.25 times the maximum input voltage. Choose the low R_{DS-ON} MOSFETs for reducing the conduction power loss. Choose the low C_{ISS} MOSFETs for reducing the switching loss. But most of time, the two factors are trade-off. Consider the system requirement and define the MOSFETs rating. The MOSFETs must be fast (switch time) and must be located close to the FP6329/A using short leads and short printed circuit traces. In case of a large output current, we must layout a copper to reduce the temperature of these two MOSFETs.

Application Information (Continued)

Compensation the Converter

The FP6329/A single-phase converter is a voltage-mode controller. The design consideration for a voltage-mode controller requires external compensation. Proper compensation of the system will allow for a calculable bandwidth. In most case, a Type III compensation network is recommended. The target of the compensation network is to provide the closed loop transfer function with 0dB crossing frequency and sufficient phase margin (greater than 45°).

The buck converter is composed of three basic blocks as Figure24 shown: modulator, output filter, and compensation network. Figure26 is the voltage-mode control loop with Type III compensation for synchronous rectified buck converter.

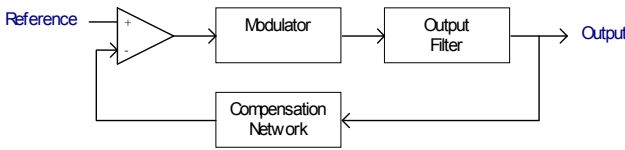


Figure24. Basic structure of the buck converter

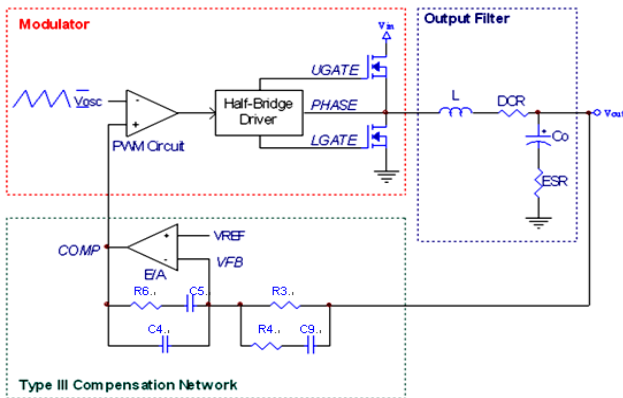


Figure25. Voltage-mode buck converter compensation

The error amplifier output is compared with the oscillator triangle wave to provide a PWM wave. The gain of modulator is input voltage divided by the ramp amplitude.

$$GAIN_{MODULATOR} = \frac{V_{IN}}{V_{OSC}}$$

$$GAIN_{MODULATOR} (dB) = 20 \log \frac{V_{IN}}{V_{OSC}}$$

The output filter includes the inductor and the output capacitance. Remember that do not ignore the DCR of the inductor and the ESR of output capacitor. The transfer function for the output filter shows a double pole break frequency at F_{LC} of LC filter and a zero at F_{ESR} of Co and ESR.

$$GAIN_{FILTER} = \frac{1 + S \cdot C_O \cdot ESR}{1 + S \cdot (ESR + DCR) \cdot C_O + S^2 \cdot L \cdot C_O}$$

Output filter break frequency equation

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_O}}, \quad F_{ESR} = \frac{1}{2\pi \cdot C_O \cdot ESR}$$

The open loop small-signal transfer function is dominated by a DC gain and developed by the double pole at F_{LC} and a zero at F_{ESR} . Figure26 represents the Bode plot of the open loop system gain. The system has different double pole and zero frequency. The phase will decline a sharp slope at the double pole for system with very low DCR and ESR parameters. System will more difficult to compensate while the phase needs an extra boost to provide required phase margin for stability.

$$GAIN_{OPENLOOP} = GAIN_{MODULATOR} \cdot GAIN_{FILTER}$$

$$= \frac{V_{IN}}{V_{OSC}} \cdot \frac{1 + S \cdot C_O \cdot ESR}{1 + S \cdot (ESR + DCR) \cdot C_O + S^2 \cdot L \cdot C_O}$$

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Application Information (Continued)

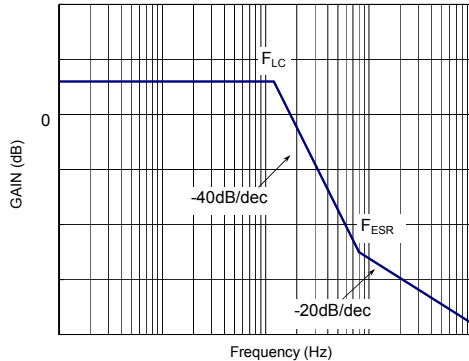


Figure 26. Bode plot of open loop gain

Proper Type III compensation of the system closes the control loop to allow for a desired bandwidth with stability. The ideal Bode plot for compensation system should be satisfied two conditions; one is a gain that decline with -20dB/decade slope and cross 0dB at the predictable bandwidth. Another one is phase margin greater than 45° below the 0dB crossing.

$$GAIN_{TYPEIII} = \frac{R3+R4}{R3 \cdot R4 \cdot C4} \cdot \frac{(S + \frac{1}{C9 \cdot (R3+R4)}) (S + \frac{1}{R6 \cdot C5})}{S(S + \frac{C4+C5}{R6 \cdot C4 \cdot C5}) (S + \frac{1}{R4 \cdot C9})}$$

Compensation break frequency equation

$$F_{P1} = \frac{1}{2\pi \cdot \frac{R6 \cdot C4 \cdot C5}{C4 + C5}}, \quad F_{P2} = \frac{1}{2\pi \cdot R4 \cdot C9}$$

$$F_{Z1} = \frac{1}{2\pi \cdot R6 \cdot C5}, \quad F_{Z2} = \frac{1}{2\pi \cdot R4 \cdot (R3 + R4)}$$

Figure 27 shows the transfer function of closed loop system with Type III compensation. The Type III compensation network applies two zeroes to give a 180° boost to the phase. This boost is necessary to contract the effect of an under damped at the double pole.

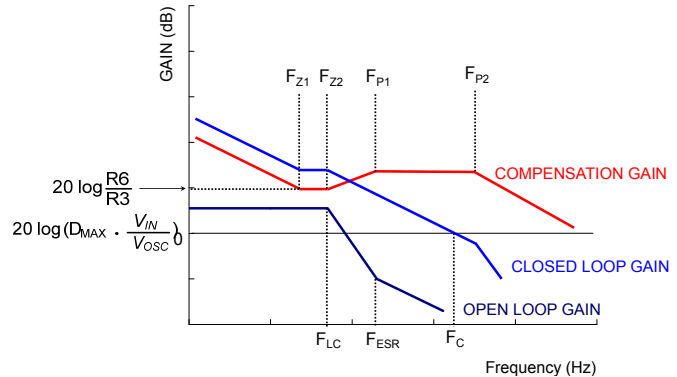


Figure 27. Bode plot of converter closed loop gain

The following guidelines will help calculate the poles and zeroes of the compensation network.

1. Select R1, 1kΩ to 10kΩ typically.
2. Choose a gain (R6/R3) that will shift the open loop gain to the desired bandwidth, Fc (1/10 to 1/4 of Fsw). R6 can be calculated by the equation:

$$R6 = \frac{V_{OSC}}{V_{IN}} \cdot \frac{F_C}{F_{LC}} \cdot R3 \cdot D_{MAX}$$

where D_{MAX}=1, since FP6329/A supports 100% duty cycle.

V_{OSC}=1.5V, the FP6329/A uses a 1.5V ramp amplitude.

$$R6 = \frac{V_{OSC}}{V_{IN}} \cdot \frac{F_C}{F_{LC}} \cdot R3 \cdot D_{MAX} = \frac{1.5 \cdot F_C \cdot R3}{V_{IN} \cdot F_{LC}}$$

3. Calculate C5 to place first zero, F_{Z1}, before F_{LC}. F_{Z1} is adjustable from 0.1 to 0.75 of F_{LC}. Usually pick the 0.5 factor.

$$C5 = \frac{1}{2\pi \cdot R6 \cdot 0.5 \cdot F_{LC}} = \frac{1}{\pi \cdot R6 \cdot F_{LC}}$$

4. Calculate C4 to place first pole, F_{P1}, at F_{ESR}.

$$C4 = \frac{C5}{2\pi \cdot R6 \cdot C5 \cdot F_{ESR}^{-1}}$$

5. Calculate R4 to place second zero, F_{Z2}, at the output filter double pole, F_{LC}.

$$R4 = \frac{R3}{F_{SW} / F_{LC} - 1}$$

6. Calculate C9 to place second pole, F_{P2}, lower than F_{LC}. F_{P2} is adjustable from 0.3 to 1.0 of F_{SW}. Usually set the F_{P2} at half the switching frequency. Set F_{P2} lower in frequency helps reduce the gain of the compensation network in high frequency and minimize duty cycle jitter.

$$C9 = \frac{1}{2\pi \cdot R4 \cdot 0.5 \cdot F_{SW}} = \frac{1}{\pi \cdot R4 \cdot F_{SW}}$$

Application Information (Continued)

Layout Notice

When designing a high frequency switching regulated power supply, layout is very important. Using a good layout can solve many problems associated with these types of supplies. The problems due to a bad layout are often seen at high current levels and are usually more obvious at large input to output voltage differentials. Some of the main problems are loss of regulation at high output current and/or large input to output voltage differentials, excessive noise on the output and switch waveforms, and instability. Using the simple guidelines that follow will help minimize these problems.

(1) Inductor

Always try to use a low EMI inductor with a ferrite type closed core. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components.

(2) Feedback

Try to put the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. It is often a good idea to run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

(3) Filter Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the VIN pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Sometimes using a small resistor between V_{CC} and IC VCC pin will more useful because the RC will be a low-pass filter. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons.

(4) Compensation

If external compensation components are needed for stability, they should also be placed closed to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors.

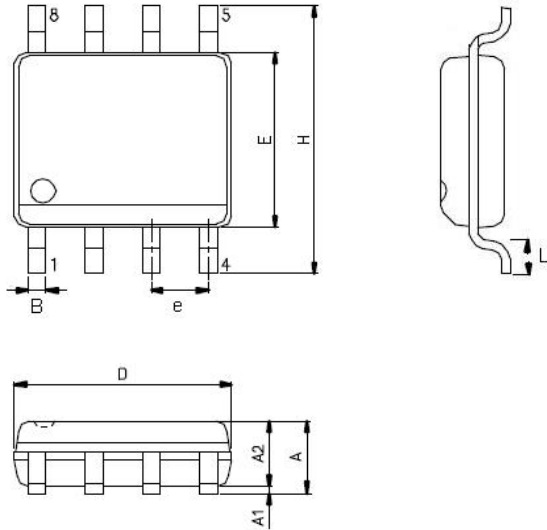
(5) Traces and Ground Plane

Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15mils (0.381mm) per Ampere. The inductor, output capacitors, and low side switch should be as close to each other possible. This will reduce lead inductance and resistance as well which in turn reduces noise spikes, ringing, and resistive losses which produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and low side switch should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane and the signal plane for improved performance. It is good practice to use one standard via per 200mA of current if the trace will need to conduct a significant amount of current from one plane to the other. Due to the way switching regulators operate, there are power on and power off states. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction.

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Outline Information

SOP- 8 Package (Unit: mm)



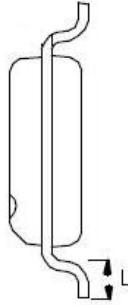
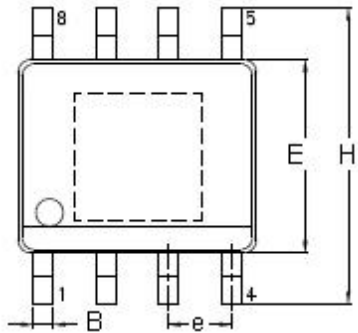
SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.35	1.75
A1	0.05	0.25
A2	1.30	1.50
B	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note 1 : Followed From JEDEC MO-012-E.

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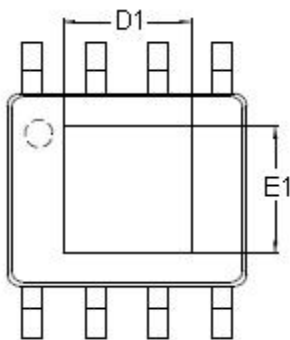
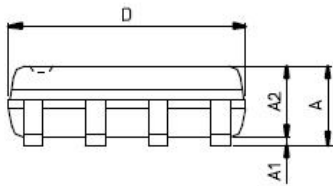
Outline Information (Continued)

SOP- 8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	2.25	3.80
E	3.80	4.00
E1	2.25	3.80
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note 1 : Followed From JEDEC MO-012-E.



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Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical system